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Using sputter deposition, nonepitaxial ultrathin film capacitors consisting of $SrRuO_3$ electrodes and dielectric $SrTiO_3$ (STO) were grown directly on oxidized silicon substrates. The surface roughness of the layers was found to be very low ($\lesssim$0.2 nm). Dielectric measurements as a function of temperature were performed on samples with different STO thickness down to 7 nm, showing temperature dependence of the interfacial passive layers. The dielectric constant of the STO films was found to be in the range of 200 at room temperature for all samples, which leads to a minimum capacitance equivalent thickness below 0.2 nm. © *2010 American Institute of Physics*.
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$SrTiO_3$ (STO) belongs to the most promising candidates of high permittivity materials in capacitors for future dynamic random access memory (DRAM) applications.[1–3] There is wide experience in the growth of metal-insulator-metal (MIM) structures containing electrode materials like Pt, Au, Ru, RuO_2, or Ti.[4–7] The low lattice mismatch with $SrRuO_3$ (SRO) allows for the heteroepitaxial growth of MIM structures.[8–11] In spite of these numerous results, a typically observed decline of the dielectric constant with decreasing STO film thickness due to the formation of interfacial passive layers seems to be inevitable. These passive layers are believed to have permittivity significantly below the value of the dielectric independent of the film thickness. The possible explanations of this effect are various and range from a finite electrostatic screening length in the electrode over growth-induced defects and strain effects to effects of the electrode material.[8,12–18]

In this paper, we report on the fabrication of SRO/STO/SRO ultrathin film capacitors on oxidized silicon substrates showing an effective permittivity value of 200 at a physical STO thickness of 10 nm and below. The capacitors were analyzed with respect to interfacial passive layers and their temperature dependence.

The MIM structures were deposited *in situ* on oxidized silicon substrates by low-rate rf sputtering from pressed powder SRO and sintered STO targets with 1 in. diameter. Growth conditions were a substrate temperature of 550 °C and a chamber pressure of 8×10^{-3} mbar Ar for both the SRO and STO deposition. The initial partial pressure of other gases, for instance oxygen, is several orders of magnitude lower and settles in the range of 10^{-7} mbar. The deposition of SRO on SiO_2 did not require adhesion layers. Prehandling procedures include wafer rinsing in acetone, isopropanol, and deionized water. The top SRO layers were patterned by depositing a Pt hard mask via photolithography, lift-off, and dry etching by Ar-ion beam. Atomic force microscopy (AFM) was performed using a Veeco CP-2 in noncontact mode. The particular thickness and the surface roughness of each film of the trilayer structure was determined by x-ray reflectometry (XRR) using a Cu k_α x-ray source and was partially confirmed by FIB-cut SEM cross sections. Grazing incident x-ray diffraction (GI-XRD) measurements were performed at a constant incident angle of 0.5°. The capacitance of the MIM structures was measured using a HP 4284 A LCR-meter. The measurements were performed with various top electrode areas, for which the displayed curves are representative. This is intended to mostly eliminate the inaccuracy of the top electrode area due to lithography or the patterning process.

The room temperature resistivity of the SRO films was determined by the van der Pauw[19] method and found to be about 500 $\mu\Omega$ cm, which is near to that of epitaxial SRO thin films[9,20] and SRO single crystals.[21] The morphology of the films' surfaces is shown in Fig. 1. The root-mean-square roughness values were 0.14 ± 0.1 nm for the SRO surface and 0.2 ± 0.1 nm for the STO surface, respectively. These values corresponded to the values obtained by XRR. Representative results of the films' structure are illustrated in Fig. 2. For comparison, the GI-XRD pattern of a 100 nm SRO bottom layer is shown in addition to the XRD spectrum of a complete SRO/STO/SRO stack. The pure SRO layer showed several peaks which can be assigned to polycrystalline SRO pseudocubically indexed. The broad shape of the peaks is due to the small grain size, following the Scherrer equation.[22] From the pattern of the SRO/STO/SRO stack an additional peak at about 40° appeared which was identified

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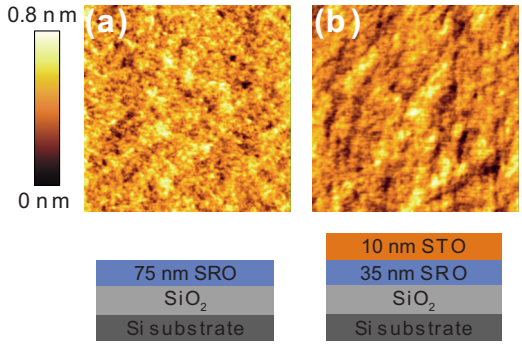

FIG. 1. (Color online) AFM images and schematic cross-sections of (a) SRO on SiO_2 and (b) STO/SRO bilayer. Scan area is 1×1 μm^2.

as the polycrystalline (111) reflex of STO. Other STO peaks were hidden by the SRO reflexes.

The room temperature capacitance equivalent thickness (CET) of the polycrystalline STO thin films as a function of the applied electric field defined as $E=V/t$ is shown in Fig. 3. The CET was calculated using the equation

$$\mathrm{CET} = \varepsilon_0 \varepsilon_{\mathrm{SiO_2}} \frac{A}{C_{\mathrm{meas}}}, \tag{1}$$

where A is the capacitor area, C_{meas} is the measured capacitance, and $\varepsilon_{\mathrm{SiO_2}}=3.9$ is the permittivity of silicon dioxide. The field-dependence is characteristic for perovskite titanates.[23] The thinnest STO layer showed a CET below 0.2 nm for a field range of ±800 kV/cm, however with insufficient leakage current density. The 10 nm STO layer showed a CET well below 0.3 nm with leakage current density in the order of 10^{-7} A/cm^2 and dissipation factor below 0.02 for a field range of ±800 kV/cm. Following the international technology roadmap for semiconductors, this fully meets the end of roadmap prediction for DRAM applications.[24] Temperature dependent measurements of the zero bias capacitance were performed in a wide temperature range. The reciprocal capacitance density over STO film thickness for different temperatures is given in Fig. 4. The data set for each temperature was linearly fitted, for which the displayed lines are shown exemplarily. These lines all have a y-axis intercept near the origin, decreasing with increasing temperature. The intercept at room temperature shows a reciprocal capacitance density of about 0.027 m^2/F,

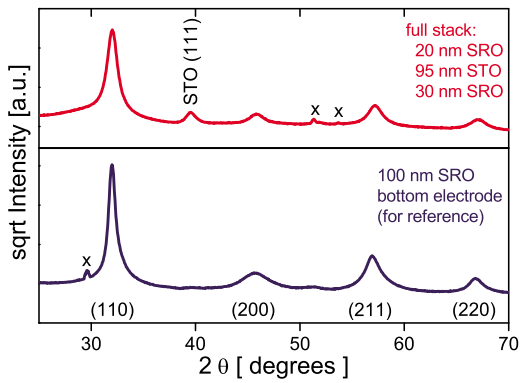

FIG. 2. (Color online) GI-XRD patterns of the depicted thin films. The peaks can be assigned to the displayed SRO and STO phases. Peaks marked with "x" are artifacts due to edge effects of the Si substrates.

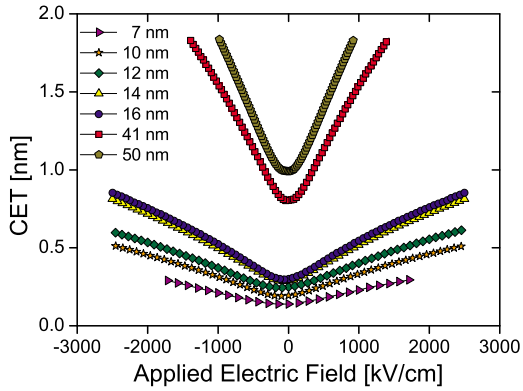

FIG. 3. (Color online) CET as function of electric dc bias field. No field offset correction has been performed. CET is calculated from 1 kHz C-V measurements with 50 mV small signal assuming a parallel plate capacitor structure. Neither variation of small signal frequency to 10 kHz nor reduction of the small signal bias down to 10 mV showed significant differences.

which is very small compared to values from literature.[4,8,17,25]

Applying the common series capacitor model for passive layers, the reciprocal capacitance can be expressed by the equation

$$\frac{A}{C_{\mathrm{meas}}} = \frac{t}{\varepsilon_0 \varepsilon_{\mathrm{eff}}} = \frac{t_i}{\varepsilon_0 \varepsilon_i} + \frac{t - t_i}{\varepsilon_0 \varepsilon_b}, \tag{2}$$

where t_i and ε_i are the thickness and permittivity of the interfacial passive layers, respectively, t is the total thickness, and ε_b is the bulk permittivity.

We are aware of the fact that from this analysis it is only possible to obtain the relation t_i/ε_i, of which the maximum, i.e., at the lowest temperature, was determined to be 4.25 pm. However, further analysis of this relation, as Takahashi *et al.*[26] had proposed, did not help in clearly determining the interface thickness t_i or its permittivity ε_i. This is due to the fact that the linear fitting of the equation

$$\frac{1}{\varepsilon_{eff}} = \frac{1}{\varepsilon_b} + \left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_b}\right)\frac{t_i}{t}, \tag{3}$$

resulted in large errors, as the determination of the permittivity requires the STO film thickness, which is associated with higher uncertainty. However, the intercepts of these fits, which are determined by the bulk permittivity, showed similar values to those obtained from the slopes of Fig. 4, which

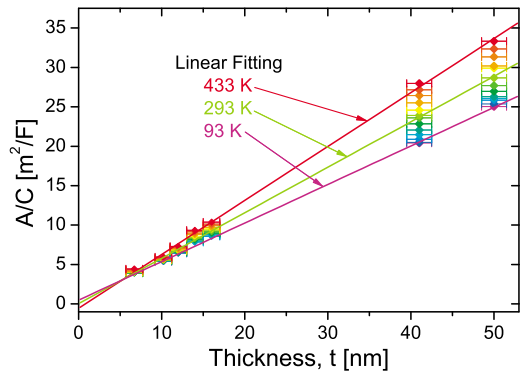

FIG. 4. (Color online) Reciprocal capacitance density as a function of STO film thickness t at varying temperature. The lines are linear fits at displayed temperatures. Error bars along the A/C axis are smaller than the symbols.

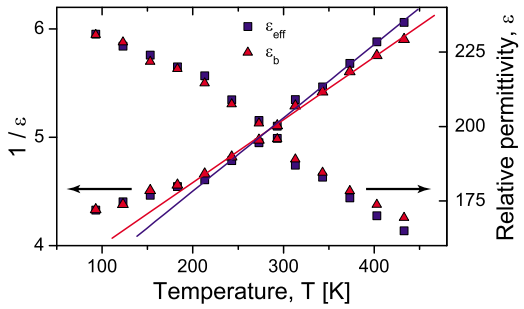

FIG. 5. (Color online) Effective permittivity and reciprocal permittivity as function of temperature. For comparison, the data points were derived from the slopes (squares) in Fig. 4 and from the intercepts (triangles) of Eq. (3). The difference in temperature dependence is likely to have its origin in a temperature dependence of the interface capacitance. Both data sets follow a Curie–Weiss behavior (solid lines) for temperatures above 200 K.

are determined by the effective permittivity. Still, there was a systematic deviation, as can be seen in Fig. 5. A possible explanation was a temperature dependence of the interface capacitance. This became more apparent because of the moderate temperature dependence of the permittivity compared to materials like $(Ba,Sr)TiO_3$ (BST) and also single crystal STO, which typically show a stronger temperature dependence.[25]

The reasons for the insignificant interfacial passive layers of the investigated samples compared to other results in literature were more subject to conjecture. As mentioned in the beginning, there are numerous models for the explanation of interfacial passive layers and as many assumptions how their impact can be reduced. Our approach to prevent their formation was the combination of several factors. SRO as a perovskite electrode gave the best known material match with STO. The smooth surface of the layers provided interfaces of very high quality. Using *in situ* vacuum processing of the complete capacitor stack at elevated temperatures, targets of high purity, and inert process gas prevented contamination of the deposited layers.

Apart from the processing and material approach, a finite electronic screening length is an intrinsic effect of the metal-insulator interface and therefore cannot be neglected. For instance, Black and Welser[14] introduced an effective dielectric constant for the electrode material and determined the effect of a Thomas Fermi screening length on MIM structures with BST as an exemplary high-*k* dielectric. Comparing these considerations with the investigated samples, we found good agreement with the order of magnitude of the derived interface capacitances. However, there was an amount of uncertainty which made it impossible to clearly distinguish the origin of interfacial passive layers and isolate the decisive effect, which is in agreement with literature.[27]

In summary, we fabricated SRO/STO/SRO ultrathin film capacitors on oxidized silicon substrates by rf sputtering. Capacitance measurements showed the STO films to have a dielectric constant of about 200 without indicating significant interfacial passive layers. This makes the investigated material combination to be one of the most promising candidates for far future DRAM capacitor applications.

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