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The effect of growth temperature on AlAs/GaAs resonant tunnelling diodes

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Abstract. In this paper we report on a systematic investigation of the influence of the growth temperature on the current voltage (I–V) characteristics of symmetric AlAs/GaAs double-barrier tunnelling diodes grown by molecular beam epitaxy (MBE) and a correlation between electrical and structural properties. It is shown by high-resolution transmission electron microscopy (HRTEM) that the growth temperature affects the interface roughness and the symmetry of the double-barrier region. Both the microstructure of the interfaces and the Si doping spreading in the double-barrier region have a significant influence on the peak-to-valley ratio (PVR) and the symmetry of the I–V characteristic. The substrate temperature was varied from 480 to 680 °C. It is demonstrated that the highest PVRs at room temperature are found for samples grown in the temperature range 580–600 °C.

A resonant tunnelling diode (RTD), first demonstrated by Chang *et al* [1], consists of two potential barriers in series, separated by a potential well. The properties of such diodes, namely the negative differential resistance and the possibility of operating at very high frequencies up to several hundred GHz, make them very attractive as multifunctional devices in ultrahigh speed circuits. In particular, the design of complex logical circuits might benefit from the use of such RTDs. In spite of this significance for potential applications many fundamental problems in the understanding of these devices are waiting for further elucidation, e.g. the factors that determine the peak-to-valley ratio (PVR) and the relative contributions of coherent and sequential tunnelling. In addition, in spite of an intentionally symmetrical barrier structure, the asymmetry in the I–V characteristics cannot be explained without taking into account details of the technological preparation processes.

In this context, the present paper reports on experimental investigations on AlAs/GaAs double-barrier RTDs, prepared by molecular beam epitaxy (MBE). In addition high-resolution transmission electron microscopy (HRTEM) was used to study the microstructural properties of the interfaces on an atomic scale. A correlation between microstructural characteristics of the RTDs and electrical properties of the diodes is presented in this paper. Furthermore, the influence of the spreading of the doping material and the growth temperature-related asymmetry of the double barriers are discussed.

The RTD samples were grown by molecular beam epitaxy (MBE) in a solid source Varian Mod-GenII system on n-type (Si-doped, $n = 1$–4×10^{18} cm^{-3}) (100)-oriented GaAs wafers. The GaAs layers were grown at a growth rate of 0.85 μm h^{-1} and the AlAs barriers at 0.35 μ m h^{-1} with a constant arsenic pressure of 1.4×10^{-5} mbar. The layer sequence was as follows: highly Si-doped GaAs substrate, 1 μm thick highly-doped GaAs buffer layer ($n = 4$–5×10^{18} cm^{-3}), 10 nm GaAs ($n = 10^{17}$ cm^{-3}), 10 nm GaAs ($n = 10^{16}$ cm^{-3}), 5 nm GaAs spacer, 6 monolayer (ML) AlAs barrier (1.7 nm), 5 nm GaAs well, 6 ML AlAs barrier, 5 nm GaAs spacer, 10 nm GaAs ($n = 10^{16}$ cm^{-3}), 10 nm GaAs ($n = 10^{17}$ cm^{-3}) and finally a 0.5 μm thick highly-doped n+ ($n = 4$–5×10^{18}) cm^{-3} GaAs top layer. The electron concentration was finally determined by capacitance–voltage (C–V) profile measurements. A series of several wafers were grown with different substrate temperatures from 480 to 680 °C. The temperatures were controlled with an IRCON infrared pyrometer. Growth rates were controlled by measuring the intensity oscillations in a reflection high-energy electron diffraction (RHEED) pattern.

All RTDs were designed as square mesa structures with dimensions from 4×4 μm^2 up to 30×30 μm^2. After a conventional lithography and lift-off process, the mesa structures were wet chemically etched with the Ni/AuGe ohmic contact serving as the etch mask. The complete reverse side of the wafer was also equipped with the same ohmic contact. I–V curves were recorded with an HP4145 B semiconductor parameter analyser. The contact was achieved directly on the mesa with gold probes.

HRTEM was carried out by examining cross-section samples, which were oriented along a ⟨100⟩ orientation

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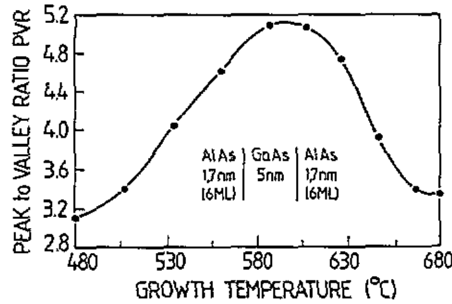

Figure 1. Ratio of the peak-to-valley current ratio (PVR) versus growth temperature of AlAs double barriers in GaAs.

parallel to the interface. A JEOL 4000 EX electron microscope operated at 400 kV, which is characterized by a spherical aberration constant of 1 mm, was used. Chemically sensitive imaging conditions were obtained by adjusting the objective lens defocus between −20 nm and −35 nm (underfocus) and using specimen thicknesses between 8 nm and 18 nm. Under these conditions, the appearance of the AlAs is dominated by the ⟨200⟩ lattice fringes and the GaAs by the ⟨220⟩ fringes [2].

The I–V curve of an RTD shows a clearly established negative differential resistance region both in the negative and in the positive voltage region. In figure 1 it is shown that the PVR is strongly dependent on the growth temperature. The results are split in two different regions: into the 'low' (below 580 °C) and the 'high' temperature range (above 580 °C). In the 'low' temperature range the PVR increases from 3.1 to 5.1 with the growth temperature, whereas in the 'high' temperature range the PVR decreases from 5.1 to 3.3. The mean deviation of the PVR at different mesas and different wafers is about 0.2. The maximum PVR was 5.35 at a current density of 4×10^4 A cm^{-2} for samples grown at about 580 °C. A strong temperature dependence is not only found in the PVR but also in the symmetry behaviour of the diodes. The ratios of the supply voltages at peak maximum 'left' and 'right' $(U_-(j_P)/U_+(j_P))$ and the corresponding ratios PVR_-/PVR_+ of the peak-to-valley ratios for negative and positive supply voltages, are chosen as parameters to demonstrate the degree of asymmetry (figure 2). For low substrate temperatures the I–V curves are nearly symmetrical and the ratios of the peak voltages $(U_+(j_P)/U_-(j_P))$ remain almost 1. This means that the two barriers must be of the same effective thickness. For growth temperatures higher than 580 °C asymmetrical I–V curves are observed (figure 2). Two reasons could account for this effect. First there could be a difference in the effective thickness of the two barriers and secondly an Si-doping segregation towards the surface could tilt the band structure of the diode.

Therefore HRTEM was used to study the microstructural properties of the interfaces on an atomic scale. It has previously been shown [3] that AlAs/GaAs interfaces do not exhibit chemically abrupt and completely flat interfaces even under optimum growth conditions. The transition between the GaAs and AlAs occurs within

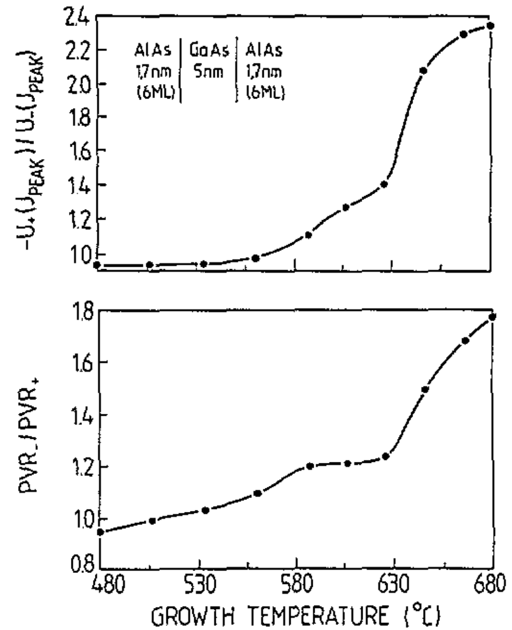

Figure 2. (a) Ratio of the peak voltages (U_{P-}/U_{P+}) and (b) the peak-to-valley current ratios (PVR_-/PVR_+) in positive and negative bias voltage supplied to the top layer.

2 to 4 monolayers (MLs). In addition, a lateral interface roughness is superimposed on the diffuse transition which can be characterized by step distances and step heights. Therefore the overall width of the interface region is determined by the width of the chemical transition region in growth direction and the superimposed lateral roughness. Both depend sensitively on the growth conditions.

At low growth temperatures, the normal and the inverted interface are expected to exhibit similar rough morphologies in terms of step distances (nanometre scale) and heights due to the slow surface diffusion of both the Al and the Ga atoms, during the growth. The interdiffusion of the group III elements is small, leading to narrow transition widths between GaAs and AlAs. Therefore, the RTD structure is symmetric because both interfaces have the same microstructure. Equal effective barrier thicknesses are indeed observed in the HRTEM image (figure 3(*a*)) for the specimen grown at 480 °C. From the gradual change of the image patterns between GaAs and AlAs, a chemical transition width of 2 to 3 MLs was determined. Two reasons could account for this observation. The first possibility is interdiffusion, which is unlikely at low temperatures. The second possibility is a lateral roughness whose scale is smaller than the specimen thickness, which is the more likely explanation for the diffuse appearance of the interfaces. Significant differences between the normal and inverted interfaces are not observed for the 480 °C samples. The diffuse appearance of the interfaces therefore most likely results from a microroughness on a scale less than the specimen thickness of 8 to 18 nm rather than from interdiffusion.

For the sample grown at 580 °C (figure 3(*b*)), an abrupt change of the image patterns between GaAs and AlAs within 1–2 MLs is observed for the normal and the inverted interface, indicating a narrow interdiffusion region. Steps at the interfaces can be clearly localized

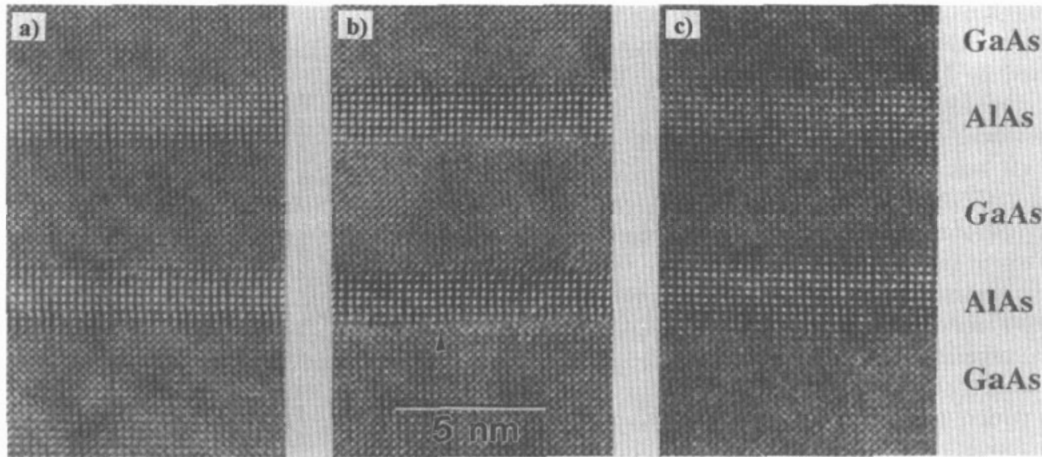

Figure 3. (100) high-resolution electron transmission images of AlAs double-barrier resonant tunnelling diodes in GaAs grown at different growth temperatures: (*a*) 480 °C, (*b*) 580 °C and (*c*) 680 °C.

as indicated by the arrow in figure 3(*b*). The lower AlAs barrier is on an average 1 ML thinner than the upper barrier. This difference in barrier thickness causes the slight asymmetry observed in the I–V curves of the diode. Similar effects were also found by Tsao *et al* [4], who investigated intentionally asymmetrical diodes.

Step distances of the 580 °C sample are generally in the range 10–20 nm for the normal interface. A slightly higher lateral step density is observed for the inverted interface while the chemical transitions between AlAs and GaAs are fairly abrupt. HRTEM consequently shows that the increase of the temperature from 480 to 580 °C results in an improvement of the lateral interface roughness. In contrast to photoluminescence experiments, where small step distances suggest smooth interfaces [5], scattering effects are relevant in resonant tunnelling diodes [6]. The scattering effect yields a sequential tunnelling current which affects the PVR. The improvement of the lateral interface roughness leads to reduced scattering in the diode and to higher PVRs, as shown in figure 1.

At high substrate temperatures ($T_s = 680$ °C) HRTEM shows a significant broadening of the AlAs barriers (figure 3(*c*)). On a larger scale (approximately 20 nm), the bottom interface of the lower AlAs barrier appears flat. The transition between the GaAs and the AlAs occurs within 2 to 3 MLs. In contrast, the diffusivity of the upper interface extends over at least 3 MLs. Lateral fluctuations can be observed on a scale of 5 to 10 nm. However, steps cannot be clearly localized. The thickness of the well is not sufficient to equalize the rough growth surface before the second AlAs barrier is grown, leading to a more diffuse bottom interface of the top barrier. A very broad transition is observed for the top interface of the top barrier. It can therefore be assumed that the barriers mainly consist of AlGaAs instead of pure AlAs. The effect that the normal interface becomes more diffuse for higher temperatures was also found by x-ray reflectivity measurements by Klemradt *et al* [7]. They found an increase in the diffusivity of the inverted interface in the temperature range 600–680 °C.

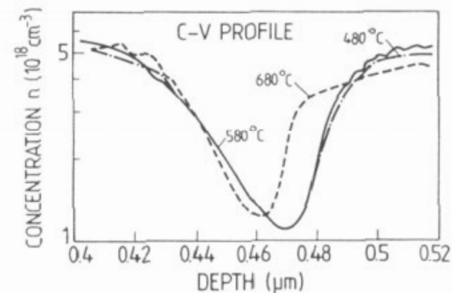

Figure 4. Electron concentration as a function of depth within the sample obtained from capacitance voltage measurements for AlAs/GaAs resonant tunnelling diodes grown at different growth temperatures.

The thicknesses of the two barriers differ only by a few MLs, which may explain the asymmetry in the temperature range 580–630 °C. The very strong increase in asymmetry above 630 °C (see figure 2) cannot be explained by the small difference in barrier thickness of the top and the bottom barrier of only some monolayers found in the HRTEM image (see figure 3). On the other hand it is known from the literature that Si segregation plays a dominant role for high growth temperatures [8, 9]. As shown in figure 4, capacitance–voltage measurements on samples grown at 480 and 580 °C gave almost identical results whereas a C–V profile of the sample grown at 680 °C exhibits a significantly smaller extension of the nominally undoped region (width of the dip in the C–V profile is more than 10 nm smaller). This suggests a segregation of the dopand material towards the growth direction. Although the absolute positions in C–V profiles in general are not very accurate the halfwidth of the dip in the C–V profiles are reproducible. This result suggests that the asymmetry observed in the I–V curves (figure 2) above 630 °C is caused by the Si segregation towards the surface.

In conclusion, a correlation between electrical and

structural properties of AlAs double-barrier resonant tunnelling diodes has shown that the PVRs of AlAs double-barrier resonant tunnelling diodes in GaAs are strongly affected by lateral interface roughness. In the temperature range 480–580 °C an improvement in the lateral step distances leads to an increase in the PVR. The highest PVR was achieved with samples grown at 580 °C (PVR = 5.35, current density = 6×10^4 A cm^{-2}). In this low temperature range no differences between normal and inverted interfaces were observed.

For higher substrate temperatures, the inverted interface appears more diffuse than the normal one. In addition, a broadening in the AlAs barriers was observed, indicating an AlGaAs rather than a pure AlAs barrier, which leads to a decrease of the PVR. Si-segregation towards the growth direction occurs for substrate temperatures above 630 °C and causes a strong asymmetry in the I–V curve of the diode with respect to the polarity of the peak voltage.

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