Barrier height enhancement of Schottky diodes on n-$In_{0.53}Ga_{0.47}As$ by cryogenic processing

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(Received 10 May 1993; accepted for publication 6 August 1993)

Schottky contacts on n-$In_{0.53}Ga_{0.47}As$ have been made by metal deposition on substrates cooled to a temperature of 77 K. The current-voltage and capacitance-voltage characteristics showed that the Schottky diodes formed at low temperature had a much improved barrier height compared to those formed at room temperature. The Schottky barrier height ϕ_B, was found to be increased from $\sim$0.2 to 0.60 eV with Ag metal. For the low temperature diode, the saturation current density, J_0, was about four orders smaller than for the room temperature diode. Deep level transient spectroscopy studies of n-InGaAs low temperature diodes exhibited one electron trap located at E_c-0.23 eV. This trap level was identified as a bulk trap.

The ternary alloy III-V compound semiconductor $In_{0.53}Ga_{0.47}As$ has a direct band gap with E_g=0.75 eV at room temperature and its lattice constant matches that of InP. n-$In_{0.53}Ga_{0.47}As$ has been widely used in high speed and optoelectronic devices because of its high electron mobility and high saturation velocity. It has been found, however, that the conventional Schottky barriers on n-InGaAs yield low barrier height (ϕ_B= $\sim$0.2 eV) hindering the realization of good Schottky devices. For this reason, several approaches have been made to enhance the Schottky barrier height on n-InGaAs using chemical passivation with sulfur, intentional surface oxidation, ion-implantation, and highly doped p^+-InGaAs interfacial layer, and use of a heterolayer such as InP.[1–5]

Recently, a cryogenic process to fabricate stable, high quality, and high barrier height Schottky contacts to n-InP has been developed.[6] This low temperature (LT=77 K) processing provided a simple way to greatly enhance the Schottky barrier height for Pd/n-InP up to 0.96 eV. The improvement in ϕ_B might be attributed to much more uniform metal atom coverage on the InP surface and reduced intermixing of metal, In and P. The phosphides formed at low temperature could also be considered as an insulator-like structure yielding a high barrier height.[7]

In this work, this low temperature deposition process is applied to improve Schottky barrier height on n-InGaAs Schottky diodes. Contacts formed at room temperature (RT=300 K) and low temperature are studied by current-voltage (I-V) and capacitance-voltage temperature (C-V-T) measurements to estimate the characteristic parameters in the LT diodes. Deep level transient spectroscopy (DLTS) studies were conducted on the simple metal/n-InGaAs(MS)LT diodes which were never previously reported due to the large leakage current of usual diodes.

Figure 1 shows the diode structure. The Schottky diodes used in this study were fabricated on 1.0 μm thick n-InGaAs epilayers with three different free-carrier concentrations of 1×10^{17} cm^{-3} (called S1 in this letter), 1×10^{16} cm^{-3} (S2), and 5×10^{15} cm^{-3} (S3) grown on an n^+-InP substrate. Samples S1 and S2 were grown at IBM by molecular beam epitaxy (MBE). Sample S3 was grown at Institut für Schicht -und Ionentechnik (ISI) by metalorganic vapor phase epitaxy (MOVPE). The diode fabrication consisted of three steps; i.e., ohmic contact on the back of the substrate, native oxide removal from the front of the InGaAs layer by chemical etching, and Schottky contact formation with the substrate cooled to low temperature. First, the samples were sequentially cleaned by trichloroethylene, acetone, methanol, and de-ionized water, and then blown dry with nitrogen gas. The ohmic contact was formed on an n^+-InP substrate by evaporating Au:Ge/Ni and alloying by rapid thermal annealing (RTA) at 360 °C for 10 s. A proximity cap was also used to protect the front surface during the annealing process. The native oxide on the front surface of the sample was then removed by wet chemical etch with H_2SO_4 solution (H_2SO_4:H_2O_2:H_2O=1:1:100) for 60 s. After the samples were rinsed in de-ionized water and blown dry with nitrogen gas, they were quickly loaded into an evaporator. Schottky metals Au or Ag, 1000 Å thick, were deposited on the n-InGaAs layers at a substrate temperature of 77 K under a high vacuum of 3×10^{-7} Torr. The low temperature was achieved by continuous liquid-nitrogen flow into

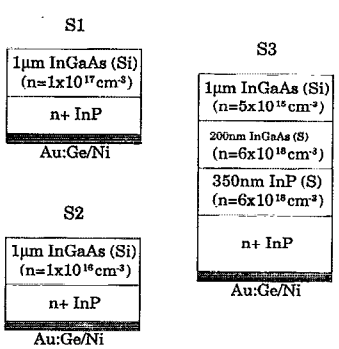

FIG. 1. Diode structures showing doping and thickness.

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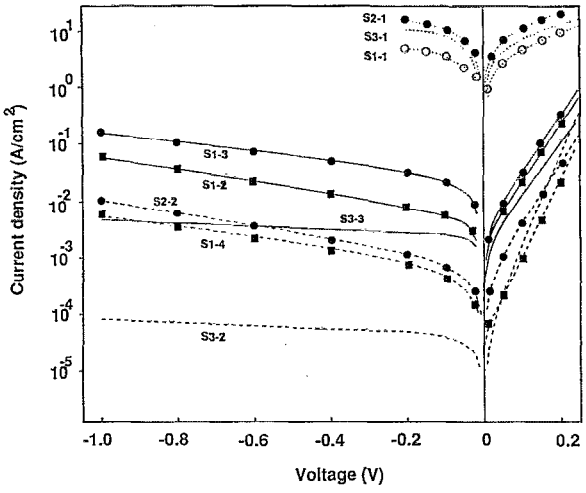

FIG. 2. *I-V* plots for metal/*n*-InGaAs diodes prepared at room and low temperature.

the sample holder and monitored with a chromel-alumel surface mounted thermocouple. Surface passivation using $P_2S_5/(NH_4)_2S$[1,8] was tried for some samples to examine whether the chemically passivated diodes with cryogenic processing can have good Schottky characteristics. For this sulfur passivation on *n*-InGaAs, the samples were immersed into $P_2S_5/(NH_4)_2S$ solution (0.03 g/ml) for 30 min right after acid etching. After the 0.8 mm^2 diodes were taken out, the surface was blown dry with nitrogen. The *I-V* and *C-V-T* characteristics of the diodes were measured from 100 to 300 K in an auto data acquisition cryogenic system. The DLTS measurements were performed in a Polaron DL4600 deep level spectrometer system with temperature from 100 to 380 K. The reverse bias was kept at -0.5 V while the filling pulse was changed from 0 to 0.4 V to distinguish the bulk and interface traps.[9]

Figure 2 and Table I show the room-temperature current-voltage (*I-V*) characteristics for RT and LT diodes. The device behavior is clearly dependent on the substrate temperature, the choice of metal, and free carrier density. For the RT diodes, the *I-V* characteristics look almost ohmic due to their low Schottky barrier height. For LT diodes, however, higher barrier heights, ϕ_B, calculated from Eq. (1) were obtained:

$$\phi_B=(kT/q)\ln(A^*T^2/J_0), \tag{1}$$

where $A^*=5.04$ A cm^{-2} K^{-2} is the Richardson constant of *n*-InGaAs, and J_0 is the saturation current density, determined from the *J*-axis intercept at $V=0$ of a straight line extension from the linear portion of forward *I-V* data. The ideality factor, *n*, was determined from the forward current characteristics using the relation

$$n=(q/kT)\left(\frac{\partial V}{\partial(\ln J)}\right). \tag{2}$$

For Au/*n*-InGaAs LT devices (S1-3), ϕ_B and *n* were found to be 0.47 eV and 1.50, respectively. For Ag/*n*-InGaAs devices (S1-2), ϕ_B and *n* were found to be 0.51 eV and 1.68, respectively. The high value of *n* may be due to an ultrathin amorphous layer at the interface to give MIS-like behavior. Compared with the RT diode, the reverse leakage current density of the LT diode was reduced by three orders. The reverse breakdown voltage of around 1.5–2.0 V was measured on both Au and Ag/InGaAs LT diodes. Ni, Cr, Pd, and Al were also tried as a barrier metal, but no big improvement of barrier height was observed. Chemically passivated Ag/InGaAs LT diodes (S1-4) showed ϕ_B of 0.55 eV and an ideality factor of 1.40. Even though those passivated LT diodes were found to be unstable during the test, compared with plain LT diodes, the reverse breakdown voltage was improved to 3.0 V and reverse leakage current was one order lower. The instability of the passivated LT diodes could be attributed to a sulfur crust on the surface of the InGaAs. In spite of the improved barrier height, all LT diodes fabricated on S1 showed high reverse leakage current due to relatively high doping density leading to a large tunneling component of reverse bias current.[10,11] Sample S2-2 showed similar forward *I-V* characteristics to S1-2. A small improvement of breakdown voltage V_{br} to -3 V and reverse current density at -1 V to 10^{-2} A cm^{-2} was observed. The best *I-V* characteristics were shown for Ag/*n*-InGaAs LT diodes fabricated on substrate S3. The barrier height ϕ_B and an ideality factor *n* for S3-2 were 0.60 eV and 1.16, respectively. The breakdown voltage V_{br} of S3-2 was also much improved to a value of more than -6 V. The reverse leakage current was greatly reduced and no soft reverse current characteristic was observed for this device. The current

TABLE I. A summary of electrical characteristics for RT and LT diodes.

Sample[a]	RT/LT	Metal	N_D (cm^{-3})	ϕ_B (eV)	*n*	V_{br} (V)	J_R at -1 V (A cm^{-2})
S1-1	RT	Au	1×10^{17}	...	...	...	...
S1-2	LT	Ag	1×10^{17}	0.51	1.68	1.5–2.0	6.2×10^{-2}
S1-3	LT	Au	1×10^{17}	0.47	1.50	1.5–2.0	1.5×10^{-1}
S1-4[b]	LT	Ag	1×10^{17}	0.55	1.40	~3.0	5.0×10^{-3}
S2-1	RT	Ag	1×10^{16}	...	...	...	-
S2-2	LT	Ag	1×10^{16}	0.54	1.57	~3.0	1.0×10^{-2}
S3-1	RT	Ag	5×10^{15}	...	...	...	...
S3-2	LT	Ag	5×10^{15}	0.60	1.16	~6.0	8.7×10^{-5}
S3-3	LT	Au	5×10^{15}	0.50	1.57	~3.0	5.0×10^{-3}

[a]Substrates S1 and S2 have an epitaxial layer grown directly on an InP substrate. Substrate S3 has buffer layers between InGaAs and InP substrate.
[b]A sulfur passivated LT diode.

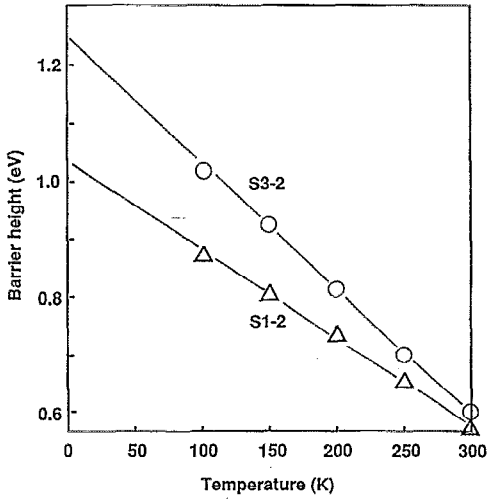

FIG. 3. Temperature dependence of zero-bias barrier heights for the Ag/InGaAs LT diodes (S1-2 and S3-2).

density difference at a reverse bias of -1 V between a RT diode (S3-1) and a LT diode (S3-1) was more than five orders. It is also interesting that for all LT diodes, Schottky barrier height and reverse current characteristics were better with Ag compared to Au.

The barrier heights from 1 MHz capacitance-voltage (C-V) measurement were in close agreement with those from I-V measurement, differing, in part, due to a difference in frequency between the two methods. The effective barrier height was calculated from

$$\phi_B = V_i + \xi + kT/q, \tag{3}$$

where V_i is the built-in potential, and ξ is the potential difference between the Fermi level and the conduction band edge. From Eq. (3), the Schottky barrier heights of Ag/InGaAs LT diodes S1-2 and S3-2 at 300 K were determined to be 0.56 and 0.60 eV, respectively. Capacitance-voltage-temperature (C-V-T) characteristics were also measured for S1-2 and S3-2 in the temperature range of 100–300 K. Good linearity was shown over the entire temperature range at reverse bias less than 1.5 V, and further confirms a high quality junction. Temperature dependence of zero bias barrier height ϕ_{B0} is described by

$$\phi_0 = \phi_0 + \beta T, \tag{4}$$

where ϕ_0 is the barrier height at zero temperature and zero bias, and β is the temperature coefficient of zero bias barrier height. the values of ϕ_{B0} versus temperature are shown in Fig. 3. The experimental values of ϕ_{B0} fit well to Eq. (4) with $\phi_0 = 1.03$ eV and $\beta = 1.53 \times 10^{-3}$ eV K^{-1} for S1-2, and $\phi_0 = 1.25$ eV and $\beta = 3.75 \times 10^{-3}$ eV K^{-1} for S3-2.

DLTS measurements were conducted on samples S3-2 and S3-3. Figure 4 shows a DLTS curve for sample S3-2 using -0.5 V reverse bias and 0.2 V filling pulse height. For the sample S3-2, one dominant peak was found in the temperature range of 100–380 K. This electron trap was located at E_c-0.230 eV. It had a trap density of 1.1×10^{14} cm^{-3} and a capture cross section of 1.58×10^{-19} cm^2. This trap can be identified as a bulk trap because its DLTS peak

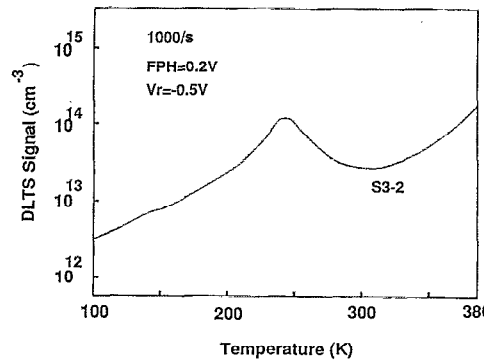

FIG. 4. A DLTS curve for the sample S3-2.

did not shift with change of the filling pulse height.[8] For sample S3-3, a similar DLTS feature was observed. The activation energy, trap density, and capture cross section of the electron trap were found to be 0.232 eV, 2.0×10^{15} cm^{-3}, and 2.13×10^{-19} cm^2, respectively. We could not obtain good DLTS data on the other samples due to high leakage current.

In conclusion, low temperature metal deposition provides a simple way to improve the Schottky barrier height on n-$In_{0.53}Ga_{0.47}As$. From I-V and C-V measurement, the LT diode with Ag metal exhibits an enhanced barrier height ϕ_B of 0.60 eV which is increased from $\sim$0.2 eV for the RT diode. This low temperature process also makes it possible to measure DLTS spectra. A bulk electron trap for LT diodes is found and its activation energy is ~ -0.23 eV. The improvement in ϕ_B and reverse leakage current with LT metal deposition could be attributed to the uniform metal coverage on the InGaAs surface and the formation of an amorphouslike structure instead of an alloy layer at the metal-semiconductor interface.

We acknowledge the assistance of Dick Pettit and Jerry Woodall from IBM for supplying MBE-grown samples and the financial support from the National Science Foundation, with Dr. Brain Clifton as Program Director.

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