CMOS Technology for SPAD / SiPM
Results from the MiSPiA Project


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OUTLINE

- Introduction

- MiSPiA CMOS FrontSPADs
  - Technology Issues
  - Thorough Characterization Results
  - Bench-Marking

- MiSPiA CMOS BackSPADs

- Conclusions
INTRODUCTION

SINGLE-PHOTON DETECTION APPLICATIONS:
- Time-resolved spectroscopy
- Fluorescence lifetime imaging
- Positron Emission Tomography
- Time-of-Flight ranging and 3D Imaging
- ...

DEMANDING REQUIREMENTS
- High Photon Detection Efficiency
- Low Noise (low DCR, Afterpulsing)
- Picosecond Timing Resolution, low quenching times
- Low Cross-Talk

Single photon counting with picosecond time-resolution!
INTRODUCTION

SINGLE-PHOTON AVALANCHE DIODEs (SPADs)

CMOS SPADs

✓ Cost-effective
✓ Good yield for mass production
✓ Suitable for arrays
✓ Good spatial resolution
✓ Quenching circuit, signal and data processing “on-chip”
✓ Good $t_{jitter}$
✓ Compatible with magnetic resonance imaging

✗ Small Fill-Factors for acceptable spatial resolutions
✗ High DCR
✗ High After-Pulsing

• Bias: ABOVE $V_{BR}$ (breakdown voltage)
• Geiger Mode: it’s a TRIGGER device!
• Opposite to APDs: GAIN is MEANINGSLESS!
MiSPiA CMOS FrontSPADs

2P4M 0.35µm CMOS Process Line at Fraunhofer IMS

8” Wafers
MiSPiA CMOS FrontSPADs

2P4M 0.35µm CMOS Process Line at Fraunhofer IMS

Can we use the standard CMOS process setup?

Too high $V_{br}$ → bad time jitters, high dark counts, and no isolation between neighbouring SPADs!
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10µm  20µm  30µm

0.35µm HV-CMOS PROCESSING
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0.35 µm CMOS SPAD Breakdown Voltage

SPAD test structures with diameters: 10 µm, 20 µm, 30 µm, 50 µm, 100 µm, 200 µm, and 500 µm

Temperature drift: 37.8 mV/°C

Temperature drift: 36.2 mV/°C

Source: F. Villa et al. “CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm”, J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

Uniformity over different shapes and areas: variation < 6% with respect to room temperature, no peripheral activation.
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SPAD Dark Count Rate

STATE-OF-THE-ART DARK COUNT RATE
- < 2 kcps @ 50 °C (Ø = 30 µm)
- < 50 cps @ room temp. (Ø = 30 µm)
- Negligible DCR @ low temperature

Acceptable DCR for large SPAD areas

Source: F. Villa et al. “CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm”, J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115
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SPAD Dark Count Rate

DCR vs T for SPADs with different diameters and excess biases between 4 V and 6 V.

DCR SPAD diameter dependence at room temperature (25°C) for excess biases between 4 V and 6 V.

Quadratic dependence

Higher order dependence

Source: F. Villa et al. “CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm”, J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115
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SPAD Dark Count Rate Cumulative Distribution Function

20 µm SPAD (64 x 32) 2048-pixel array

$t_{\text{HOLD}} = 300 \text{ ns}$

< 5% hot SPADs

VERY HIGH DCR UNIFORMITY!

Larger area SPADs show higher DCR and also more „hot“ pixels...

- 30 µm SPAD 64 x 32 pixel array
- 50 µm SPAD 32 x 1 pixel array
- 100 µm SPAD 32 x 16 pixel array
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Photon Detection Efficiency

First 20 µm SPAD test-structures measured at IMS

0.35 µm CMOS SPADs compared to:
• the state-of-the-art custom-process reach-through thick SPAD by Excelitas
• red-enhanced SPAD by Polimi and MPD
• planar silicon thin SPAD from MPD, and
• CMOS SPAD in 130 nm technology (MegaFrame Project, 2009)

30 µm SPAD pixels measured at POLIMI

6 V excess bias
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Uniformity of the photoactive area

Detection uniformity was measured by scanning the SPAD photoactive area with a laser spot with 2 µm and 6 µm steps.

20 µm SPAD (effective diameter without the guard-ring)

500 µm SPAD (effective diameter without the guard-ring)

\[
\epsilon_U = \frac{C_{\text{max}} - C_{\text{min}}}{C_{\text{eff}}} \times 100
\]

Source: F. Villa et al. “CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm”, J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115
**MiSPiA CMOS FrontSPADs**

**Afterpulsing Probability**

**LOW AFTERPULSING PROBABILITY**

- Negligible AP (< 1%) @ $T_{HOLD-OFF} > 50$ ns for SPAD areas up to 50 µm diameters
- Negligible AP (< 1%) @ $T_{HOLD-OFF} > 90$ ns for SPAD areas > 50µm diameters (150ns for 500µm)
- Maximum Count Rate = 50 Mcps

SPAD test structures with diameters: 10 µm, 20 µm, 30 µm, 50 µm, 100 µm, 200 µm, and 500 µm

*Source: F. Villa et al. “CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm”, J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115*
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Timing Response

GOOD TIMING RESPONSE
• FWHM < 100 ps (Ø = 10 µm)
• FWHM < 140 ps (Ø = 20 - 30 µm)
• Reduced variations among big devices (%σ_{FWHM} < 3)
• Small wavelength influence (%Δ_{FWHM} < 5)
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Timing Response

Results obtained using the on-chip integrated quenching circuit with tunable hold-off time and reduced electronics.
Photon timing response of a 500 µm SPAD at different radial positions of the illumination spot (ρ) from 0 µm (SPAD centre) to 250 µm (periphery of the SPAD photoactive area).

Photon timing response vs. radial position of the illumination spot (expressed in % of the radius length).
### MiSPiA CMOS FrontSPADs

A bit of SPAD Bench-Marking, just to see where we are…

<table>
<thead>
<tr>
<th>SPAD Technology</th>
<th>PDE [%]</th>
<th>DCR/area @ 25°C [cps/µm²]</th>
<th>Time-Jitter, FWHM [ps]</th>
<th>SPAD Photoactive Area Diameter [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>λ = 400nm</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>λ = 850nm</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>This work [1]</td>
<td>45</td>
<td>4.5</td>
<td>0.055</td>
<td>40 (AP &lt; 1%)</td>
</tr>
<tr>
<td>0.35 µm CMOS planar silicon thin SPAD (not this technology) from MPD [3]</td>
<td>25</td>
<td>4.5</td>
<td>3.979</td>
<td>600 (AP &lt; 1%)</td>
</tr>
<tr>
<td>CMOS SPAD in 130 nm technology (MegaFrame Project, 2009) [4]</td>
<td>14</td>
<td>6</td>
<td>0.249</td>
<td>100 (AP &lt; 0.02%)</td>
</tr>
<tr>
<td>CMOS SPAD in 90 nm technology (SPADNet Project, 2012) [5]</td>
<td>17</td>
<td>21</td>
<td>3.466</td>
<td>15 (AP &lt; 0.375%)</td>
</tr>
</tbody>
</table>

**Notes:**

# MiSPiA CMOS FrontSPADs

A hypothetical SiPM Bench-Marking, just to see where we are...

<table>
<thead>
<tr>
<th>SPAD Technology</th>
<th>PDE [%]</th>
<th>DCR/area @ 25°C [cps/μm²]</th>
<th>T(_{\text{HOLD-OFF}}) [ns]</th>
<th>Time-Jitter, FWHM [ps]</th>
<th>SPAD Photoactive Area Diameter [μm], cell-size [μm²], and FF [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>This work [1]</strong></td>
<td>45</td>
<td>53 (470 nm)</td>
<td>4.5</td>
<td>0.055</td>
<td>40 (AP &lt; 1%)</td>
</tr>
<tr>
<td><strong>HAMAMATSU Multi-Pixel Photon-Counter (MPPC)</strong> Series S10985 [3]</td>
<td>40</td>
<td>50 (440 nm)</td>
<td>-7</td>
<td>n.a.</td>
<td>-22 (cell size: 50 μm x 50 μm, FF = 61.5 %)</td>
</tr>
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</table>

This work [1] 45 53 (470 nm) 4.5 0.055 40 (AP < 1%) 85


HAMAMATSU Multi-Pixel Photon-Counter (MPPC) Series S10985 [3]


[3] [http://www.hamamatsu.com/resources/pdf/ssd/s10984_series_etc_kapd1024e03.pdf](http://www.hamamatsu.com/resources/pdf/ssd/s10984_series_etc_kapd1024e03.pdf)
MiSPiA CMOS BackSPADs

Schematic representation of the BackSPAD process flow and back-side thinning

Bonding of the top SOI SPAD over the bottom CMOS electronic pixel, through the Metal4 interconnect bonding layer
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Process simulation of a cross-section of the SOI BackSPAD wafer

Fully-Depleted (HV) BackSPADs

Partially-Depleted (LV) BackSPADs
MiSPiA CMOS BackSPADs

**State-of-the-Art MiSPiA FrontSPAD DCR:**

![Graph showing DCR vs. SPAD diameter](image)

For approx. 100 µm BackSPAD diameter:

\[
\text{DCR}_{\text{BackSPAD}} \approx 40 \times \text{DCR}_{\text{FrontSPAD}}
\]

**For 150 µm FrontSPAD pixels with 30 µm SPAD diameter**

- \( \text{DCR}_{\text{FrontSPAD}} \approx 100 \text{ cps with a Fill-Factor of } 3.14\% \)

**Equivalent 150 µm BackSPAD pixels with 143 µm SPAD diameter**

- \( \text{DCR}_{\text{BackSPAD}} \approx 240 \text{ kcps with a Fill-Factor of } 71.4\% \)

A trade-off must be met between the BackSPAD DCR and the photoactive area!
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**Wafer-bonding of the BackSPAD SOI/CMOS array chips**

- Wafer without seal ring after back grinding
- Wafer with seal ring after back grinding
- Wafer with seal ring after reduced back grinding and dry etching
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Wafer-bonding of the BackSPAD SOI/CMOS array chips

Pads and SPADs on wafer bonded BackSPADs

Cross section of SOI wafer after waferbonding and backthinning

4 µm thick Si/SiO2 film
CONCLUSIONS

- The MiSPiA FrontSPADs deliver:
  - the lowest DCR reached so far in CMOS technologies
  - high UV-PDE due to the special UV-transparent Silicon-Nitride based passivation layer

- BackSPADs are based on a standard SOI-CMOS technology, the ROIC is developed in the standard 0.35 µm CMOS technology

- The measured DCR are higher than those measured in FrontSPADs, but still in the expected range of state-of-the-art CMOS SPADs (kcps)

- The presence of deep trench isolation minimizes cross-talk issues, drastically decreases the minimum distance between adjacent SPAD structures (7µm), and does not increase the DCRs for distances above 1 µm to the BackSPAD device area

- The developed technology is suitable also for SiPM developments, where further optimization of the fill-factors should be addressed
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