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Integration of perovskite oxide dielectrics into complementary metal–oxide–semiconductor capacitor structures using amorphous TaSiN as oxygen diffusion barrier

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The high permittivity perovskite oxides have been intensively investigated for their possible application as dielectric materials for stacked capacitors in dynamic random access memory circuits. For the integration of such oxide materials into the CMOS world, a conductive diffusion barrier is indispensable. An optimized stack p^{++}-Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir was developed and used as the bottom electrode for the oxide dielectric. The amorphous TaSiN film as oxygen diffusion barrier showed excellent conductive properties and a good thermal stability up to 700 °C in oxygen ambient. The additional protective iridium layer improved the surface roughness after annealing. A 100-nm-thick (Ba,Sr)TiO_3 film was deposited using pulsed laser deposition at 550 °C, showing very promising properties for application; the maximum relative dielectric constant at zero field is $\kappa \approx 470$, and the leakage current density is below 10^{-6} A/cm^2 for fields lower then ± 200 kV/cm, corresponding to an applied voltage of ± 2 V. © *2011 American Institute of Physics*.
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I. INTRODUCTION

High-κ materials with perovskite structure have been widely investigated for possible application as future dielectrics for the stacked capacitors in dynamic random access memory (DRAM) circuits.[1–3] High-κ materials on conductive silicon have another possible application in bioelectronics for capacitive stimulation of nerve cells for the investigation of the interaction between chip-based circuits and living cells.[4,5]

The oxygen diffusion through the bottom electrode (BE) into the silicon plug during the deposition of perovskite oxide dielectrics or their post-deposition annealing in oxygen atmosphere at temperatures in the range 500–700 °C have to be prevented.[6–8] This unwanted reaction leads to the formation of silicon dioxide with much lower dielectric constant in series with the high-κ material, leading to an unacceptable decrease of the stack capacitance.

The introduction of a conductive diffusion barrier between the BE and silicon plug should prevent the oxygen diffusion through the BE. The most promising candidate is $Ta_xSi_yN_z$ (TaSiN in the following) amorphous film, which has also been considered for use in a copper metallization scheme as a conductive diffusion barrier. The lack of fast diffusion paths and high crystallization temperatures makes it suitable for application as an oxygen diffusion barrier in stacked capacitor DRAM structures with perovskite oxide materials.[9–12]

II. EXPERIMENTAL PROCEDURES

The (100) p-type silicon wafer with a boron doping density of $N_a = 10^{20}$ cm^{-3} was the substrate for all experiments. The thin film stack used as the bottom electrode consists of one intermediate platinum layer, the conductive diffusion barrier TaSiN, and an upper platinum or iridium layer (Si/Pt/TaSiN/Pt or Si/Pt/TaSiN/Ir). The following notation was used in the text: Adjacent layers are presented with a separation by slash (e.g., Si/Pt/TaSiN/Pt), where the film most to the right is uppermost on the sample. The atomic percentage of elements is given in subscripts (e.g., $Ta_{21}Si_{57}N_{21}$).

$Ta_{21}Si_{57}N_{21}(Ar_1)$ thin film was deposited using reactive radio frequency (rf) magnetron sputtering in a high vacuum system Leybold Univex 450 C with a $TaSi_{2.7}$ target. The target was 4" in diameter and 4 mm thick. The vacuum system base pressure was 7×10^{-7} mbar, and the total gas pressure during the sputtering was 10^{-2} mbar. The total gas flow (60 sccm), as well as the ratio of argon to nitrogen was kept constant during sputtering (54 sccm Ar plus 6 sccm (Ar/1% N_2)). The films were deposited at room temperature without any additional substrate heating. The cathode power was 240 W. Properties of different TaSiN thin films, depending on deposition parameters, have been investigated,[13] but their description is beyond the scope of this paper.

Platinum and iridium films of BE were deposited using DC magnetron sputtering. The sputter gas was argon and the target power was 375 W. Without interrupting the vacuum, TaSiN thin film was deposited onto the platinum layer using standard parameters. Prior to deposition of TaSiN or platinum layers on the p^{++}-silicon substrate, the native SiO_2 was removed by etching the substrate with 40% hydrofluoric acid.

The dielectric material used for this investigation is 100-nm-thick ($Ba_{0.7}$,$Sr_{0.3}$)TiO_3 (BST) deposited by pulsed laser deposition (PLD) at 550 °C. The oxygen partial pressure was 0.25 mbar, the repetition rate 10 Hz, and the laser energy 100 mJ. For comparative purposes, platinized silicon

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wafers were used as the reference BE (Si/SiO_2/10 nm TiO_x adhesion layer/100 nm Pt). The platinum top electrodes layers for electric measurements were deposited by e-beam evaporation and structured by a lift-off process.

The different as-deposited stacks were characterized using a 4-point probe to obtain the resistance and atomic force microscopy (AFM) to determine the surface roughness. Rutherford backscattering spectroscopy (RBS) was used for the depth profiling of the different stacks. The capacitance of the dielectric layer in the different capacitor stacks was measured with a precision LCR meter HP 4284 A from Hewlett Packard at 1 kHz. Leakage current measurement was performed using a voltage source Burster 4462 and a Keithley 617 electrometer (bottom electrode was grounded).

III. RESULTS AND DISCUSSION

An optimized thin film stack as BE for the capacitor structure was developed. The base is a highly doped, conducting silicon wafer (p^{++}-Si). The amorphous $Ta_{21}Si_{57}N_{21}$ thin film was used as a conductive oxygen diffusion barrier in order to protect the silicon substrate from oxidation during the deposition of the dielectric material. The resistivity of as-deposited $Ta_{21}Si_{57}N_{21}$ film is 1.5×10^{-5} Ωm, and it hardly changes after annealing in an oxygen atmosphere at 700 °C (1.4×10^{-5} Ωm).[13] The $Ta_{21}Si_{57}N_{21}$ film is amorphous after deposition and remains amorphous up to 700 °C. A polycrystalline hexagonal $TaSi_2$ crystal phase is formed after annealing at 750 °C, as indicated in the XRD diagram (Fig. 1(a)).

Already, after sputter deposition at nominally room temperature, the junction $Si/Ta_{21}Si_{57}N_{21}$ develops a high contact resistance of 57 Ω. The RBS data for the $Si/Ta_{21}Si_{57}N_{21}$ junction after annealing at 700 °C are depicted in Fig. 1(b). No additional oxide layer could be detected between the silicon substrate and $Ta_{21}Si_{57}N_{21}$ layer (see inset in Fig. 1(b)), which means that the high resistance layer at the interface is thinner than the RBS resolution of about 5 nm. The stack behavior is improved after introducing an intermediate platinum layer. After deposition, the stack $Si/Pt/Ta_{21}Si_{57}N_{21}$ has the same resistance as the thick silicon substrate (0.13 Ω). The resistance does not change after annealing in an oxygen atmosphere at 700 °C, and the rms value of the top TaSiN layer is < 0.7 nm.

It was reported that the BST film does not crystallize well on the TaSiN surface.[14] In order to avoid the direct contact of the BST film to the TaSiN layer, an additional layer was introduced. A platinum or iridium upper layer was sputtered on the $Ta_{21}Si_{57}N_{21}$ without breaking the vacuum, so that the diffusion barrier lies in between two thin metal films. The resistances of these as-deposited stacks $Si/Pt/Ta_{21}Si_{57}N_{21}/Pt$ or $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir$ show ohmic behavior and are identical to that of the Si wafer, indicating that the layer- and contact-resistances on top are negligible. The deposited Ir thin film is smoother ($rms = 0.54$ nm) than the Pt layer ($rms = 2.0$ nm). After annealing in an oxygen atmosphere, the resistance and the roughness increase. Only the stack with Ir upper layer is stable up to 550 °C, and its roughness has an acceptable value (1.05 nm), while the stack with a Pt upper layer shows degraded values. All the data are summarized in Table I.

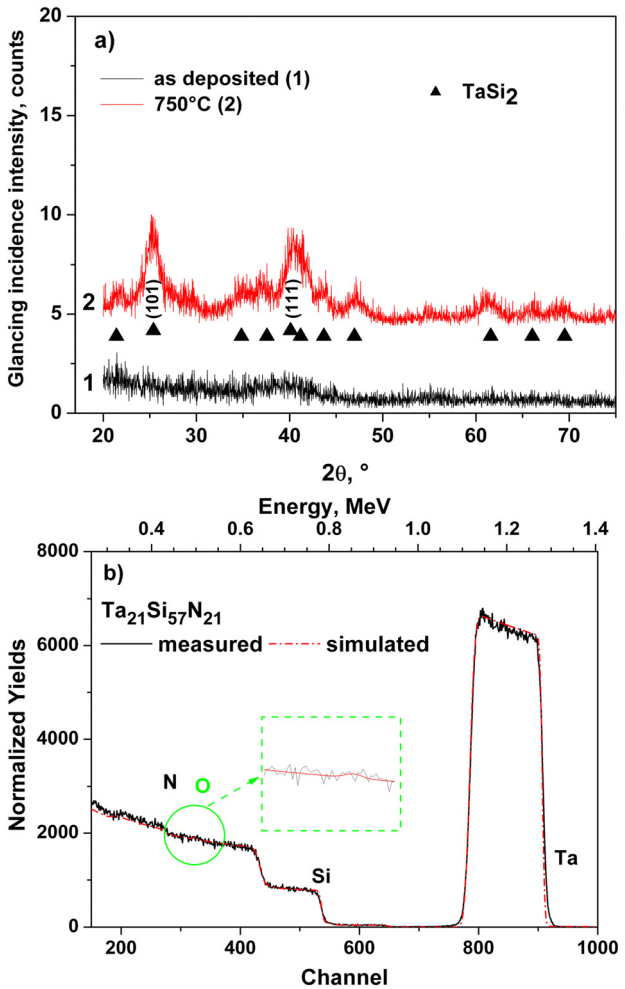

FIG. 1. (Color online) (a) XRD diagram with glancing incident geometry for TaSiN film on silicon after deposition and after annealing at 750 °C in oxygen. (b) RBS data for $Ta_{21}Si_{57}N_{21}$ on silicon substrate after annealing at 700 °C in oxygen.

RBS diagrams of the $Si/Pt/Ta_{21}Si_{57}N_{21}/Pt$ stack in the state "as-deposited" and after annealing at high temperatures in oxygen are presented in Fig. 2(a). The increasing reaction of the upper platinum layer with $Ta_{21}Si_{57}N_{21}$ after baking can be seen. The intermediate platinum layer was totally consumed and converted into Pt_xSi already at 500 °C. The

TABLE I. Roughness and resistance of $Si/Pt/Ta_{21}Si_{57}N_{21}$ stacks with Pt or Ir upper electrode "as-deposited" and after rapid thermal annealing (RTA) for 10 min in an oxygen atmosphere at the indicated temperatures.

Upper layer		As-deposited	500 °C	600 °C	700 °C
Pt	rms, nm	1.99	10.2	11.9	12.5
	R, Ω	0.11	0.20	0.20	0.80
Ir	rms, nm	0.54	0.95	9.58	25.6
	R, Ω	0.11	0.11	1.35	1.72

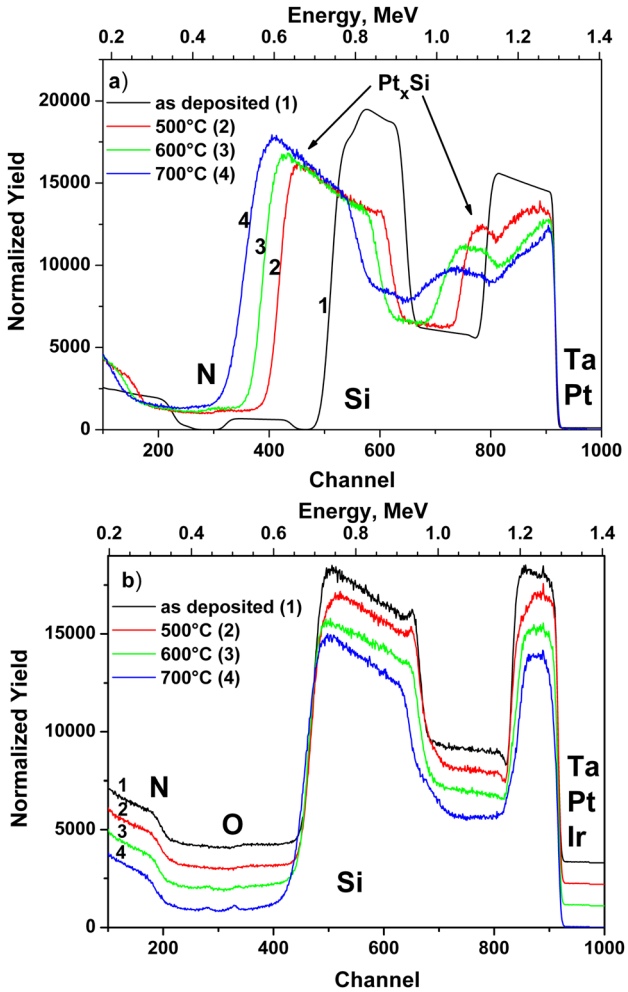

FIG. 2. (Color online) RBS for (a) Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt and (b) Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stacks after deposition and after annealing at different temperatures in an oxygen atmosphere.

Pt_xSi from the upper layer intermixes with TaSiN at temperatures above 600 °C. Since the silicide layer is too thick, resulting in an overlap of the silicon and the oxygen signals ($E_O = 0.51$ MeV and $E_N = 0.44$ MeV), the oxygen could not be properly detected.

In the RBS spectra of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack (Fig. 2(b)), it is noticeable that the reactivity of iridium to $Ta_{21}Si_{57}N_{21}$ is not as pronounced as in the case of platinum. The RBS analysis identified an oxygen containing layer on the top of the iridium and at the interface $Ta_{21}Si_{57}N_{21}$ to iridium after annealing at 600 °C and 700 °C, which may lead to an increase in the resistance.

As the Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack showed promising properties up to 550 °C, a BST layer was deposited using PLD. The scheme of the new stack is presented in Fig. 3. In order to measure the whole stack, the bottom side of the p^{++}Si substrate was etched and then coated with 100-nm-thick platinum layer and fixed with silver paste on a copper plate, which served as BE.

The relative permittivity of the BST thin film in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt capacitor structure is $\kappa \sim 470$ at the maximum (Fig. 4). There is no difference using the different

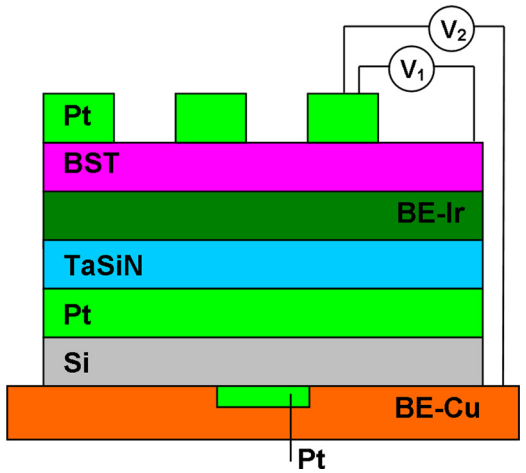

FIG. 3. (Color online) Scheme of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/$Pt_{(top)}$ stack used for electric characterization (not to scale).

BEs, iridium (V_1), or copper (V_2). The permittivity–electric field dependence has a slightly butterfly-like shape, possibly indicating some ferroelectricity in the thin BST film. The permittivity is largely tunable.

The leakage current dependence on the electric field was measured by applying the voltage in 0.1 V steps. After applying the voltage, the current was recorded for 300 s to measure the "true" leakage current without contributions of relaxation or degradation, as shown in Fig. 5(a). Then, the sample was first depolarized ($V = 0$) for 300 s and the next voltage step was applied. The leakage current density-electric field characteristic ($log\ j - E$) of the capacitor system Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/$Pt_{(top)}$, for which the top electrode was platinum and the bottom electrode the highly doped p^{++}-silicon, connected to a copper plate, is shown in Fig. 5(b). In the range of the applied electric field from 50 kVcm^{-1} up to 200 kVcm^{-1}, the current density increases slowly and is lower than 1×10^{-6} Acm^{-2}. With larger electric fields, the leakage current density increases more steeply.

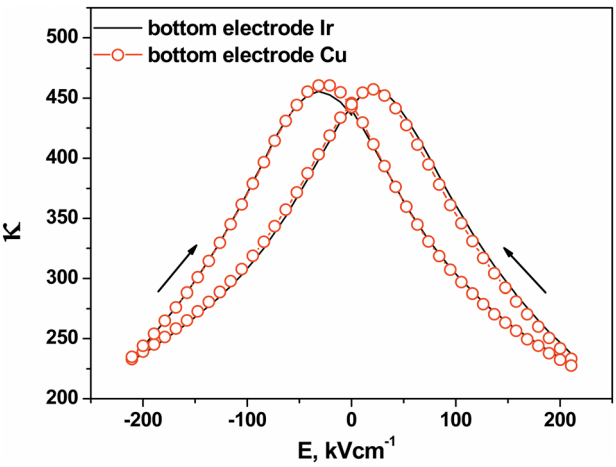

FIG. 4. (Color online) Relative permittivity of BST thin film in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/$Pt_{(top)}$ stack vs applied electric field.

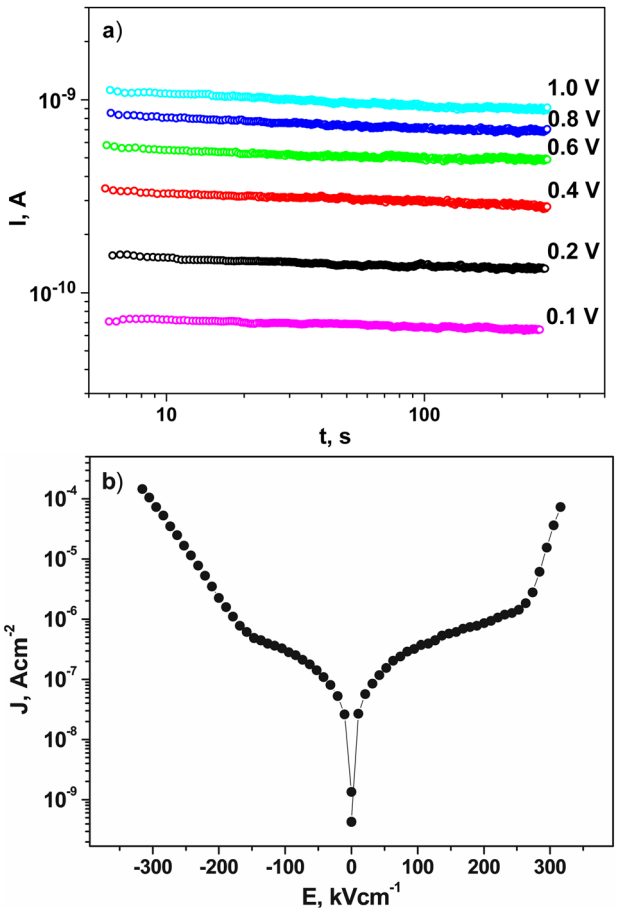

FIG. 5. (Color online) (a) Current response upon voltage step stimulation and (b) leakage current density vs applied electric field for BST thin film in the $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir/BST/Pt_{(top)}$ stack.

IV. CONCLUSIONS

An optimized conductive film stack on a p^{++} silicon wafer including a conductive and stable oxygen diffusion barrier was developed for the application as the bottom electrode in stacked capacitors with perovskite oxide dielectrics for integration into CMOS chips. The more simple junction $Si/Ta_{21}Si_{57}N_{21}$ develops an unacceptable high contact resistance. Improved behavior was achieved using an intermediate platinum layer. The stack $Si/Pt/Ta_{21}Si_{57}N_{21}$ has good thermal stability, conductive properties, and a smooth surface after annealing at 700 °C in an oxygen atmosphere. Although the properties of as-deposited p^{++}-$Si/Pt/Ta_{21}Si_{57}N_{21}/Pt$ are very promising concerning the resistance and roughness, the stack failed after processing at temperatures above 500 °C due to an unacceptable increase of roughness and resistance. The introduction of the top iridium layer improves the thermal properties of the p^{++}-$Si/Pt/Ta_{21}Si_{57}N_{21}/Ir$ stack, which is stable up to 550 °C with acceptable roughness. BST thin film, deposited by PLD at 550 °C on the BE stack p^{++}-$Si/Pt/Ta_{21}Si_{57}N_{21}/Ir$, shows a high relative dielectric constant at zero field, $\kappa \sim 470$. The leakage current density of BST thin film is below $j = 10^{-6}$ A/cm^2 for fields lower than ± 200 kV/cm, corresponding to an applied voltage of ± 2 V. Thus, such a stack is suitable for DRAM applications within the CMOS world.

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