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Ambipolar charge transport in microcrystalline silicon thin-film transistors

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Hydrogenated microcrystalline silicon (μc-Si:H) is a promising candidate for thin-film transistors (TFTs) in large-area electronics due to high electron and hole charge carrier mobilities. We report on ambipolar TFTs based on μc-Si:H prepared by plasma-enhanced chemical vapor deposition at temperatures compatible with flexible substrates. Electrons and holes are directly injected into the μc-Si:H channel via chromium drain and source contacts. The TFTs exhibit electron and hole charge carrier mobilities of 30–50 $cm^2/V\,s$ and 10–15 $cm^2/V\,s$, respectively. In this work, the electrical characteristics of the ambipolar μc-Si:H TFTs are described by a simple analytical model that takes the ambipolar charge transport into account. The analytical expressions are used to model the transfer curves, the potential and the net surface charge along the channel of the TFTs. The electrical model provides insights into the electronic transport of ambipolar μc-Si:H TFTs.
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I. INTRODUCTION

Thin-film transistors (TFTs) are key elements for large-area electronic applications. To date, TFTs based on amorphous silicon (a-Si:H) are commonly used as pixel switches for display backplanes.[1] However, the realization of more complicated driver circuitry is not possible due to low charge carrier mobility and device instability of a-Si:H.[1–4] So far external drivers are needed or the circuitry has to be realized by polycrystalline silicon (poly-Si) TFTs with high charge carrier mobilities and stable threshold voltages.[5] However, the manufacturing cost of poly-Si TFTs is higher due to high processing temperatures.[5,6]

Hydrogenated nanocrystalline or microcrystalline silicon (nc-Si:H or μc-Si:H) is a promising alternative to existing technologies due to its high electron and hole charge carrier mobilities.[7–9] Microcrystalline silicon consists of amorphous phases, silicon crystallites and voids, and is usually deposited at low temperature by plasma-enhanced chemical vapor deposition (PECVD) using a high hydrogen dilution.[10] The high electron and hole charge carrier mobilities in μc-Si:H facilitate the realization of integrated thin-film circuits such as shift register or line and row multiplexers. However, the realization of complementary metal-oxide-semiconductor (CMOS) based integrated circuits requires complex processing of the thin-film devices. Alternative solutions based on ambipolar circuits have been proposed, which simplify the device fabrication.[11]

In this study, ambipolar TFTs were realized based on μc-Si:H. The transistors were prepared by PECVD at temperatures up to 160 °C. Electrons and holes are directly injected into the μc-Si:H channel via chromium drain and source contacts. No highly doped n- or p-layers were inserted between the metal contacts and the channel layer. The device fabrication will be described in Sec. II of the manuscript. The electrical characterization of the ambipolar TFTs will be presented in Sec. III. Section IV is divided into two parts. In Sec. IV A a simple analytical model will be presented that describes the electrical characteristics of unipolar μc-Si:H TFTs. The analytical model allows for describing the potential and the net surface charge along the channel, as well as the transfer curves of the unipolar μc-Si:H transistors. In Sec. IV B the model is extended to describe the potential and the net surface charge along the channel, as well as the transfer curves of ambipolar μc-Si:H transistors. The results will be discussed in Sec. V, before the study is summarized in Sec. VI.

II. DEVICE FABRICATION

The microcrystalline silicon thin film transistors were fabricated on borosilicate glass substrates. The drain and source contacts of the ambipolar μc-Si:H TFTs were realized by chromium (Cr) with a thickness of 30 nm. Chromium exhibits a work function of 4.5 eV, which allows for the efficient injection of electrons and holes in the μc-Si:H film [Fig. 1(a)]. The channel material was formed by an intrinsic microcrystalline silicon (i-μc-Si:H) film with a thickness of 100 nm. The thickness of the channel layer was chosen to be 100 nm to attain a compromise between a high quality μc-Si:H (Refs. 10 and 12) and a low series resistance between the drain/source contacts and the charge carrier accumulation region.[13] The i-μc-Si:H channel layer was deposited by PECVD at a deposition temperature of 160 °C and plasma excitation frequency of 13.56 MHz, in the high pressure (1330 Pa) and high power ($0.3\ W/cm^2$) regime, which facilitates the deposition of material at high deposition rates

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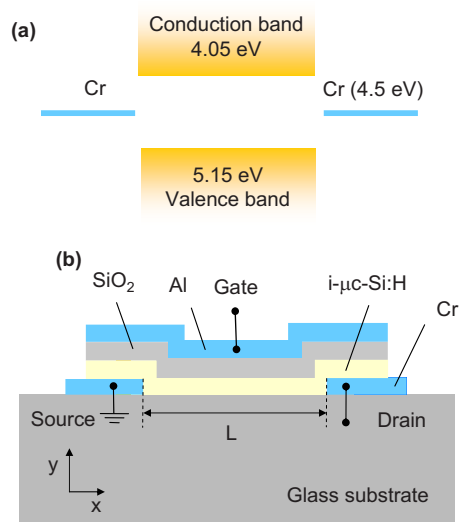

FIG. 1. (Color online) Schematic cross-section of a top-gate staggered ambipolar microcrystalline silicon thin film transistor (b) and electron affinity of silicon and the drain and source electrodes (chromium) (a).

of up to 25 nm/min.[14,15] The μc-Si:H channel layer was prepared in the transition to amorphous growth regime to ensure high device performance.[16,17]

Following the deposition of the i-μc-Si:H channel layer, a gate dielectric (silicon oxide, SiO_2) of 300 nm was prepared by PECVD at 150 °C. Finally, the gate metal electrode was formed by aluminum (Al) film with a thickness of 100 nm. The schematic cross-section of the ambipolar μc-Si:H TFT is depicted in Fig. 1(b).

III. EXPERIMENTAL RESULTS

The transfer characteristics of an ambipolar μc-Si:H TFT with a channel length, L, of 20 μm and a channel width, W, of 1000 μm are shown in Figs. 2(a) and 2(b). The n-channel transfer characteristics [Fig. 2(a)] were measured for drain voltages, V_D, of 0.1, 1, 3, and 5 V. The linear ($V_D \leq 1$ V) and saturation ($V_D > 1$ V) operational region can be clearly distinguished from the measured transfer curves. An electron charge carrier mobility of 52 $cm^2/V\,s$ and a threshold voltage of 1.85 V were extracted from the n-channel transfer characteristics of the ambipolar TFT. The transistor exhibits a subthreshold slope of 0.5 V/decade.

The p-channel transfer characteristic of the ambipolar μc-Si:H TFT is shown in Fig. 2(b), for drain voltages, V_D, of 1, 3, and 5 V. For the p-channel operation, the ambipolar TFT exhibits a hole charge carrier mobility of 8 $cm^2/V\,s$

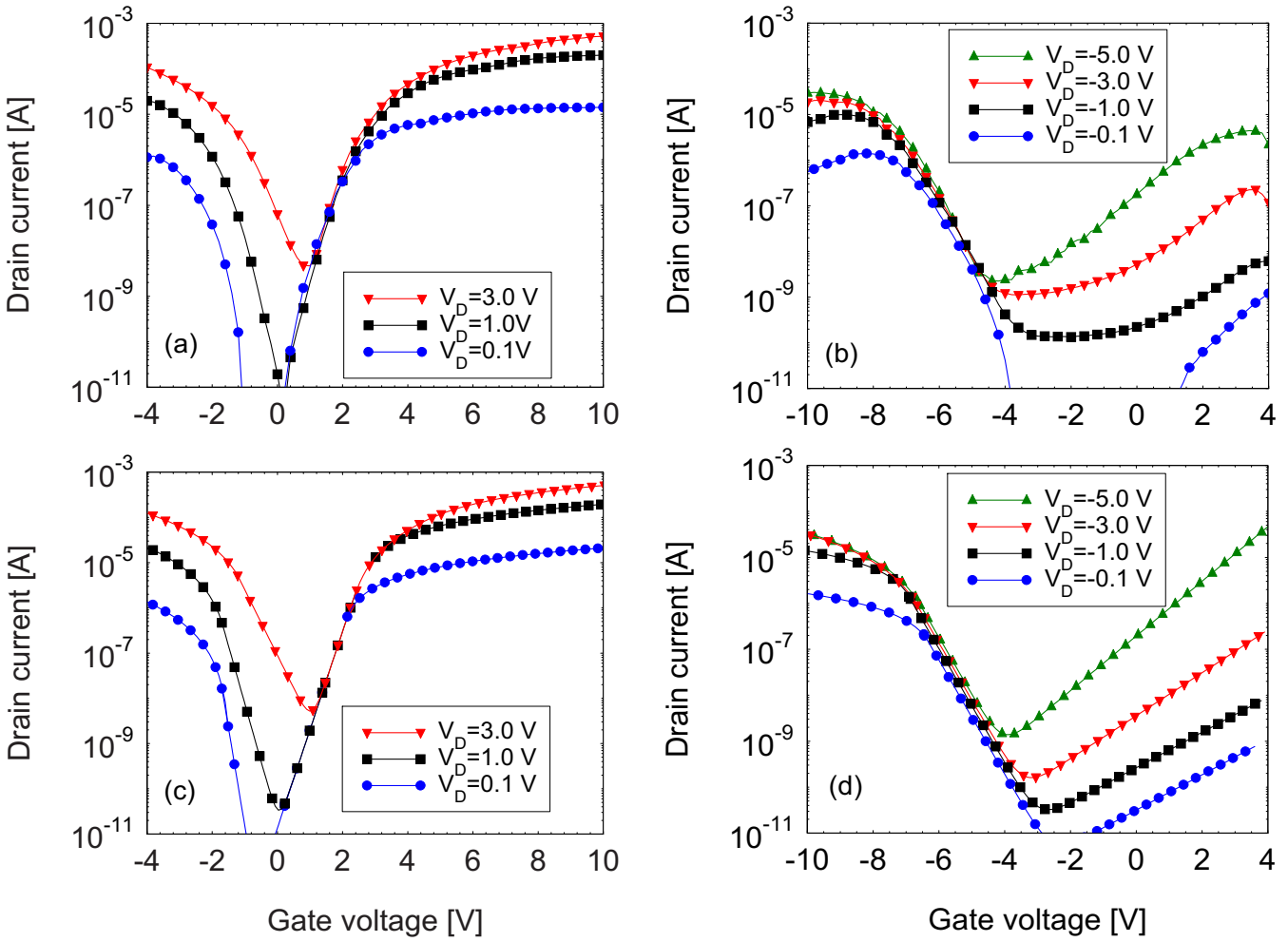

FIG. 2. (Color online) Measured [(a) and (b)] and fitted [(c) and (d)] transfer characteristics of n-channel [(a) and (c)] and p-channel [(b) and (d)] ambipolar μc-Si:H TFTs with a channel width, W, of 1000 μm and a channel length, L, of 20 μm.

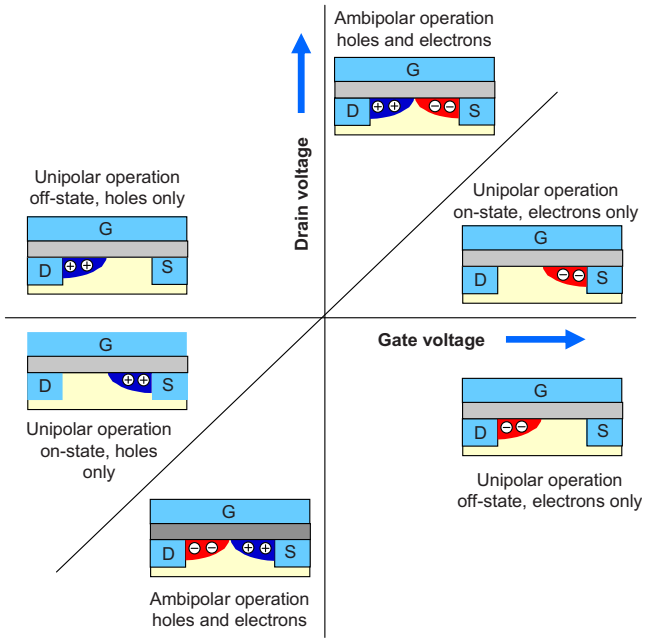

FIG. 3. (Color online) Different operation modes of μc-Si:H TFTs depending on the applied bias voltage.

and a threshold voltage of −5.7 V. The TFT exhibits a subthreshold slope of 0.7 V/decade. The simulated transfer characteristics in Figs. 2(c) and 2(d) will be described in Sec. V.

Ambipolar TFTs with high drain currents in the electron- and hole-dominated transport regime can only be realized if electrons and holes are effectively injected in the μc-Si:H channel. Both electrons and holes contribute to the device characteristics under ambipolar operation. Depending on the applied drain voltage and gate voltage, either electrons, holes, or both types of charge carriers may determine the electrical characteristics. The different modes of operation are illustrated in Fig. 3 as a function of the gate and the drain voltages. For small positive drain voltages and positive gate voltage the TFT operates like an n-type unipolar transistor. Electrons are injected from the source electrode into the channel of the transistor. For positive gate voltages the transistor is turned on, whereas for negative gate voltages the transistor is turned off and holes are injected from the drain electrode of the transistor. For larger positive drain voltages and positive gate voltages the transistor behaves like an ambipolar transistor. Electrons are injected from the source while holes are injected from the drain electrode. As a result electron and holes are accumulated in the channel. Depending on the applied voltages, the charge carrier mobilities for the electrons and the holes, and the threshold voltage, a recombination point is observed.

In order to describe the charge and potential distributions along the channel a simple analytical model was developed.

IV. MODEL OF UNIPOLAR AND AMBIPOLAR TFTS

The field-effect transistor is described by a simple charge-sheet model, which was proposed for the fist time by Shockley in 1952 (Ref. 18) and later extended by Brews in 1978 and Van de Wiele in 1979.[19,20] In this simple model the field-effect transistor is treated as a plate capacitor. All charges are assumed to be immediately at the interface of the dielectric so that the thickness of the accumulation layer is zero. This assumption implies that no band bending exists across the charge-sheet, which results in an error of this model. However, we will accept this small error at the expense of gaining a better insight into the device operation and the charge transport. The transistor can be described by an equivalent circuit, which is shown in Fig. 4. The equivalent circuit just consists of resistors and capacitors. The resistors, r(x)dx, and capacitors, C_G, are differential resistance elements and capacitance elements along the channel, respectively. The resistors R_{CS} and R_{CD} represent the drain and source contact resistances of the transistor. The voltages, V(x), and, V(x+dx), are the potential along the channel. We will first introduce the basic expressions for the charge and potential distributions long the channel for a unipolar TFT.[18] In the second step the model will be extended to describe the behavior of an ambipolar TFT.

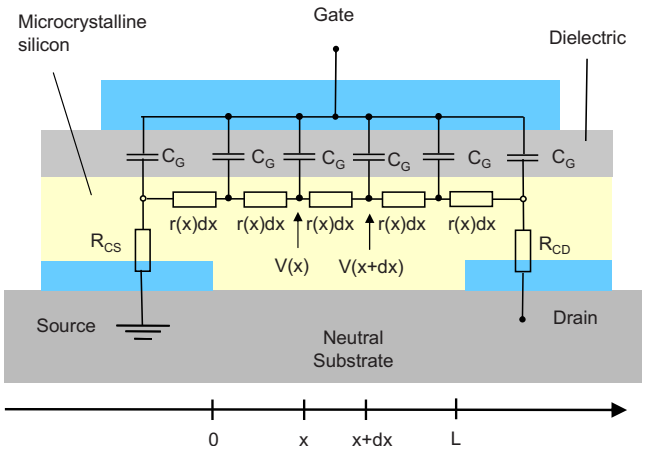

FIG. 4. (Color online) Equivalent circuit of a TFT. The transistor is described by a charge sheet model.

A. Unipolar TFTs

The differential resistance along the channel can be described by the following:

$$r(x) = \frac{1}{qW[\mu_n n(x) + \mu_p p(x)]}, \quad (1)$$

where μ_n and μ_p are the electron and the hole charge carrier mobilities, respectively. To calculate the resistance of the channel, R(x), as a function of the position we have to integrate over the differential resistance up to the specific position in the channel. At this stage we assume that the contact resistances can be neglected. The potential along the channel can be calculated by $V(x)=R(x)/R_{ch}\times V_D$, where R_{ch} is equal to the total channel resistance, R(x=L), which can be calculated by integrating over the complete channel and V_D is the drain voltage. In the case of a unipolar TFT the charges in the channel are either electrons or holes. In the case of electron transport the net surface charge is given by $-q\times n(x)$ and $p(x)=0$. In the case of a hole current the net surface charge can be described by $-q\times p(x)$ and $n(x)=0$. In the following we assume electron transport. After integration

the net surface charge as a function of the position in the channel can be calculated. At the drain electrode the net surface charge can be described by $Q(x=L)=C_G\times[V_D-(V_G-V_{Tn})]$, where V_G and V_{Tn} are the gate and the threshold voltage so that the total channel resistance can be calculated by the following:

$$R_{ch}=\frac{L}{\mu_n W C_G|V_G-V_{Tn}-V_D/2|}. \tag{2}$$

Combining the expression of the surface charge with the total channel resistance leads to an expression for the net surface charge, Q(x), which allows for calculating the electron concentration per unit area, which is given by $n(x)=-Q(x)/q$. The potential distribution along the channel is given by the following:

$$V(x)=(V_G-V_{Tn})\pm\sqrt{(V_G-V_{Tn})^2-2V_D(V_G-V_{Tn}-V_D/2)\frac{x}{L}}. \tag{3}$$

The drain current of the transistor can be expressed as $I_D=V_D/R_{Ch}$ leading to the classical equations describing the charge transport in a field-effect transistor. For $V_D<(V_G-V_{Tn})$ the transistor behaves like a normal unipolar transistor operating in the linear region. Since only electrons contribute to the current flow the parameter V_{Tn} describes the threshold voltage of an electron transporting TFT. The drain current in the linear region of operation is given by the following:

$$I_D=\frac{WC_G}{L}\mu_n V_D\left(V_G-\frac{V_D}{2}-V_{Tn}\right). \tag{4}$$

For $(V_G-V_{Tn})\leq V_D$ the transistor saturates and the drain current is given by the following:

$$I_D=\frac{WC_G}{2L}\mu_n(V_G-V_{Tn})^2. \tag{5}$$

Equations (4) and (5) describe the drain current for gate voltages larger than the threshold voltage. When the gate voltage is smaller than the threshold voltage, V_{Tn}, the mobile charge density in the channel is low so that the gate charge $Q_G=-Q_n-Q_T$, where Q_G, Q_n, and Q_T are the gate, mobile, and trapped charge density, can be approximated by the trapped charge density. When the semiconductor is very thin the band bending in the semiconductor can be neglected, which yields the following equation for the trapped charge density:

$$Q_T=-qN_T d_S\times(E_F-E_i), \tag{6}$$

where q is the elementary charge, N_T the trap density, d_s the thickness of the semiconductor, E_F and E_i are the Fermi and the intrinsic energy level. Since $Q_G=C_G V_G$, Eq. (6) can be written in the following form:

$$(E_F-E_i)=\frac{C_G V_G}{qN_T d_S}. \tag{7}$$

The electron concentration in the channel near the source, n, can be therefore described by the following:

$$n=n_i\exp\left(\frac{C_G V_G}{qN_T d_S kT}\right), \tag{8}$$

where n_i is the intrinsic carrier concentration. In the subthreshold regime, the current flow is controlled by charge diffusion.[21,22] If the drain voltage is larger than a few kT/q, the subthreshold current, I_{Dsub}, is described by the following:

$$I_{Dsub}=W\mu kTd_S\frac{dn}{dx} \tag{9}$$

or

$$I_{Dsub}=\frac{W}{L}C_G\mu d_S kTn_i\exp\left[\frac{q(V_G-V_{Tn})}{kT}\frac{C_G}{q^2N_T d_s}\right]. \tag{10}$$

The defect density of the μc-Si:H channel material, N_T, directly correlates with the subthreshold slope, S, of the transistor. The defect density can be calculated by the following:[21]

$$N_T=S\frac{C_G\log_{10}(e)}{qkTd_S}. \tag{11}$$

The drain current in all three regions of operation (linear region, saturation region, and subthreshold region) can be described by Eqs. (4), (5), and (10).

B. Ambipolar TFTs

In the following, the model will be extended to account for the ambipolar charge transport. The charge transport of ambipolar TFTs is determined by electrons and holes. Subsequently, the holes in the channel can be expressed by $p(x)=Q(x)/q+n(x)$. Schmechel *et al.*[23] were the first to use a charge-sheet model to describe the operation of ambipolar field effect transistors. In their study they investigated the operation of organic TFTs. However, the model does not describe the subthreshold behavior of the transistor. Here we extend the model to account for the operation of the transistors in all regions. Depending on the type of ambipolar transistor we can distinguish an n-type ambipolar transistor and a p-type ambipolar transistor as it is shown in Fig. 3. An n-type ambipolar transistor exhibits electron transport for small positive drain and positive gate voltages and electron and hole transport for high positive drain voltages and positive gate voltages. An p-type ambipolar transistor exhibits only hole transport for small negative drain voltages and negative gate voltages and electron and hole transport for large negative drain voltages and negative gate voltages. In the following we will discuss the operation of an n-type ambipolar TFT. During ambipolar operation the channel is filled by electrons from the source electrode to a point in the channel where the electrons recombine with the holes coming from the drain electrode of the transistor. The point at which the charges recombine is defined as x_0. At this point the net surface charge is zero, so that the voltage $V(x=x_0)=V_G-V_{Tn}$. The channel resistance is composed of two resistors, where the resistor, R_S, describes the resistance of the channel region ranging from the source electrode to the recombination point x_0. The charge transport in this region is governed by electrons. The resistor, R_D, describes the region from the

recombination point, x_0, to the drain electrode. The charge transport in this region is determined by holes. In other words, the ambipolar transistor can be treated as two serial connected field-effect transistors, where one of the transistors is an n-type transistor and the other transistor is a p-type transistor.

Since the charge transport in the channel region from the source electrode to the recombination point, x_0, is governed by electrons, we can assume that $Q(x)=-qn(x)$. Analog to the calculation for the unipolar transistor leading to the following expression for the total channel resistance from the source electrode to the recombination point, x_0:

$$R_S = \frac{2x_0}{\mu_n W C_G |V_G - V_{Tn}|}, \tag{12}$$

where V_{Tn} and μ_n are the threshold voltage and the carrier mobility from the source electrode to the recombination point x_0. Since the charge transport in the region from the recombination point to the drain electrode is governed by the holes, we can assume that $Q(x)=qp(x)$. Deriving an expression for the total channel resistance from the recombination point to the drain electrode as follows:

$$R_D = \frac{2(L - x_0)}{\mu_p W C_G |V_D - (V_G - V_{Tp})|}. \tag{13}$$

Since the current in both resistors has to be the same the following expression for the recombination point can be calculated:

$$x_0 = \frac{L}{1 + \frac{\mu_p}{\mu_n}\left[\frac{V_D - (V_G - |V_{Tp}|)}{V_G - |V_{Tn}|}\right]^2}. \tag{14}$$

To limit the complexity of the analytical model we assume that $|V_{Tp}| \cong |V_{Tn}|$. The location of the recombination zone within the channel of the transistor strongly depends on the applied drain voltage and the charge carrier mobilities. Since the mobility of the electrons for microcrystalline silicon is higher than the mobility of the holes the center of the recombination zone shifts from the center of the channel toward the drain electrode. The recombination point, x_0, depends on the carrier mobility ratio and not on the absolute values of the charge carrier mobility.

In the next step the potential distribution along the channel can be calculated by the following:

$$V_S(x) = (V_G - V_{Tn}) - (V_G - V_{Tn})\sqrt{1 \mp \frac{x}{x_0}}, \tag{15a}$$

$$V_D(x) = [V_D - (V_G - V_{Tp})]\sqrt{1 \mp \frac{L - x}{L - x_0}} + (V_G - V_{Tp}), \tag{15b}$$

where Eq. (15a) is valid in the region $(0 < x \leq x_0)$ and Eq. (15b) in region $(x_0 \leq x < L)$.

For $V_D < (V_G - V_{Tn})$ the drain current of the ambipolar transistor operates in the linear region and the charge transport is determined only by electrons, so that Eq. (4) is valid. For $(V_G - V_{Tn}) \leq V_D \leq (V_G - V_{Tp})$ the transistor saturates and the drain current is given by Eq. (5). The voltage, V_{Tp}, refers to the threshold voltage describing the holes transport in the channel. For $V_D \geq (V_G - V_{Tp})$ and $(V_G - V_{Tn}) > 0$ the transistor exhibits the behavior of an ambipolar transistor. Holes and electrons contribute to the current flow as follows:

$$I_D = \frac{W}{2L} C_G \{\mu_n (V_G - V_{Tn})^2 + \mu_p [V_D - (V_G - V_{Tp})]^2\}. \tag{16a}$$

Equation (16a) describes the transistor behavior for high drain voltages. However, Eq. (16a) is only valid if $V_D \geq (V_{Tn} + V_{Tp})$. For $V_D \leq (V_{Tn} + V_{Tp})$ both transistors operate in the subthreshold region. In this case the drain current is described by the following:

$$I_{Dsub} = \frac{W}{L} C_G d_S k T n_i \left\{ \mu_n \exp\left(\frac{(V_G - V_{Tn}) C_G}{q N_{Tn} d_S k T}\right) + \mu_p \exp\left(\frac{[V_D - (V_G - V_{Tp})] C_G}{q N_{Tp} d_S k T}\right)\right\}, \tag{16b}$$

where N_{Tn} and N_{Tp} are the electron and hole defect densities of the μc-Si:H of the channel material, respectively. For $V_D \geq (V_G - V_{Tp})$ and $(V_G - V_{Tn}) < 0$ the complete current flow is determined by holes resulting in the following expression:

$$I_D = \frac{W}{2L} C_G \{\mu_p [V_D - (V_G - V_{Tp})]^2\}. \tag{16c}$$

The four operation regions of an n-type ambipolar μc-Si:H TFTs can be divided in the linear region [electrons, Eq. (4)], saturation region [electrons, Eq. (5)], ambipolar region [electrons and holes, Eq. (16a) and (16b)] and saturation region [holes, Eq. (16c)]. In the following section the equations will be used to fit the experimental data and determine the device parameters.

V. DISCUSSION

The measured and fitted transfer characteristics of an n-type and p-type ambipolar μc-Si:H TFT with a channel length, L, of 20 μm and a channel width, W, of 1000 μm are shown in Figs. 2(a)–2(d), respectively. The experimental data of the n-type ambipolar transistor was fitted by using Eqs. (4), (5), and (16a)–(16c). The transfer curves in Fig. 2(c) were calculated for drain voltages of 0.1, 1, and 3 V, considering a threshold voltage of 1.85 V, and device charge carrier mobility of 52 $cm^2/V\,s$. The electron defect density was determined to be 4.8×10^{16} $cm^{-3}\,eV^{-1}$. The drain current of the transistor for negative gate voltages was fitted by adjusting the hole defect density and the threshold voltage, V_{Tp}, in Eqs. (16b) and (16c). The transfer curves for the p-type ambipolar TFT are shown in Fig. 2(d) for drain voltages of −0.1, −1, −3.0, and −5.0 V. The threshold voltage, V_{Tn}, and the hole charge carrier mobility were determined to be −5.7 V and 8 $cm^2/V\,s$, respectively. The electron defect density was determined to be 8.5×10^{16} $cm^{-3}\,eV^{-1}$. A summary of the extracted device parameters is given Table I. A comparison of the extracted device parameters with unipolar

TABLE I. Summary of extracted device parameters of an n-type and p-type ambipolar μc-Si:H TFTs. The parameters are compared to extracted device parameters of unipolar μc-Si:H TFTs.

	Effective electron mobility ($cm^2/V\ s$)	Effective hole mobility ($cm^2/V\ s$)	Electron threshold voltage (V)	Hole threshold voltage (V)	Electron defect density ($cm^{-3}\ eV^{-1}$)	Hole defect density ($cm^{-3}\ eV^{-1}$)
n-type ambipolar transistor	52	1–30	1.85	(−1.6)–(−3.5)	4.8×10^{16}	⋯
p-type ambipolar transistor	10^{-2}–10^{-1}	8	1.5–2.0	−5.7	⋯	8.5×10^{16}
n-type unipolar transistor	55	⋯	2.5–3	⋯	2×10^{16}	⋯
p-type unipolar transistor	⋯	12	⋯	4–5	⋯	6.5×10^{16}

n-type and p-type transistors exhibits similar device parameters.[24] The extracted device parameters of the ambipolar TFT are only slightly lower.

The extracted device parameters summarized in Table I were used as input parameters to calculate the potential and net surface charge distribution along the channel of the transistor. The potential and the normalized charge distribution of an n-type μc-Si:H transistor are shown Fig. 5(a) for different drain voltages. The gate voltage was assumed to be 2.5 V. For small drain voltages of 0.1 and 0.5 V the charge transport is only controlled by electrons [Fig. 5(a)]. The threshold voltage is equal to 1.85 V so that the transistor already exhibits ambipolar operation for drain voltages larger than 0.65 V. The potential distributions for drain voltages larger than 1.0 V are shown in Fig. 5(b). The position of the recombination point depends on the ratio of the charge carrier mobilities for electrons and holes, and the drain voltage. The transfer characteristic of the transistor in Fig. 2(c) can only be described if the hole mobility is drain voltage dependent. The hole charge carrier mobility increases with increasing drain voltage, whereas the electron mobility does not depend on the gate or drain voltage. The change in the hole mobility as a function of the drain voltage was considered when calculating the potential along the transistor channel. For small drain voltages of 1.0 and 1.5 V the hole mobility is significantly smaller than the electron mobility so that the voltage drop across the hole accumulating region close to the drain contact is high compared to the voltage drop across the electron accumulating region. Subsequently the electric field is high in the region close to the drain electrode. With increasing hole mobility the recombination point shifts toward the source electrode and the electric field in the hole accumulating region is reduced. The influence of the gate voltage on the potential distribution along the channel is shown in Fig. 6. The drain and the threshold voltages were assumed to

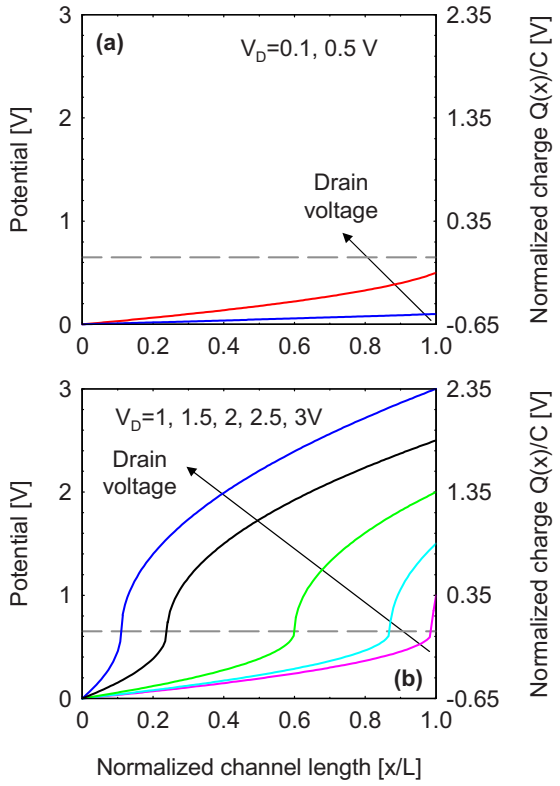

FIG. 5. (Color online) Calculated potential and normalized net surface charge distributions along the channel of an n-type ambipolar μc-Si:H TFT for different drain voltages. The input parameters were derived from the experimental data in Fig. 2(c).

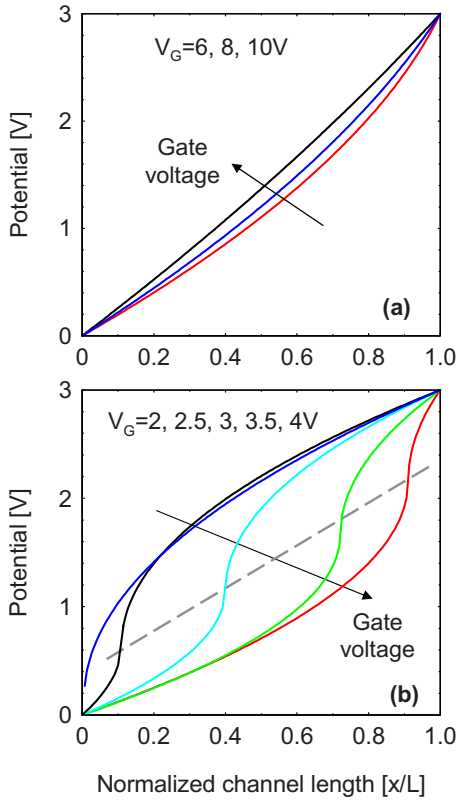

FIG. 6. (Color online) Calculated potential and normalized net surface charge distributions along the channel of an n-type ambipolar μc-Si:H TFT for different gate voltages. The input parameters were derived from the experimental data in Fig. 2(c).

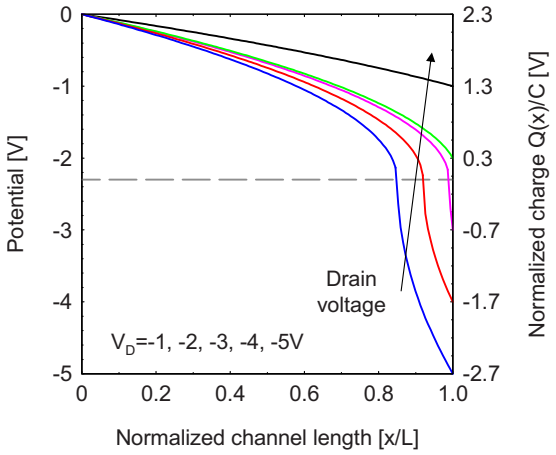

FIG. 7. (Color online) Calculated potential and normalized net surface charge distributions along the channel of a p-type ambipolar μc-Si:H TFT for different drain voltages. The input parameters were derived from the experimental data in Fig. 2(b).

be 3.0 and 1.85 V. For large gate voltages of 8.0, 9.0, and 10.0 V the channel is filled with electrons and unipolar charge transport is observed [Fig. 6(a)]. For gate voltages smaller than 5.85 V ambipolar transport is observed. The dashed line in Fig. 6(b) marks the transition from electron to hole charge transport. The curves above the dashed line represent hole charge transport, whereas the curves below the dashed line describe electron charge transport. When decreasing the gate voltage the recombination point shifts from the drain to the source electrode. The electric field is highest for the recombination point. For a gate voltage of 2.0 V the complete channel is filled with holes and the electrons do not contribute to the charge transport anymore.

The same analysis was repeated for the p-type ambipolar transistor. The potential distribution and the normalized charge are shown in Fig. 7 for different drain voltages. The threshold voltage of the p-type device is high with −5.7 V, so that we assumed an applied gate voltage of −8.0 V. Ambipolar charge transport is observed for drain voltages of −3.0, −4.0, and −5.0 V. The absolute drain voltage at which ambipolar transport is observed decreases with decreasing absolute values of the gate voltage. Irrespective of the applied voltages the recombination point is relatively close to the drain electrode since the electron carrier mobility is significantly lower than the hole mobility for the p-type ambipolar transistor. Due to the low electron mobility a high electric field is obtained in the region between the recombination point and the drain electrode.

Measurements of different ambipolar transistors with different channel lengths show that the contact resistance has a distinct influence on the device carrier mobility. Further information on the contact resistance of ambipolar μc-Si:H TFTs is given in reference.[25] The normalized contact resistance for n-type transistor is in the range of 1 kΩ cm, whereas the p-type ambipolar transistors exhibit a contact resistance of 4 kΩ cm. The contact resistance has a significant influence on the potential and net surface charge distribution along the channel of the transistor for short channel transistors. In this study we have concentrated on transistors with a channel length of 20 μm, where the influence of the contact resistance on the overall device performance is still relatively small. To account for the influence of the contact resistance on the potential Eq. (3) has to be modified.

Ambipolar TFTs allow for the realization of complementary logic circuitry on glass or flexible substrates at low deposition temperatures. The transistors in this study were fabricated at temperature of 160 °C. The logic circuits can be integrated as line and row drivers of flat panel displays. Ideally the voltage gain, which is defined as $v_{GAIN} = \partial V_{OUT}/\partial V_{IN}$, where V_{OUT} and V_{IN} are the output and input voltage of the inverter should be high while the power consumption and the operating voltages are low. The ambipolar inverter characteristic is usually limited by the transistor operating in the off-state. Since the off-current is relatively high the voltage transfer characteristic of the ambipolar inverter deviates from an ideal CMOS inverter characteristic. As a consequence the noise margin of the ambipolar inverter is reduced and the power consumption is increased, which limits the realization of complex thin-film circuitry. The problem can only be reduced by selecting the right operating voltages of the inverter. Conventional CMOS inverters exhibit an increase in the noise margin with increasing operating voltages. However, this is not the case for ambipolar inverters.[25] In order to realize ambipolar inverters with high voltage gain and lower power consumption the threshold voltages of the individual transistors should be low so that the circuits can be operated at low operating voltages. In general, it can be concluded that ambipolar inverters are an interesting addition to existing CMOS inverter technology. However, the specific disadvantages of the technology have to be taken into account when designing ambipolar inverter based circuitry.

VI. CONCLUSIONS

Ambipolar microcrystalline silicon TFTs were realized at temperatures below 200 °C with high electron and hole charge carrier mobilities of 52 $cm^2/V\,s$ and 8 $cm^2/V\,s$, respectively. The use of ambipolar transistors provides a simple route in realizing large-area integrated circuits at low cost based on μc-Si:H TFTs. A simple analytical approach based on a charge-sheet model was presented, that allows for describing the current voltage characteristic of unipolar and ambipolar TFTs. Furthermore, the model allows for calculating the potential and the net surface charge distribution along the transistor channel of unipolar and ambipolar devices. The electrical model provides insights into the electronic transport of the ambipolar μc-Si:H TFTs. The potential and the charge distributions along the channel were calculated by using the extracted device parameters.

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