Microcrystalline silicon thin-film transistors operating at very high frequencies

Marko Marinkovic, Elias Hashem, Kah-Yoong Chan, Aad Gordijn, Helmut Stiebig, and Dietmar Knipp

Citation: Applied Physics Letters **97**, 073502 (2010); doi: 10.1063/1.3481391
View online: http://dx.doi.org/10.1063/1.3481391
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/97/7?ver=pdfcov
Published by the AIP Publishing

Microcrystalline silicon thin-film transistors operating at very high frequencies

Marko Marinkovic,[1] Elias Hashem,[1] Kah-Yoong Chan,[1,2,3] Aad Gordijn,[2] Helmut Stiebig,[2,4] and Dietmar Knipp[1,a)]
[1]*School of Engineering and Science, Jacobs University Bremen, 28759 Bremen, Germany*
[2]*IEF5-Photovoltaics, Research Center Jülich, 52425 Jülich, Germany*
[3]*Faculty of Engineering, Multimedia University, Selangor, 63100 Cyberjaya, Malaysia*
[4]*Malibu GmbH & Co. KG, 33609 Bielefeld, Germany*

(Received 16 January 2010; accepted 31 July 2010; published online 18 August 2010)

The switching behavior of hydrogenated microcrystalline silicon thin-film transistors (TFTs) was examined and switching frequencies exceeding 20 MHz were measured for short channel devices. The microcrystalline silicon TFTs were prepared by plasma-enhanced chemical vapor deposition at temperatures compatible with plastic substrates. The realized microcrystalline silicon transistors exhibit high electron charge carrier mobilities of 130 $cm^2/V\,s$. The switching frequency is limited by the contact resistances and overlap capacitances between the gate and the drain/source electrodes. Switching frequencies larger than 20 MHz were measured for transistors with a channel length of 5 μm. The high switching frequencies facilitate the realization of radio-frequency identification tags operating at 13.56 MHz. © *2010 American Institute of Physics*. [doi:10.1063/1.3481391]

The great interest in radio frequency identification tags (rfid tags) has stimulated considerable research on flexible or printed electronics.[1] Even though different material systems exhibit very promising performance silicon possesses a significant advantage over the other technologies since silicon thin film transistors are the current standard in display industry and devices can be prepared at low temperature on large areas.[1,2] However, existing silicon thin-film technologies suffer from several drawbacks; low charge carrier mobility and device stability for amorphous silicon TFTs and high fabrication cost for polycrystalline silicon TFTs.[1–4]

Recent developments reveal that micro or nanocrystalline silicon is a promising alternative for large area electronic applications like flexible displays or rfid tags. The charge carrier mobility exceeds the mobilities of amorphous silicon significantly, while the preparation conditions are comparable, which allows for an inexpensive device preparation on large areas.[5–9] Therefore, the fabrication cost is significantly lower than the cost for the fabrication of polycrystalline silicon TFTs.

In this paper, the switching behavior of microcrystalline silicon thin film transistors was investigated and the limiting factors were identified. The schematic cross-section of the realized microcrystalline silicon TFTs is depicted in Fig. 1. Top-gate staggered transistor structures were investigated in this paper since the electronic properties of bulk microcrystalline silicon are superior to the properties of the nucleation layer. The drain and source metal contacts of the TFTs were realized by electron-beam evaporated chromium with a thickness of 30 nm on glass substrates. Afterwards, an n-type microcrystalline silicon film with a thickness of 25 nm was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 180 °C to form Ohmic contacts between the drain and source metal electrodes and the intrinsic channel material. The thickness of the channel layer was chosen to be 100 nm, which is thick enough to ensure high quality microcrystalline silicon bulk properties. On the other hand the channel layer should be thin to minimize the series resistance between the drain/source electrode and the accumulation region close to the gate dielectric. The 100 nm thick intrinsic microcrystalline silicon channel layer was prepared by PECVD at 160 °C, in the high pressure (1330 Pa) and high power ($0.3\ W/cm^2$) regime, which facilitates the deposition of material at high deposition rates of up to 25 nm/min.[10,11] The films were prepared near the transition to amorphous growth. The crystalline volume fraction of the films measured by Raman spectroscopy was equal to 45%–50%. Films prepared near the transition to amorphous exhibit the highest charge carrier mobility.[12] The n- and i-layers were prepared at an excitation frequency of 13.56 MHz. Following the deposition of the i-layer, a gate dielectric (silicon oxide, SiO_2) of 300 nm thickness was prepared by PECVD at 150 °C. Silicon oxide was used as gate dielectric instead of silicon nitride to minimize the defect density at the channel/dielectric interface.[13,14] Finally, the gate electrode was formed by an electron-beam evaporated aluminum film of 100 nm thickness. Prior to electrical characterizations, all transistors were annealed at 150 °C for 30 min under ambi-

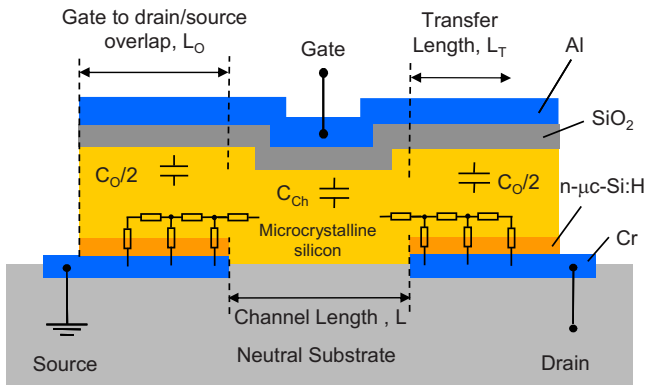

FIG. 1. (Color online) Schematic cross-section of a top-gate staggered microcrystalline silicon TFT.

a)Electronic mail: d.knipp@jacobs-university.de.

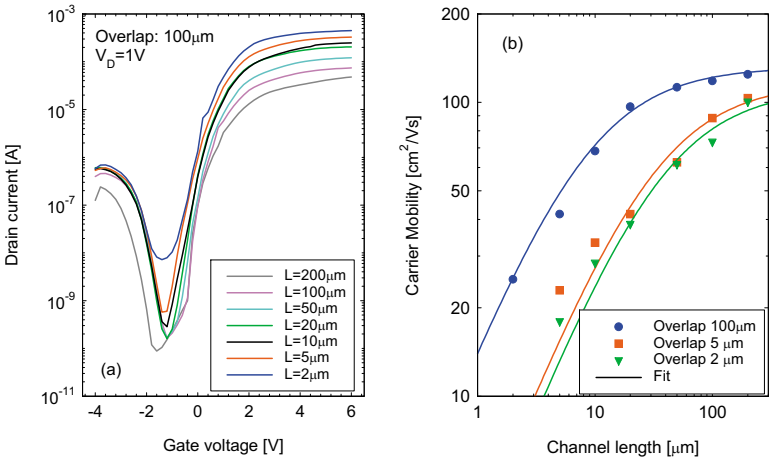

FIG. 2. (Color online) (a) Transfer characteristics of microcrystalline silicon TFTs for channel lengths ranging from 2 to 200 μm for a drain voltage of 1.0 V. (b) Device carrier mobility of microcrystalline silicon thin film transistors as a function of the channel length for different overlaps of the gate to drain/source contacts.

ent conditions.[15] The electrical characterization of the TFTs was performed at room temperature under dark conditions.

The transfer characteristics of microcrystalline silicon TFTs with channel lengths ranging from 2 to 200 μm and channel width of 1000 μm are shown in Fig. 2(a). The transfer characteristics were measured for a drain voltage, V_D, of 1.0 V. The transistor exhibits low threshold voltages and on/off ratios of more than four orders of magnitude. The charge carrier mobilities were extracted from the measured transfer characteristics in the linear region of operation. The charge carrier mobility is plotted in Fig. 2(b) as a function of the channel length. The charge carrier mobility was measured for transistors with a gate to drain/source overlap, L_O, of 2 μm, 5 μm, and 100 μm. The charge carrier mobility drops with decreasing channel length. Considering an Ohmic contact behavior, the following expression for the mobility can be derived:

$$\mu_{\text{eff}} = \mu_0 \cdot \frac{L}{L + \mu_0 \cdot r_C \cdot C_G \cdot (V_G - V_T - V_D/2)}, \tag{1}$$

where μ_0 is the field effect mobility of the microcrystalline channel material and μ_{eff} is the device mobility extracted from the measured transistors, where L, W, and C_G are the channel length, channel width and the gate capacitance per unit area, respectively.[16] V_G, V_D, and V_T are the gate voltage, the drain voltage, and the threshold voltage, respectively. The normalized contact resistance, r_C, is given by the product of the contact resistance, R_C, and the channel width W. We extracted an electric field mobility, μ_0, of 130 $\text{cm}^2/\text{V s}$ and a normalized contact resistance of 0.3 $\text{k}\Omega$ cm for transistors with a large gate to drain/source overlap (100 μm). Transistors with a small gate to drain/source overlap of 5 and 2 μm exhibit mobilities of 120 and 110 $\text{cm}^2/\text{V s}$, and normalized contact resistances of 1.35 and 1.5 $\text{k}\Omega$ cm. The normalized contact resistances are in good agreement with measurements of the contact resistance by the transfer length method. For long channel devices the contact resistance has only a small influence on the device mobility, whereas for short channel lengths a distinct drop of the device mobility is measured. For transistors with large gate to source/drain overlap ($L_O \gg L_T$) the normalized contact resistance can be described by

$$r_C \approx \frac{\rho_C}{L_T} = \sqrt{\rho_C R_S}, \tag{2}$$

where L_T is the transfer length of the transistor, R_S is the sheet resistance of the transistor channel, and ρ_C the specific contact resistance between the chromium drain and source electrode and the microcrystalline silicon layer. The transfer length defines the critical distance over which most of the charge is transferred from the drain and source contacts to the channel material.[16] The transfer length is measured from the edge of the drain and the source electrodes (Fig. 1). The transfer length can be calculated by

$$L_T = \sqrt{\frac{\rho_C}{R_S}}. \tag{3}$$

The sheet resistance can be expressed in terms of the transistor parameters leading to the following expression for the transfer length

$$L_T = \sqrt{\rho_C C_G \mu_0 (V_G - V_T)}. \tag{4}$$

We determined a specific contact resistance of 0.07 $\Omega\ \text{cm}^2$ and a transfer length of 3 μm for $V_G - V_T = 1$ V and 7 μm for $V_G - V_T = 5$ V. For small gate to drain/source overlaps of 5 and 2 μm not all the charges can be transferred from the drain and source electrodes to the channel, so that the device mobility drops. Typical transfer lengths of high mobility organic, amorphous silicon or gallium-indium doped zinc oxide (GZO) thin film transistors range from 0.3 to 2 μm.[17–19] The transfer length of microcrystalline silicon thin film transistors is higher because of the relatively high charge carrier mobility and specific contact resistance. A further reduction in the gate to drain/source overlap well below the transfer length will lead to a drop of the device mobility.

The transfer frequency of a microcrystalline silicon thin film transistor as function of the channel length is shown in Fig. 3. The transfer frequency defines the operating frequency at which the gate current of the transistor is equal to the transistor drain current.[20] The transfer frequency of an ideal field effect transistor is given by

$$f_T = \frac{1}{2\pi} \cdot \frac{\mu_{\text{eff}} V_D}{L^2}, \tag{5}$$

where μ_{eff} is the effective device mobility.[20] The transfer frequency scales by $1/L^2$, so that a reduction in the channel length by one order of magnitude leads to an increase in the

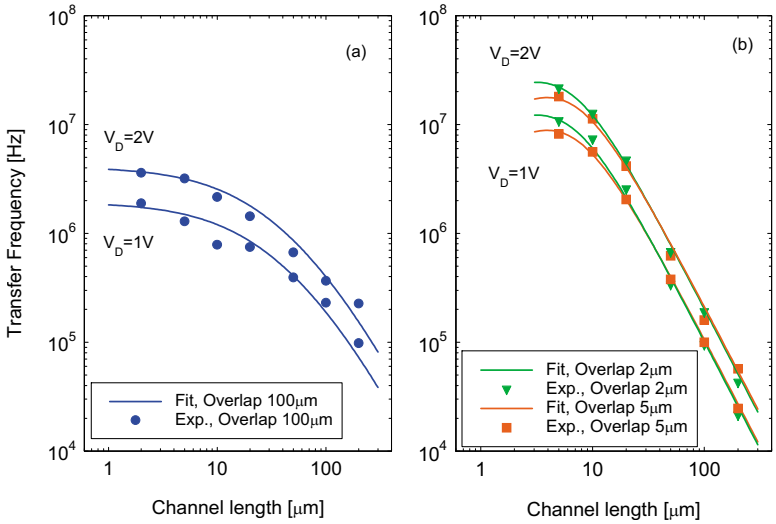

FIG. 3. (Color online) Transfer frequency for microcrystalline silicon thin film transistors with gate to drain/source overlap of 100 μm (a), 5 μm (b), and 2 μm (b).

transfer frequency by two orders of magnitude. The transfer frequency was measured for gate to drain/source overlaps of 100, 5, and 2 μm. For transistors [Fig. 3(a)] with a large gate to drain/source overlap of 100 μm a transfer frequency of up to 4 MHz was measured for a low drain voltage of 2 V. For transistors with small gate to drain/source overlaps of 5 and 2 μm the transfer frequency reaches more than 20 MHz for a drain voltage of 2 V. For transistors with a channel length of 10 to 200 μm the transfer frequency can be described by Eq. (5) and the transfer frequency scales by $1/L^2$. For transistors with a channel length of less than 10 μm a saturation of the transfer frequency is obtained. The saturation is caused by the influence of the contact resistors and the overlap capacitance on the device operation. The contact resistances at the drain and source electrodes of the transistor lead to a reduction in the device mobility and therefore to a drop of the transfer frequency. Furthermore, the transfer frequency is reduced by the overlap capacitance between the gate electrode and drain/source electrodes. For large gate to drain/source overlaps or short transistors channels the overlap capacitance has a distinct influence on the upper limit of the transfer frequency. In order to account for the influence of the overlap capacitance Eq. (5) has to be multiplied by $C_{Ch}/(C_{Ch}+C_O)$, where $C_{Ch}=C_G\times W\times L$ is the channel capacitance and C_O is the gate to drain/source overlap capacitance. A comparison of Figs. 3(a) and 3(b) shows that the transfer frequency of transistors with the large overlap is higher for transistors with channel lengths exceeding 30 μm. The transfer frequency for long channel length is determined by the contact resistance rather than the overlap capacitance. Since the contact resistance of the transistor with the large gate to drain/source overlap is small the transfer frequency is high. For transistors with short channel lengths the transfer frequency is dominated by the overlap capacitance, so that the higher transfer frequency is obtained for the transistors with the small gate to drain/source overlap. To achieve operating frequencies well above 100 MHz the channel length and the specific contact resistance have to be decreased. The overlap of gate to drain/source should be small but not significantly smaller than the transfer length.

In summary, top-gate microcrystalline silicon TFTs were realized at maximum process temperature of 180 °C with high electron charge carrier mobilities exceeding 100 cm^2/V s. In this study, the transient behavior of microcrystalline silicon channel material was investigated. The contact resistance and the overlap capacitance have a distinct influence on the transfer frequency. For short channel transistors the transfer frequency is limited by the contact resistance and the overlap capacitance. Maximum transfer frequencies exceeding 20 MHz have been achieved for transistors with a channel length of 5 μm.

The authors like to acknowledge S. Bunte and Y. Mohr (IBN-PT) for preparation of the PECVD SiO_2, M. Hülsbeck, J. Kirchhoff, T. Melle, S. Michel, and R. Schmitz for technical assistances and E. Bunte, R. Carius, D. Hrunski, S. Reynolds, and V. Smirnov for helpful discussions.

[1] *Flexible Electronics: Materials and Applications*, edited by W. S. Wong and A. Salleo (Springer, Heidelberg, 2009).
[2] *Thin-Film Transistors*, edited by C. R. Kagan and P. Andry (Marcel Dekker, New York, Basel, USA, 2003).
[3] B. Stannowski, R. E. I. Schropp, R. B. Wehrspohn, and M. J. Powell, J. Non-Cryst. Solids **299–302**, 1340 (2002).
[4] M. J. Powell, Appl. Phys. Lett. **43**, 597 (1983).
[5] J. I. Woo, H. J. Lim, and J. Jang, Appl. Phys. Lett. **65**, 1644 (1994).
[6] I.-C. Cheng and S. Wagner, Appl. Phys. Lett. **80**, 440 (2002).
[7] C.-H. Lee, A. Sazonov, and A. Nathan, Appl. Phys. Lett. **86**, 222106 (2005).
[8] K. Kandoussi, A. Gaillard, C. Simon, N. Coulon, T. Pier, and T. Mohammed-Brahim, J. Non-Cryst. Solids **352**, 1728 (2006).
[9] K.-Y. Chan, E. Bunte, H. Stiebig, and D. Knipp, Appl. Phys. Lett. **89**, 203509 (2006).
[10] L. Guo, M. Kondo, M. Fukawa, K. Saitoh, and A. Matsuda, Jpn. J. Appl. Phys., Part 2 **37**, L1116 (1998).
[11] B. Rech, T. Roschek, J. Muller, S. Wieder, and H. Wagner, Sol. Energy Mater. Sol. Cells **66**, 267 (2001).
[12] K.-Y. Chan, D. Knipp, A. Gordijn, and H. Stiebig, J. Appl. Phys. **104**, 054506 (2008).
[13] Y. Ma, T. Yasuda, and G. Lucovsky, J. Vac. Sci. Technol. A **11**, 952 (1993).
[14] S. W. Hsieh, C. Y. Chang, and S. C. Hsu, J. Appl. Phys. **74**, 2638 (1993).
[15] K.-Y. Chan, E. Bunte, H. Stiebig, and D. Knipp, J. Appl. Phys. **101**, 074503 (2007).
[16] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).
[17] A. Hoppe, D. Knipp, B. Gburek, A. Benor, M. Marinkovic, and V. Wagner, Org. Electron. **11**, 626 (2010).
[18] S. Luan and G. W. Neudeck, J. Appl. Phys. **72**, 766 (1992).
[19] J. Park, C. Kim, S. Kim, I. Song, S. Kim, D. Kang, H. Lim, H. Yin, R. Jung, E. Lee, J. Lee, K.-W. Kwon, and Y. Park, IEEE Electron Device Lett. **29**, 879 (2008).
[20] M. Shur, *Introduction to Electronic Devices* (Wiley, New York, 1990).