A Flexible Data Acquisition Board for Nuclear Detectors

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Abstract—For two-dimensional scintillation detectors based on position-sensitive photomultipliers, a new PCI or cPCI unit has been developed. It aims at fast signal and data processing by the usage of advanced technologies like digital signal processors and field-programmable gate arrays. The main features of this design are described in this paper. Digital test measurements were carried out showing that the chosen design complies with the requirements of nuclear pulse processing for such applications.

Index Terms—Detector, detector read out, digital signal processor (DSP), field-programmable gate array (FPGA), neutron, photomultiplier, UniDAQ.

I. INTRODUCTION

TWO-DIMENSIONAL detectors with position-sensitive photomultipliers are described in [1]–[3]. Such detectors are useful in gamma scintigraphy and in neutron scattering experiments. The detector size of 100 mm diameter and the obtainable spatial resolution of about 1.5 mm with a ^{6}Li-glass scintillator are adequate in high-resolution diffraction and reflection experiments [4] and [5]. Furthermore, if the detector is equipped with a CsI scintillator and lead collimator, a spatial resolution of 2 mm for 140-keV gammas is achieved, which is sufficient for use in clinical tests of thyroid scintigraphy. The pulse handling for these detector systems is usually done by an analog-based pulse and data processing, which requires a slow separate timing circuit for digitizing the maximum signal.

To reduce the electronic dead time of such systems, a new data acquisition board, the *Universal Digital Signal Processor Data Acquisition* board (UniDAQ), has been developed and is shown in Fig. 2. This one-slot board includes all the temporary information of the detector signals and allows for a complete pulse shape discrimination, e.g., to distinguish between a gamma and a neutron pulse. In our main application, only the maximum value of the shaped pulse is determined from this temporary information. It is further processed in a pulse-height discrimination with preset discriminator levels. The resulting digital information can then be used in multichannel analyzer (MCA) applications and for position-sensitive particle

detection. In the following sections, we describe the layout of UniDAQ and its use in combination with a position-sensitive photomultiplier tube (PMT) from Hamamatsu (R3292).

II. DATA ACQUISITION BOARD

Fig. 1 shows the block diagram of a UniDAQ board containing a digital signal processor (DSP), a field-programmable gate array (FPGA), and four main amplifiers, which are equipped with free-running analog-to-digital converters (ADCs). We decided to use the D-Module C6701 as an ultra-high-performance solution for the most embedded DSP applications. The D-Module contains the Texas Instruments 320C6701 DSP with 32-bit floating-point arithmetic, with a speed of 800 Mflop and a memory of 512 kByte. The FPGA is a XILINX product of the Virtex family of the XCV300 type with more than 300 000 gates. As DSP and FPGA are programmable components, a large field of specific applications may be covered by this board. In our application, the FPGA has to determine the maximum and the position by a division. The FPGA units in combination with the DSP can certainly perform much more sophisticated tasks.

Furthermore, the board may be equipped with either a standard PCI or a compact PCI (cPCI) interface connector, which allows it to be used in a normal PC as well as in an industrial 19-in crate environment.

The four free-running ADCs generate a stream of data at a rate of 40 ADCs 12-bit words per microsecond. This data stream is analyzed by the FPGA to obtain the pulse maxima. The condition for a local maximum is that the actual word sum is smaller than the previous and the consecutive word sum, provided the values exceed the lower level discriminator. Because of integration and differentiation of the analog pulses, it is sufficient to determine only their maximum and not the integral under the digitized pulses, which would take much more time. As a final result of this pulse processing, four ADC words are obtained that are close to the local maximum. This maximum search is completed within one ADC cycle.

To calculate the position of the event, the signal ratios Q_x and Q_y have to be calculated in the FPGA according to (1) and (2)

$$Q_x = \frac{\text{ADC1} - \text{ADC2}}{\text{ADC1} + \text{ADC2}} \tag{1}$$

$$Q_y = \frac{\text{ADC3} - \text{ADC4}}{\text{ADC3} + \text{ADC4}}. \tag{2}$$

Apart from some offset values, Q_x and Q_y represent the direct storage address of the current event. This calculation takes less than 1 μs.
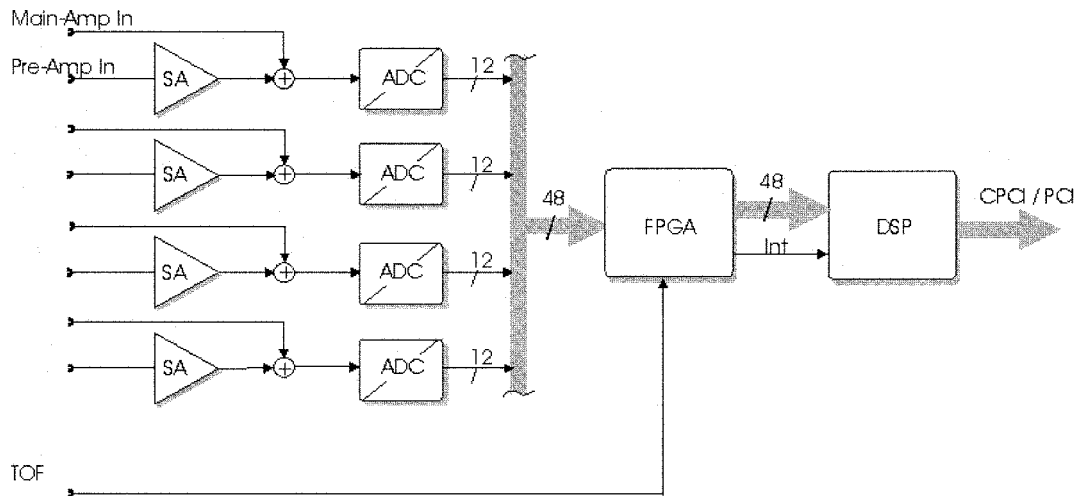
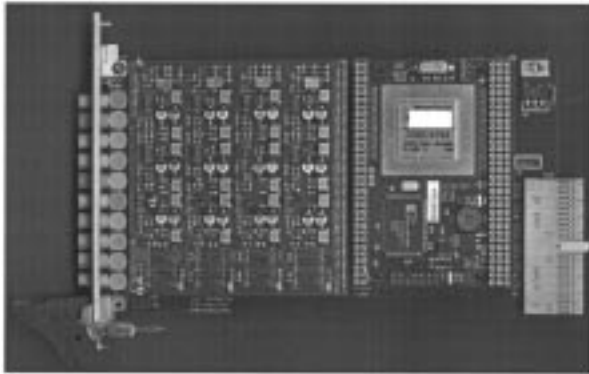Fig. 1. Block diagram of the signal processing.

Fig. 2. Picture of the UniDAQ board.

The four ADC maxima words, and the Q_x and Q_y words are then transferred to the DSP (Texas Instruments C6701) module. The sum pulse

$$\text{Sum} = (\text{ADC1} + \text{ADC2} + \text{ADC3} + \text{ADC4}) \qquad (3)$$

is then compared with the upper and lower discriminator levels, which are stored in a lookup table onboard indexed by the position values Q_x and Q_y. These discriminator values are determined in a calibration mode, where the detector is exposed to a homogeneous radiation field. For neutron scintillation detectors, the gamma discrimination is usually performed via pulse-height discrimination. In cases where the neutron signal heights are position-dependent, it is mandatory to discriminate not with one discriminator level but with discriminator levels that are position-dependent. Since there is considerable inhomogeneity of photocathode sensitivity, this position-dependent discrimination is necessary for an efficient rejection of gammas. In the case where the sum fits between the discriminator values, the final step is to increment the memory cell that is addressed by the position of Q_x and Q_y. The processing time for these three steps in the DSP is less than 3 μs.

To operate the board under Windows NT, a device driver (SYS) was developed. The driver serves as a hardware-oriented interface to 32-bit applications and provides numerous functions like allocating memory, reading data, etc. This set of op-erations represents a basis for most applications and can easily be extended. The driver may be either statically or dynamically loaded.

III. EXPERIMENTAL RESULTS

Tests of the board prototype were performed by applying analog signals to the four main amplifiers. At first, different pulse shapes were observed due to the tolerances of the electronic components used. Because the position reconstruction strongly depends on equal pulse shapes, a digital stretcher was implemented in the FPGA. Thus, when the maxima of the individual channels are reached, they are stored in order to obtain the maximum sum value. This leads to a better position determination according to (1) and (2).

In the first design, there was also considerable frequency noise in the range of 10 mV on the sampled signals. It was caused by the DSP and FPGA clocks due to the compact board size. This noise is ineffective because of synchronized digitization. In the completely new redesign, analog filtering was implemented. Operational amplifiers with improved parameters (gain bandwidth, low noise, low power) were used.

After these improvements had been made, a satisfactory rela-tive electronic resolution of $\pm 1/2$ based on 256 channels across the detector area was measured. This corresponds to an elec-tronic contribution to the spatial resolution of less than ± 0.5 mm for a 5-in position-sensitive PMT [6]. This electronic contribu-tion was sufficiently small compared with the physical spatial resolution of 2 mm, as determined by a ^{6}Li glass scintillator, and 1 mm with a LiGd borate scintillator.

In addition, the position reconstruction was tested with the improved board. Fig. 3 shows one of the four time signals dig-itized at 40 MHz. During the test measurements, the individual pulse heights were changed in order to simulate the statistical fluctuations of real detector signals. In addition, the pulse ra-tios were changed over time in order to simulate special event patterns. Fig. 4 shows the result of such a measurement. Here the numerators of (1) and (2) are changed stepwise over time according to sine and cosine functions, simulating event distri-butions according to circles with several radii. The simulation
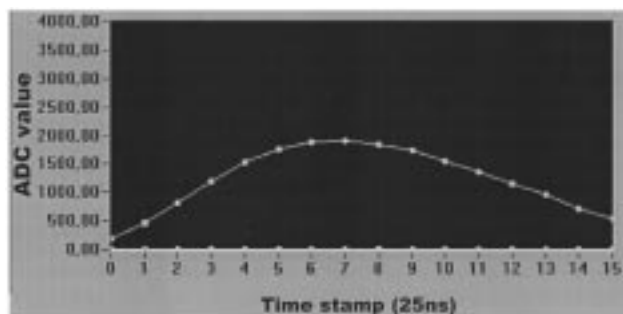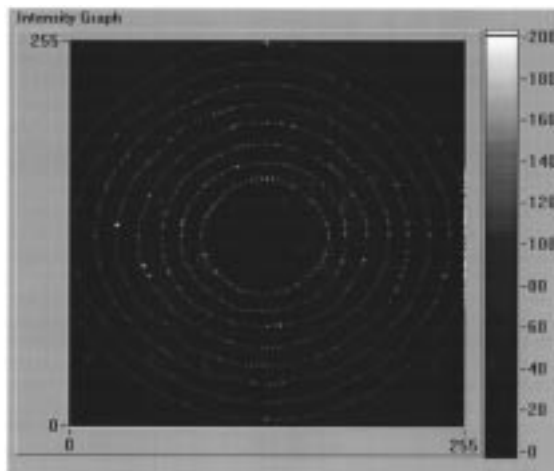
Fig. 3.   Digitized signal of one channel.

Fig. 4.   Two-dimensional plot of simulated detector signals.
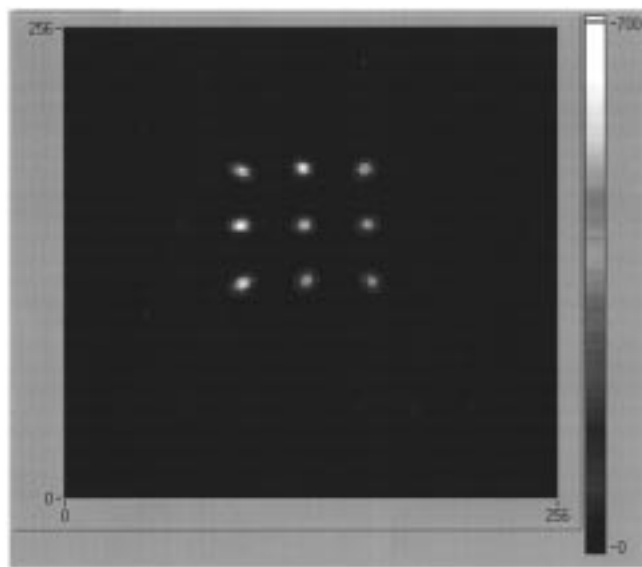

Fig. 5.   Two-dimensional gamma intensity distribution measured with a Pb diaphragm of 2-mm holes and 18-mm spacing.

results clearly demonstrate the linearity of the detector response over a wide pulse range. The finite thickness of the circles indicates the satisfactorily low levels of noise.
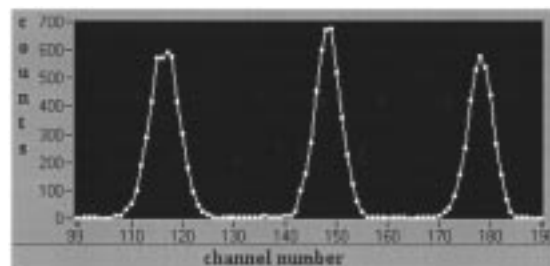

Fig. 6.   Horizontal line-intensity scan through the center of Fig. 6.

IV. REAL DATA ACQUISITION

Because of a long period of reactor shutdown, real data were collected with low-energy gammas from a ^{99m}Tc source. A lead diaphragm of 4 mm thickness with nine holes of 2 mm diameter and separated by 18 mm was placed in front of a NaI scintillator of 7 mm thickness optically coupled to the detector front attached to a 5-in position-sensitive PMT. The 141-keV gamma generates a pulsed height in a NaI, which is approximately a factor of two smaller than the pulse that a neutron generates in a ^{6}Li-glass scintillator.

The two-dimensional plot in Fig. 5 shows nine well-resolved separated peaks.

For a quantitative evaluation, a horizontal line scan of these data is shown in Fig. 6. A full-width at half-maximum of the peaks of 3.5 mm is determined. This corresponds to the spatial resolution of the detector of 3 mm.

V. CONCLUSION

The design of a new data acquisition board for MCA and position-sensitive PMT applications is presented. It uses advanced FPGA and DSP technologies for pulse processing, which leads to short overall dead times of less than 2 μs in contrast to more than 10 μs for the commonly used analog methods. The performance of this design was demonstrated with real detector data and satisfactory results were obtained.

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