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Annealing effects in low temperature amorphous silicon flexible solar cells

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Abstract

We report the effects of prolonged post-deposition annealing on the performance of amorphous silicon (a-Si:H) solar cells and single layers, that are fabricated at low temperature of 120 °C on flexible PET and glass substrates. These low temperature solar cells show a significant improvement in performance upon post-deposition annealing (up to two hours) in all parameters of the current-voltage (JV) curves of the solar cell, resulting in an efficiency increase up to 34 % (relative). Comparison of external quantum efficiencies of p- and n-side illuminated cells, as well as varied absorber layer thicknesses and reverse bias voltage, suggest that the collection of minority carriers are mainly improved upon annealing. Both the increase of the built-in field in the solar cell and improvement in the electronic properties of the absorber layer were found to contribute to an improved carrier collection and solar cell performance.

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1. Introduction

Thermal annealing effects in amorphous silicon (a-Si:H) solar cells have been a subject of intensive studies. A significant portion refers to reduction in performance of a-Si:H solar cells under prolonged illumination, known as Staebler-Wronski-Effect (SWE) [1], and corresponding improvement in performance upon annealing. Various aspects of the annealing behaviour have been studied: degradation-annealing kinetics, variations in annealing temperatures and also times [2–6]. The light-soaking generated effects are usually reversible upon annealing. In such case, the reduction and improvement in performance are commonly related to the intrinsic absorber layer, particularly the decrease or increase in defect density, which are commonly related to hydrogen atoms and dangling bonds. The hydrogen content of amorphous silicon, which is linked to other properties like band gap and conductivity, critically depends on the deposition temperature during the plasma enhanced chemical vapour deposition (PECVD) process. Hydrogen-rich a-Si:H materials, usually obtained at lower deposition temperatures, are known to be more sensitive to prolonged illumination than layers containing less hydrogen, resulting in a higher magnitude of changes during the light-soaking-annealing cycles [7]. An advantage of amorphous silicon solar cells produced at low temperatures below 140 °C, is the suitability for use on low cost plastic films for flexible devices. These flexible devices have the advantages of being lightweight and enabling specialized applications like building integrated photovoltaics (BIPV) with a variety of shapes and sizes. However, low temperature solar cells are particularly sensitive to post-deposition annealing treatments. Brinza et al. studied a-Si:H solar cells deposited at 100 °C and showed an efficiency increase of up to 40 % due to post-deposition annealing at 100 °C, mainly due to an increase in $V_{oc}$ [8]. Other studies reported an even stronger increase in efficiency up to a factor of 5 for a deposition temperature of 75 °C and annealing at 110 °C, caused by a strong increase in short-circuit current density [9]. An improvement of 50 % was found by Wang et al. for amorphous silicon germanium solar cells prepared at 200 °C for different annealing temperatures up to 230 °C [10]. In this work, we report on the effects of post-deposition annealing of low temperature (120 ± 10 °C) amorphous silicon solar cells, prepared on glass and transparent polyethylene terephthalate (PET) substrates. We show that all parameters of the current-voltage (JV) curves of our a-Si:H solar cells are significantly improved upon annealing at 120 °C during more than two hours, resulting in an efficiency improvement up to 34 % relative. While only slight changes were found in the electrical and optical properties of the individual layers upon annealing, a comparison of performance of p- and n-side illuminated cells with varied absorber layer thicknesses suggest that the minority carriers are largely responsible for the improvement in the performance of the solar cells by post-deposition annealing.

2. Experimental

Amorphous silicon (a-Si:H) layers and solar cells were fabricated by RF-PECVD in a UHV cluster tool deposition system using a gas mixture of silane and hydrogen. Trimethylborane and phosphine were added as doping gases for the deposition of p-type and n-type layers, respectively. The substrate temperature during the deposition was kept at a nominal temperature of 120 °C. Additionally, a standard temperature a-Si:H solar cell was prepared at a substrate temperature of 200 °C for comparison. More details on the deposition process can be found in [11]. Solar cells in p-i-n deposition sequence were prepared on commercially available Asahi-U type substrates with an absorber layer thickness of 450 nm or 150 nm. For p-side illuminated cells, the back contact is formed by evaporation of silver pads, which simultaneously define the cell area of 1 cm². Additionally, n-side illuminated cells were fabricated, where a thin layer of indium-doped tin oxide, covered with a small silver grid is used as front contact and the glass side of the Asahi-U type substrate is covered with silver to serve as back contact (see also [12] for additional details). Individual layers (a-Si:H p-, n- and i-types) with layer thickness between 350 to 500 nm were prepared on Corning Eagle XG glass substrates. Conductivities of individual layers were measured with evaporated coplanar silver contacts in vacuum. Photosensitivity $PS$ for the intrinsic absorber layer is defined as the ratio of photo ($\sigma_b$) to dark ($\sigma_d$) conductivity. The solar cells were characterized using a class A sun simulator for JV measurements under 100 mW/cm² AM1.5 illumination at a temperature of 25 °C. Fill factor (FF), open-circuit voltage ($V_{oc}$), short-circuit current density ($J_{sc}$) and efficiency ($\eta$) were evaluated from these JV curves. External
quantum efficiencies ($EQE$) were determined from the differential spectral response of the solar cell with and without external bias voltage of -0.5V. Annealing occurs, for both solar cells and silicon layers, in ambient air and/or high vacuum ($\sim 10^{-6}$ mbar) at a temperature $T_a$ of 120 °C for up to 150 minutes in steps of 30 minutes.

3. Results and Discussion

In the following, the effect of the post-deposition annealing on the solar cell performance is shown and discussed. In Fig. 1, relative $JV$ parameters, normalized to the as-deposited state, of three solar cells fabricated at different temperatures and on different substrates are shown as a function of annealing time: I) standard deposition temperature of 200 °C on glass (grey triangles), II) low deposition temperature of 120 °C on glass (black triangles) and III) low deposition temperature of 120 °C on PET (green circles). While the effect of annealing on the standard temperature solar cell on glass is rather low with only 2 % relative improvement in efficiency (Fig. 1(a)) after 120 minutes annealing, the effect on the low temperature (120 °C) solar cell is significant for all $JV$ parameters. The strongest improvement is evident for fill factor values in Fig. 1(c), with an increase of 21 ± 1 % relative after 120 minutes annealing. The reason for this is mainly a reduction in series resistance in the solar cell, decreasing from 19.5 $\Omega$ to 11.5 $\Omega$, while no distinct change in shunt resistance can be observed. $J_{sc}$ (Fig. 1(d)) and $V_{oc}$ (Fig. 1(b)) values are increased by 8 % and 4 %, respectively, resulting in a relative improvement in efficiency of 34 %. For the same cell on a flexible PET substrate, the improvement is even stronger for all $JV$ parameters. One can speculate that stronger improvement of the solar cell performance on PET substrate upon annealing could be related to a lower actual temperature of the PET substrate, which in turn, could result in poorer electronic quality of the solar cell materials and thus the solar cells on PET substrates may be more sensitive to post-deposition annealing.

Fig. 1. Relative $JV$ parameters, compared to the as-deposited state, as a function of annealing time for different solar cells: black triangles: 120 °C solar cell on glass substrate, grey triangles: 200 °C solar cell on glass substrate, green circles: 120 °C solar cell on PET substrate. The lines are guides to the eye.

Additional experiments (not shown here) indicate that the annealing effects are independent of the type of back or front contacts used in the cell (different TCO or TCO/Ag layers), and therefore the effects can solely be assigned to the changes within the silicon layer stack. Conductivities of the p-type and n-type layer, as well as the photosensitivity of the intrinsic layer are shown in Fig. 2. It can be seen from Fig. 2(a) and (b), that the dark conductivity of both p-type and n-type layer increases only slightly by a maximum factor of 3.2; from $1.9\cdot10^{-8}$ S/cm to $4.3\cdot10^{-8}$ S/cm and from $4.7\cdot10^{-4}$ S/cm to $1.5\cdot10^{-4}$ S/cm, respectively. The conductivity increase can be related to a shift in Fermi level position closer to the valence band in the case of p-type and closer to the conduction band in the
case of n-type layer, respectively. Electrical properties of relatively thick individual layers (with thickness between 350 nm to 500 nm) measured on glass substrates may not necessarily reflect the exact layer properties in the solar cell device, where much thinner layers with thickness below 20 nm are used. Nevertheless, we will assume that when such layers are used in the solar cells that this annealing induced Fermi level shift will result in a stronger built-in field in the solar cell. The photosensitivity of intrinsic a-Si:H can be related to the material quality of the layer, and photovoltaic devices showing high performance usually contain absorber layers with values $\geq 1 \cdot 10^5$. As shown in Fig. 2(c), the post-deposition annealing of the intrinsic absorber layer leads only to a small increase in photosensitivity from $4.2 \cdot 10^4$ to $7.9 \cdot 10^4$ after 120 minutes annealing. The assumed stronger built-in field, along with the slight improvement in material quality of the intrinsic absorber layer, can partly be responsible for the improvement in open-circuit voltage and fill factor upon annealing, as shown in Fig. 1 (b) and (c).

![Fig. 2. Dark conductivities of (a) p-type and (b) n-type amorphous silicon layer, as well as the photosensitivity of the intrinsic amorphous silicon layer (c) as a function of annealing time.](image)

Additional details on the effects of thermal treatment on $J_{SC}$ and also information on the collection efficiency in the solar cell devices can be obtained from $EQE$ measurements. The effect of annealing on $EQE$ curves of the a-Si:H solar cells is shown in Fig. 3(a). An increase over the whole wavelength range can be observed with annealing. The largest increase occurs within the first 30 minutes as also visible from the short circuit current density in Fig. 1(d). For more detailed information, normalized changes in the $EQE$ spectra are calculated by $EQE(t)/EQE$(as deposited) and plotted in Fig. 3(b). It can be seen that an improvement in $EQE$ curves with annealing occurs over the entire wavelength range, up to a factor of 1.3. Here, short wavelength light is to a great extent absorbed in the front part of the solar cell, and as the light enters through the p-layer, photogenerated electrons have to travel through the complete i-layer to the n-layer to get collected. Holes are easily collected in that case and therefore electron collection is limiting the current in the device. Qualitatively, an improvement of the $EQE$ in the short wavelength region (below 500 nm) therefore suggests that the collection of the photogenerated electrons, i.e. electron drift length $L_e$ in the absorber layer is improved with annealing. On the other hand, the increase of the $EQE$ in the long wavelength range suggests an increase in the drift length of holes that have to travel towards the p-layer to be collected. We note that the contribution of minority carriers is negligible in the conductivity measurements of the intrinsic samples where electrons are the majority carriers and therefore hole transport, and important for us, the improvement in hole transport properties cannot be detected by simple conductivity measurements.

Additional information on the electrical transport and charge carrier collection can be obtained from a
comparison of p- and n-side illuminated solar cells. Such an approach has been previously used to study the effects of electronic defects [13] or oxygen content [12] in the absorber layers on the performance of solar cells. The effect of annealing on EQE curves on the performance of n-side illuminated a-Si:H solar cells is shown in Fig. 4(a), and the corresponding normalized EQE curves are plotted in Fig. 4(b). It can be seen that stronger improvement in EQE upon annealing occurs at the short wavelength region (below 500 nm), up to a factor of 2.3. In contrast, EQE curves in the long wavelength region are weaker improved, by a maximum factor of 1.25, close to that of p-side illuminated solar cells. As the light enters through the n-layer, in this case holes are the carriers to travel through the entire absorber layer to be collected for short wavelength absorption. The far greater effect of annealing for the n-side illuminated cells in the short wavelength region, compared to the p-side illuminated cell, implicates that the changes in EQE curves with annealing are mainly limited by the collection of the of minority carriers.

Fig. 3. (a) absolute and (b) normalized external quantum efficiencies for different annealing times (as deposited, 30 min, 60 min, 120 min) for the p-side illuminated solar cell.
Fig. 4. (a) absolute and (b) normalized external quantum efficiencies for different annealing times (as deposited, 30 min, 60 min, 120 min) for the n-side illuminated solar cell.

We note that the charge carrier collection within the i-layer can be improved by (i) an increase in the mobility-lifetime product ($\mu\tau$-product) and/or by (ii) an increase in the built-in field in the device:

(i) A comparison of EQE curves of p- and n-side illuminated solar cells indicates much stronger improvement in n-side illuminated EQE upon annealing at the short wavelength region. This can be attributed to the improvement in i-layer properties upon annealing, namely mobility-lifetime product of the minority carriers.

(ii) The effect of changes in the built-in field in the devices can be evaluated by studying of EQE curves with additionally applied reversed voltage bias. Fig. 5 shows the ratio of $EQE$ with and without bias voltage of -0.5 V for different annealing times for the case of 450 nm thick p-side illuminated solar cell (shown in Fig. 3). It can be seen that the effect of reverse bias is reduced with annealing (from a factor of up to 1.15 in as deposited state down to a factor of 1.05 ± 0.03 after 120 min annealing time).

![Graph showing the ratio of EQE with and without reverse bias voltage for different annealing times.]

Fig. 5. Ratio of $EQE$ with and without bias voltage of -0.5 V for different annealing times.
The curves are qualitatively similar to Fig. 3(b), but with reduced magnitude of the changes, suggesting that the changes in EQE curves upon annealing result from both (i) changes in i-layer properties and (ii) an improvement in the built-in field in the device. Interestingly, in the case of thinner absorber layer, the effect of annealing is predominantly visible in the long-wavelength region, as shown in Fig. 6(a) for the case of 150 nm thick p-side illuminated solar cell, while only minor effect of the reverse bias occurs over the entire wavelength range. These results confirm the contribution of both effects upon annealing: the improvement in the collection of the minority carriers (i.e. due to changes in the $\mu$-$\tau$-product) and an increase in the built-in field in the device, which can have two possible reasons:

- Improvement in the electrical properties of doped layers due to a shift in Fermi levels and
- Improvement in the electronic quality (i.e. decreasing defect density) in the absorber layer. Both effects are in agreement with changes in the individual layers upon annealing shown in Fig. 2.

4. Conclusion

We have shown that a-Si:H solar cells deposited at a low temperature of 120 °C on both glass and flexible PET substrates are significantly improved upon annealing with increase in the efficiency up to 34 % (relative). While for the electrical properties of the individual silicon layers only slight improvement is detected, the comparison of p- and n-side illuminated solar cells suggests that an improvement in the hole collection is mainly responsible for the improvement in solar cells with annealing. The effects of reverse bias voltage and variation in the absorber layer thickness indicate that both the built-in field in the device, as well as the i-layer material quality, namely mobility-lifetime product, improve with the annealing treatment resulting in improved collection efficiency in the devices.

References


