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## Gate-defined quantum-dot devices realized in InGaAs/InP by incorporating a $HfO_2$ layer as gate dielectric

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Gate-defined quantum dots in an InGaAs/InP heterostructure are realized by incorporating a high- $\kappa$  HfO<sub>2</sub> material as a gate dielectric using atomic layer deposition. The fabricated quantum-dot devices show Coulomb blockade effect at low temperature. The Coulomb blockade current peaks are found to shift in pairs with the magnetic field applied perpendicular to the quantum-dot plane, due to the filling of electrons into spin-degenerate orbital states. When the magnetic field is applied parallel to the quantum-dot plane, spin splittings of orbital states are observed and the extracted effective g-factors are found to be different for different orbital states. © 2009 American Institute of Physics. [DOI: 10.1063/1.3077188]

Semiconductor quantum dots (QDs) are a subject of extensive research of today. These systems not only are of great interest for studies of basic physics, such as quantum many body and spin physics, <sup>1-3</sup> but also have potential applications in nanoelectronics and photonics. State of the art methods of fabricating semiconductor QDs include self-assembled growth, 5-7 scanning probe microscope oxidization, 8 wet 9 or dry<sup>10</sup> etching, lithographically patterning of top gates, 11–13 etc. In the employment of the lithographically patterning technology listed above, patterned metal gates are made on the surface of a semiconductor heterostructure. Application of negative voltages to the gates can deplete electrons beneath, creating an electron QD inside the heterostructure. High tunability, smooth confinement boundaries, and good device reproducibility make the patterning top-gate technology superior to several other methods in making QDs for studies of transport phenomena. So far, most top-gate defined QDs have been realized in GaAs/AlGaAs heterostructures. 11-14 However, top-gate defined QDs in InP based heterostructures have not been reported to date, although the heterostructures are promising material systems for applications in microelectronics<sup>15</sup> and optoelectronics<sup>16</sup> and, in particular, the InGaAs/InP two-dimensional electron gas (2DEG) system has interesting electron transport properties, such as small electron effective mass, high electron mobility, large effective g-factor, and strong spin-orbit coupling strength. 17-19 A well-known problem is that the metal/InP Schottky barrier height is too low (typically < 0.5 eV)<sup>20,21</sup> to suppress the leakage current of the gate.

In this letter, we report the realization of gate-defined QDs in an InGaAs/InP heterostructure by employment of a high- $\kappa$  material as a gate dielectric. Using atomic layer deposition (ALD), a thin HfO<sub>2</sub> layer is grown on the surface of the heterostructure prior to the deposition of a metal gate layer. The technology is first characterized with split-gate defined quantum point contact (QPC) devices and is then exploited to fabricate top-gate defined QDs in the heterostructure. The fabricated QD devices show Coulomb blockade effect at low temperature. It is observed that the conduc-

tance peaks shift in pairs with the magnetic field applied perpendicular to the 2DEG plane. When the magnetic field is applied parallel to the 2DEG plane, spin splittings of QD orbital states are observed and the effective *g*-factors are then extracted.

The wafer used in this work is a modulation-doped semiconductor heterostructure grown by metal-organic vapor phase epitaxy. On a semi-insulating InP:Fe substrate, a 50 nm thick undoped buffer layer, a 9 nm thick In<sub>0.75</sub>Ga<sub>0.25</sub>As quantum well, a 20 nm thick undoped InP layer, a 1 nm thick Si  $\delta$ -doped InP layer, and finally a 20 nm thick InP cap layer are grown epitaxially. At 300 mK, the sheet electron concentration, mobility, and mean free path in the InGaAs quantum well are  $4.2 \times 10^{15}$  m<sup>-2</sup>, 6.77 m<sup>2</sup>/V s, and 725 nm, respectively, determined by Hall measurements in dark. Standard mesas with annealed Au/Ge Ohmic contacts are fabricated by two steps of electron-beam lithography. To obtain a clean and insulating heterostructure surface prior to growth of HfO<sub>2</sub>, the sample is etched in diluted HF acid (HF:H<sub>2</sub>O =1:4) for 20 min followed by sulfur passivation in solution of  $[(NH_4)_2S_x: H_2O=1:9]$  at 60 °C for 20 min. A nominal 24 nm thick (300 cycles) HfO<sub>2</sub> film is grown on the pretreated surface from hafnium tetrakis(dimethylamide) Hf[N(CH<sub>3</sub>)<sub>2</sub>]<sub>4</sub> and water<sup>22</sup> in a Savannah 100 ALD system at 300 °C. Although the Ohmic contact pads are covered by the HfO2, the forces generated by a standard thermosonic wire bonder allow metal to penetrate through the thin HfO2 film and connect the Ohmic contact pads of the device to the outside electrodes. Therefore, no patterning (etching or lift-off) process of the HfO<sub>2</sub> layer is needed. Finally, the top gates are fabricated by a third step of electron beam lithography and thermal evaporation of a 50 nm thick Ti/Au metal layer. It is worth noting that the InP native oxide can result in electrical instabilities at the insulator/InP interface<sup>23</sup> and, thus, proper pretreatment of the InP surface<sup>24</sup> prior to an ALD process is essential.

The technology is evaluated using split-gate devices fabricated with the above procedure of processes. The inset in Fig. 1 shows an atomic force microscope (AFM) image of a typical split-gate structure fabricated on the surface of the InGaAs/InP heterostructure. The lithographically defined opening of the split gate is about 150 nm wide. Negative

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FIG. 1. (Color online) Linear-response conductance G of a gate-defined QPC in an InGaAs/InP heterostructure measured against the split-gate voltage  $V_g$  at 4.2 K. The inset shows an AFM image of the QPC device and a schematic diagram of the measurement circuit.

voltage  $V_g$  is applied to the split gate to form a QPC in the InGaAs quantum well and the width of the conduction channel of the QPC can be tuned by varying the applied gate voltage. Electrical measurements show that the breakdown field of the  $HfO_2$  film is  $\geq 4$  MV/cm and, under normal device operation conditions, the gate leakage current density is in the order of  $10^{-8}$ – $10^{-7}$  A/cm<sup>2</sup>. The dielectric constant  $\kappa$  of as-grown HfO<sub>2</sub> film is known to be approximately 15,<sup>25</sup> much larger than the value of 3.9 for SiO<sub>2</sub>. Figure 1 shows the linear-response conductance G of the QPC measured at 4.2 K as a function of the gate voltage  $V_g$  using standard lock-in technique. In Fig. 1, the conductance quantization with several well defined steps is observed, revealing a signature of quantum and ballistic transport effect in the fabricated split-gate device. The results show excellent dielectric properties of as-grown HfO2 films, through which smooth potentials are achieved by gating, confirming the feasibility of the device fabrication technology.

An InGaAs/InP QD device fabricated with the above developed technology is shown in the inset in Fig. 2(a). The QD is defined by four surrounding gates, i.e., left, plunger, right, and cross-bar gate. Static voltages applied to the four gates are denoted by  $V_l$ ,  $V_p$ ,  $V_r$ , and  $V_{cr}$ , respectively. The lithographically defined structure of the QD is square shaped and has a nominal size of 250 nm. A dc voltage  $V_{\rm sd}$  is applied between the source and drain of the device in a symmetric configuration, with  $V_d$ =+ $V_{\rm sd}$ /2 and  $V_s$ =- $V_{\rm sd}$ /2. Transport

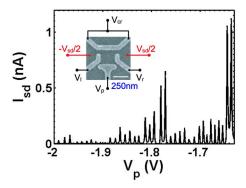


FIG. 2. (Color online) Source-drain current  $I_{\rm sd}$  vs plunger gate voltage  $V_p$  measured for a QD in InGaAs/InP defined by setting other gate voltages at values of  $V_r$ =-1.66,  $V_r$ =-1.59, and  $V_{cr}$ =-1.58 V. The inset shows the scanning electron microscope image of the QD device and a schematic diagram of the measurement setup. The device is measured at 300 mK with  $V_{\rm sd}$ =50  $\mu$ V.

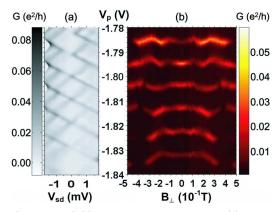


FIG. 3. (Color online) (a) Charge stability diagram and (b) magnetic-field evolution of the Coulomb blockade peaks of a gate-defined QD device (see text for details). In (a) the differential conductance is plotted as a function of  $V_{\rm sd}$  and  $V_p$  and in (b) the linear-response conductance is plotted as a function of  $V_p$  and the perpendicular magnetic field  $B_{\perp}$ .

properties of the QD are measured at 300 mK in a <sup>3</sup>He based cryostat.

Figure 2(a) shows the measured current  $I_{sd}$  through the QD as a function of the plunger gate voltage  $V_p$  at  $V_{\rm sd}$ =50  $\mu$ V. The QD is defined by applying voltages  $V_l = -1.66$ ,  $V_r = -1.59$ , and  $V_{cr} = -1.58$  V to the left, right, and cross-bar gate, respectively. Sharp Coulomb blockade current peaks are observed. The spacing between peaks is almost constant, indicating the system is in the manyelectron transport regime. The irregularity in peak amplitude is due to the variations in quantum level spacing and QD-2DEG reservoir couplings. <sup>26</sup> Similar Coulomb blockade current oscillations can be observed by sweeping  $V_l$ ,  $V_r$ , or  $V_{cr}$ instead with other gate voltages fixed at constant values. In the linear-response regime, the capacitance of a gate to the QD,  $C_g$ , can be calculated via  $C_g = e/\Delta V_g$ , where e is the electron charge and  $\Delta V_g$  is the gate voltage difference between two neighboring Coulomb peaks. In this way, the capacitances of the four gates to the QD are determined to be  $C_p = 15.86$ ,  $C_l = 16.35$ ,  $C_r = 12.14$ , and  $C_{cr} = 21.36$  aF.

Figure 3(a) shows a charge stability diagram of the QD, where the differential conductance is plotted as a function of the source-drain bias  $V_{\rm sd}$  and the plunger gate voltage  $V_p$ , with gate voltages  $V_l$ ,  $V_r$ , and  $V_{cr}$  being fixed at constant values of -1.62, -1.62, and -1.59 V. In the diamondshaped areas (Coulomb blockade regions) in Fig. 3(a), the electron transport is blocked and the number of electrons in the dot is fixed at integer numbers. The single electron charging energy of the dot is about 1.1 meV (half of the width of a diamond), which leads to a total capacitance of the QD of  $C_{\Sigma}$  = 145 aF. If we assume the QD structure to be a disk, the capacitance can be expressed as  $C_{\Sigma}=4\kappa\kappa_0 d$ , where  $\kappa$  and  $\kappa_0$ are dielectric constants of InGaAs and vacuum and d is the size of the QD. The electric size d of the QD can be estimated to be about 280 nm, comparable to the structure size defined lithographically. Figure 3(b) shows the evolution of the conductance peaks with the applied magnetic field. Here, the field  $B_{\perp}$  is applied perpendicularly to the 2DEG plane. The evolution of the conductance peaks is seen to show pronounced "wiggles." The effect is attributed to magnetic field induced crossings between QD orbital levels. We have further found that the peaks generally shift in pairs with the magnetic field  $B_{\perp}$ . We attribute this phenomenon to the filling of electrons into two spin states of orbital levels in

FIG. 4. (Color online) (a) Charge stability diagram and (b) magnetic-field evolution of the Coulomb blockade peaks of a gate-defined QD device (see text for details). In (a) the differential conductance is plotted as a function of  $V_{\rm sd}$  and  $V_p$  and in (b) the linear-response conductance is plotted as a function of  $V_p$  and the parallel magnetic field  $B_{\parallel}$ .

the QD. Similar phenomena have been observed in  $In_{0.05}Ga_{0.95}As/Al_{0.22}Ga_{0.78}As$  QDs but at one order of magnitude larger magnetic fields  $B_{\perp}$ .<sup>27</sup>

Figure 4 shows the measurements of the same device as in Fig. 3, but with the magnetic field  $B_{\parallel}$  being applied parallel to the 2DEG plane, after another cooling down. Figure 4(a) shows the charge stability diagram of the QD formed in a voltage configuration of  $V_{\rm sd}$ =50  $\mu$ V,  $V_l$ =-1.66,  $V_r$ = -1.59, and  $V_{cr}=-1.58$  V. It is seen from Fig. 4(a) that the plunger gate capacitance and the charging energy are almost the same as those in Fig. 3(a). Figure 4(b) shows the evolution of the conductance peaks of the QD with  $B_{\parallel}$ . Since the field is parallel to the 2DEG plane, the influence of magnetic-field induced level interactions is expected to be small. Thus, the observed phenomenon in Fig. 4(b) arises mainly from the material properties of the heterostructure. In the measurements, the energy difference between two adjacent conductance peaks can be obtained from  $\Delta \mu(B)$  $=\alpha_p e \Delta V_p$ , where  $\alpha_p = C_p / C_{\Sigma}$  is the plunger gate lever arm and  $\Delta V_p$  is the corresponding difference in the voltage applied to the plunger gate. In the constant interaction model, we have  $\Delta \mu(B) = e^2 / C_{\Sigma} + \Delta \epsilon(B)$ , where  $\Delta \epsilon(B)$  is the energy difference between quantum states involved in tunneling at the zero source-drain bias. For odd spin filling one expects  $\Delta \epsilon(B) = |g_n^* \mu_B B|$ , while for even spin filling  $\Delta \epsilon(0) > 0$  and  $\Delta \epsilon(B) = \Delta \epsilon(0) - |g_n^* \mu_B B|/2 - |g_{n+1}^* \mu_B B|/2$ . Here  $\mu_B$  is the Bohr magneton, n and n+1 are the indices of the levels being filled on the Coulomb peaks below and above the corresponding diamond, and  $g_n^*$  is the effective g-factor of quantum level n. The g-factor can be different for different quantum levels.<sup>28,29</sup> By fitting of the data in Fig. 4(b), we obtain g-factors for three quantum states,  $|g_{m+1}^*| = 0.90$ ,  $|g_{m+2}^*| = 1.83$ , and  $|g_{m+3}^*| = 2.08$ . Values of  $|g^*| \approx 4$  have been extracted for InGaAs/InP quantum wells in an applied perpendicular magnetic field configuration.<sup>30</sup> Our extracted g-factors are smaller than these out-of-plane g-factors but are fully comparable to the values determined in an optically detected magnetic resonance experiment  $^{31}$  in which values of  $|g^*|$ ≈2 have been extracted for an InGaAs/InP quantum well with a magnetic field applied parallel to the quantum-well plane.

In summary, we have developed a technology of fabricating gate-defined QD devices in InGaAs/InP by incorporating a HfO<sub>2</sub> thin film. Coulomb blockade effect has been observed in the fabricated devices at low temperature. It has also been observed that when a magnetic field is applied perpendicular to the QD plane, the conductance peaks shift in pairs with the magnetic field. However, when the magnetic field is applied parallel to the 2DEG plane, spin splittings of QD orbital states have been observed and the extracted effective g-factors are found to vary with the QD orbital state.

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