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Nanometer patterning of epitaxial $CoSi_2$/Si(100) for ultrashort channel Schottky barrier metal–oxide–semiconductor field effect transistors

Q. T. Zhao,[a] F. Klinkhammer, M. Dolle, L. Kappius, and S. Mantl
Institut für Schicht- und Ionentechnik (ISI-IT), Forschungszentrum Jülich, D-52425 Jülich, Germany

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A nanometer patterning method, based on local oxidation of silicide layers, was used to pattern epitaxial $CoSi_2$ layers. A feature size as small as 50 nm was obtained for 20 nm epitaxial $CoSi_2$ layers on Si(100) after patterning by local rapid thermal oxidation in dry oxygen. A Schottky source/drain metal–oxide–semiconductor field effect transistor with epitaxial $CoSi_2$ on *p*-Si(100) was fabricated using this nanopatterning method to make the 100 nm gate. The device shows good I–V characteristics at 300 K. © *1999 American Institute of Physics.* [S0003-6951(99)02503-6]

Downscaling of microelectronic devices is primarily hampered by the size of the source and drain contacts. Conventional metal–oxide–semiconductor field effect transistors (MOSFETs) use ohmic source and drain contacts to the ion implanted silicon. Replacing these contacts by silicides which form Schottky contacts at source and drain allows a considerable reduction of the contact areas because of the much lower series resistance per unit area. This issue becomes even more important for nanoscaled MOSFETs, where the carriers are injected from the contacts to the channel.[1] Simulations show that the MOSFETs with Schottky contacts at source and drain are promising devices with ultrashort gate lengths.[2] So far, the shortest gate length of the Schottky barrier MOSFETs (SB-MOSFETs) reported is 0.25 μm patterned by electron-beam lithography of silicon,[3] and polycrystalline silicides were used as the Schottky contacts at source and drain.[3,4]

Epitaxial silicide, such as $CoSi_2$, has superior properties as compared to the polycrystalline silicides due to the excellent interface sharpness and the lack of grain boundaries. As the feature size of the devices decreases to nanometer, these properties play a more important role. Nanopatterned epitaxial silicides provide a new approach to the future silicon nanoelectronics.[5] Patterning of the silicide nanostructures, however, is very difficult because of the need of electron-beam lithography and the lack of suitable gases for reactive ion etching. In this letter we used a new silicide nanometer patterning method to fabricate the ultrashort (<100 nm) gate structures for the SB-MOSFETs. This patterning method, as reported elsewhere,[6,7] is based on local oxidation of silicide (LOCOS) layers. It is similar to the well known local oxidation of silicon (LOCOS) technique which is used to form the field oxides for MOSFETs.

Epitaxial $CoSi_2$ layers with a thickness of 20 nm were grown by molecular beam allotaxy (MBA) after growth of 140 nm Si buffer layers on floating zone phosphorus doped Si(100) (>1 kΩ cm) substrates.[8,9] The MeV He ion channeling measurements have shown that the $CoSi_2$ layers have a high crystalline quality with minimum yields of 4%. Their specific electrical resistivity was measured to be 14 $\mu\Omega$ cm at room temperature. The nanometer patterning of the $CoSi_2$ layers based on LOCOSI involves two key steps. First, a conventional oxidation mask of 20 nm SiO_2 and 300 nm Si_3N_4 was deposited by plasma enhanced chemical vapor deposition (PECVD) and patterned along ⟨110⟩ directions by optical lithography and dry etching. Second, rapid thermal oxidation (RTO) was performed in dry oxygen. The patterned structures were investigated by cross-sectional transmission electron microscopy (XTEM) and scanning electron microscopy (SEM). For fabrication of the devices, the buffer layer of Si was doped by B ion implantation and rapid thermal annealing to form a uniform *p*-type doping layer with a concentration of 1×10^{17} B/cm^3.

Figure 1 shows the XTEM micrographs of a 20 nm epitaxial $CoSi_2$ layer on Si(100) patterned after RTO at 950 °C for Fig. 1(a) 1 min, and Fig. 1(b) 3 min. The originally continuous silicide layer is separated near the edge of the

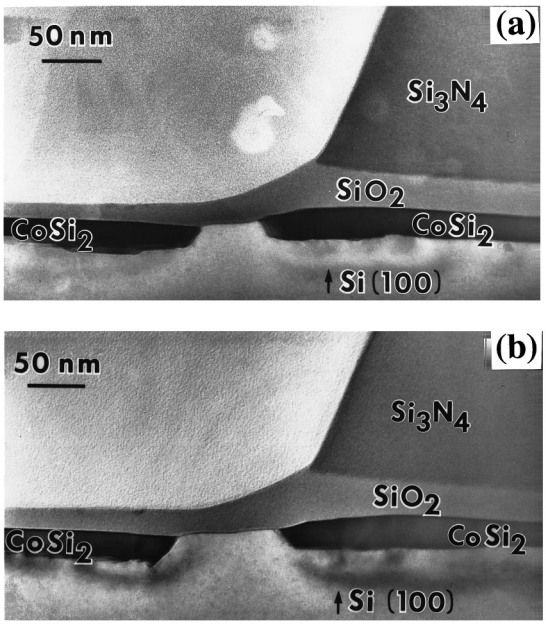

FIG. 1. XTEM micrographs of a 20 nm epitaxial $CoSi_2$ patterned by LOCOSI at 950 °C for (a) 1 min, and (b) 3 min. The gaps between the silicide layers are 50 and 90 nm for the cases of (a) and (b), respectively.

[a]Electronic mail: q.zhao@fz-juelich.de

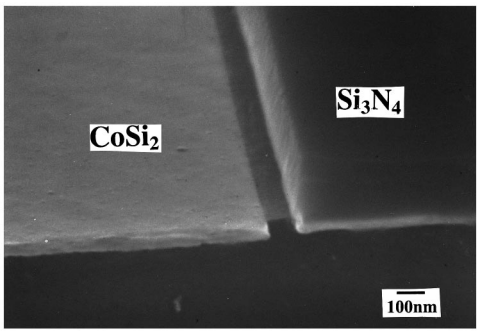

FIG. 2. SEM image for the sample of Fig. 1(b) after oxide removal, indicating good uniformity of the 90 nm gap.

nitride mask with a gap of 50, and 90 nm for the case of Figs. 1(a) and 1(b), respectively. In the unprotected regions SiO_2 formed on top of $CoSi_2$ layer. The breakdown fields of SiO_2 layers on $CoSi_2$ were measured to be 5–8 MV/cm approaching nearly the quality of thermal oxide on silicon. During RTO the oxidant (O_2) diffuses to the $SiO_2/CoSi_2$ interface where two chemical reactions take place: the dissociation of $CoSi_2$ and the oxidation of silicon. The excess Co diffuses through the silicide layer to the lower $CoSi_2/Si$ interface to form $CoSi_2$ again, while the excess Si forms SiO_2. The latter process gives rise to the growth of the typical SiO_2 ''bird's beak'' underneath the edge of the nitride mask. The vertical displacements of $CoSi_2$ layers are less than 10 nm in Fig. 1. This is a great advantage, since the structure remains nearly planar, in contrast to the large vertical distances (>100 nm) in Refs. 6 and 7 for thicker silicide layers. Patterning of thin $CoSi_2$ layers in this work also needs a smaller thermal budget as compared to thick silicide layers.

For applications a high lateral uniformity of the gap is necessary. In order to investigate the lateral uniformity of the separation, the oxide was removed by buffered HF etching. A typical resulting structure is shown in a SEM micrograph of Fig. 2 for the 20 nm $CoSi_2$ layer patterned by LOCOSI at 950 °C for 3 min. We can see that the gap of 90 nm is highly uniform. We found that the stress generated by the oxidation masks plays a key role in this patterning process. A Monte Carlo simulation, considering the stress dependence of the dissociation of $CoSi_2$ and the oxidation of Si at the $SiO_2/CoSi_2$ interface as well as the stress dependent diffusion of Co, has been established. It could be shown that the simulation predicts well the evolution of the micrographs during local oxidation.[10]

The structure shown in Fig. 1 is the base for the fabrication of the ultrashort channel SB-MOSFET. One silicide region is used as source, the other one as drain. The ultrashort channel gate length was defined by this new technique, instead of e-beam lithography. Figure 3 shows the transistor fabrication process. In the first step silicide wires with two silicide contact pads were made [Fig. 3(a)]. Then an oxidation mask was patterned and aligned so that half the structures were covered [Fig. 3(b)]. Subsequent RTO in dry oxygen at 950 °C for 5 min produced a 100 nm wide gap in the silicide wire, near the edge of the oxidation mask [Fig. 3(c)]. The silicon gap is now covered with ≈ 30 nm SiO_2 which served as the gate oxide. Finally, metallizations of gate, source, and drain were made by optical lithography and

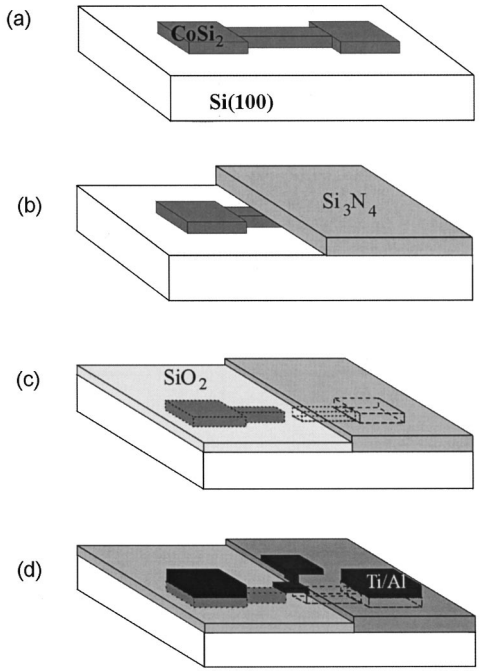

FIG. 3. Device fabrication process: (a) patterning of silicide wires, (b) patterning of the oxidation mask, (c) local oxidation of the silicide wire, (d) metallization of gate, source, and drain contacts.

liftoff of 20 nm Ti/300 nm Al [Fig. 3(d)]. Figure 4 shows the I–V characteristics measured from the two separated areas [i.e., from the source and drain contacts in Fig. 3(d) with zero gate bias] of $CoSi_2$ wires with sizes of 80×180 and $100\times400\ \mu$m, as indicated in the figure, after RTO at 950 °C for 5 min. The curves show typical I–V behavior of two reversibly biased Schottky diodes. According to Ref. 11, the Schottky barrier height and the ideality factor can be approximately calculated from the reversed I–V curves with the following equations for the voltage $V>3k_BT/q$:

$$I=-I_s\exp(qV/n'k_BT),$$

$$I_s\approx AA^*T^2\exp(-q\phi_b/k_BT),$$

where q is the electron charge, k_B is the Boltzmann constant, T is the measurement temperature in K, A is the Schottky contact area in cm^{-2}. The Schottky contact areas are 80×90 and $100\times200\ \mu m^2$, respectively, because of the

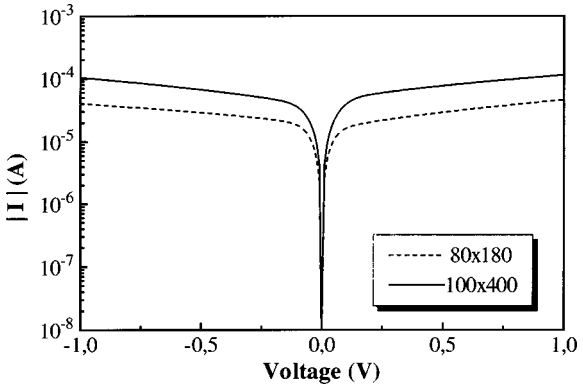

FIG. 4. I–V characteristics measured from the two separated parts [i.e., from source and drain areas in Fig. 3(d) with zero gate bias] of $CoSi_2$ wires with sizes of $80\times180\ \mu$m and $100\times400\ \mu$m after RTO, showing two reversibly biased Schottky diodes.

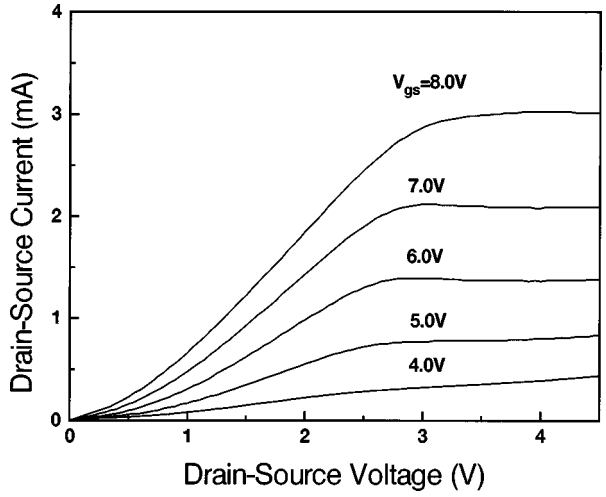

FIG. 5. *I–V* characteristics of an *n*-channel Schottky barrier MOSFET with a gate length of 100 nm at 300 K. Source and drain contacts are made with 20 nm thick epitaxial $CoSi_2$ on Si(100).

separation of the $CoSi_2$ wires near the edges of nitride mask after RTO. A^* is the effective Richardson constant ($\approx 32\ \mathrm{A\,cm^{-2}\,K^{-2}}$ for *p*-Si substrate), and ϕ_b is the Schottky barrier height. $n'^{-1}=1-n^{-1}$. Here n is the ideality factor for forward bias. From the two curves in Fig. 4, the Schottky barrier height of $CoSi_2$ for *p*-Si is calculated to be 0.42 eV, and the ideality factor n is 1.03 indicating a good $CoSi_2$/Si interface after RTO.

Figure 5 shows the output characteristics at 300 K of an n-channel SB-MOSFET with a channel length of 100 nm and a gate width of 50 μm. The drain and source contact areas are $80\times 80\ \mu\mathrm{m}^2$. The *I–V* characteristics show the typical SB-MOSFET behavior. The drain current increases slowly at low drain-source bias because the carriers cannot pass the Schottky barrier. As soon as the electrons overcome the barrier, they are injected into the channel and a normal transistor behavior and saturation are observed. The performance of the device can be further improved by reducing the gate oxide thickness and the drain and source contact areas, and by replacing the metal gate by polysilicon contact. Even smaller channel lengths seem feasible with this new technique.

In conclusion, a nanometer patterning method for thin epitaxial $CoSi_2$ layers based on local oxidation was investigated. Separation of $CoSi_2$ layers takes place near the edge of the nitride mask during rapid thermal oxidation. Highly uniform gaps as small as 50 nm between the protected and unprotected $CoSi_2$ layers were fabricated. The vertical displacements of the oxidized part amounts to less than 10 nm. This technique was used to fabricate ultrashort channel SB-MOSFETs. A Schottky barrier n-MOSFET with a gate length of 100 nm was fabricated using this technique, and it shows good *I–V* characteristics at 300 K. Further investigations of the devices are under development.

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