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Reliability analysis of the low resistance state stability of $Ge_{0.3}Se_{0.7}$ based solid electrolyte nonvolatile memory cells

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We report on the low resistance state (LRS) stability analysis of $Ge_{0.3}Se_{0.7}$ based solid electrolyte nonvolatile memory cells under elevated temperature and bias current stress conditions. The activation energy was found to be about 1.02 eV, which is comparable to that of an electromigration-induced failure process. Experimental results also show that there is trade-off between the LRS stability and the thickness of $Ge_{0.3}Se_{0.7}$ layer. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3103555]

Resistance random access memory (ReRAM) is one of the competitors for emerging nonvolatile memories such as, for example, the magnetic random access memory, the phase-change memory, and the ferroelectric random access memory.[1] ReRAM cells are based on various materials such as organic compounds,[2] transition metal oxides,[3–5] and ion conducting solid electrolytes,[6,7] which show resistance switching phenomena when sandwiched between suitable metal electrodes. In recent years, resistance switching cells based on ion conducting solid electrolytes have been extensively studied due to their promising features of low power consumption, high switching speed, and scalability. Whereas the switching mechanism of oxide materials is still under debate, it seems to be reasonably well understood in the case of ion conducting solid electrolytes assuming electrochemical growth and rupture of metallic filaments. Endurance of more than 10^{10} cycles, high data retention, and switching in the nanoampere range have already been demonstrated.[8,9] The integration of these materials in future nonvolatile ReRAM and logic devices will, however, not only rely on the excellent electrical properties but also on the reliability. One of the major reliability issues for ReRAM and logic devices is data retention, which is defined as the ability of a memory cell to retain stored data between the time for writing and subsequent reading of the stored information. Temperature and parasitic current could significantly accelerate the retention failure process for memory and crossbar array based logic devices. Surprisingly, very little has been explored on the reliability of these memory devices under constant current stress conditions.[10]

In this letter, we present an investigation on the stability of the low resistance state (LRS) of $Ge_{0.3}Se_{0.7}$(Cu) based memory devices under constant current stress conditions. A constant current stress was applied to memory cells in the LRS at room temperature as well as elevated temperatures and the statistical distribution of the measured time-to-switch off t_{sw} was determined in order to get an insight into the degradation mechanism of the device characteristics. Devices with active areas ranging from 2 to 150 μm^2 were fabricated as single cross-point structures using standard photolithography techniques. The detailed layer sequence of the memory devices as used in this study was the following: Si/SiO_x substrate/5 nm TiO_2/30 nm Pt (bottom electrode)/2–3 nm $SiO_x/Ge_{0.3}Se_{0.7}$/100 nm Cu (top electrode). More details on the fabrication process of the memory devices and their resistance switching properties can be found in Ref. 11 and 12. The reliability analysis was performed by monitoring the voltage change under constant current stress of memory cells which were initially voltage-programmed to the LRS by imposing a current compliance of 100 μA. All measurements were done using an Agilent B1500 semiconductor parameter analyzer.

The memory cell resistances in the LRS were found to be randomly distributed around 1 kΩ independent of the memory cell active area and the thickness of the $Ge_{0.3}Se_{0.7}$ thin film. Figure 1 shows the resistance versus time characteristic of a memory cell integrated with 70 nm $Ge_{0.3}Se_{0.7}$ under a constant current stress of −30 μA at room temperature. As the resistances in the LRS exhibited a random distribution, we act on the assumption that data loss or—more precisely—the "switch off" events will also obey some statistics. Furthermore, it can be clearly seen from Fig. 1 that several small sudden jumps already appear before the final switch off. We believe that the electrochemical dissolution of a filament is closely related to classical "weakest-link" type of problems in solid state physics such as breakdown of thin oxides and random resistor networks which have been extensively studied by means of percolation models in literature.[13,14]

In order to find out the statistical distribution of the time-to-switch off t_{sw} constant current stress at different ampli-

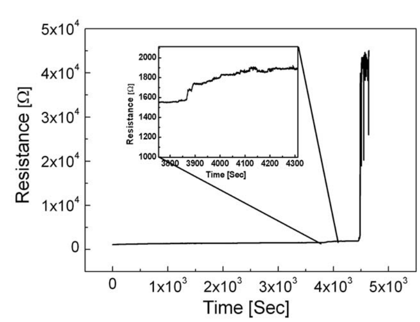

FIG. 1. Resistance evolution of a memory cell under a current stress of −30 μA at room temperature.

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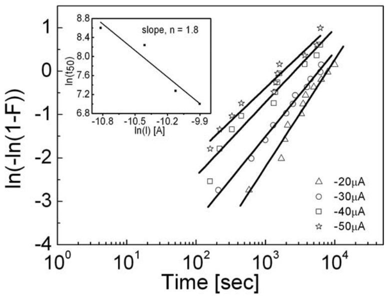

FIG. 2. Weibull plots of the cumulative time-to-switch off (t_{sw}) distributions for memory cells with a 70 nm $Ge_{0.3}Se_{0.7}$ film at different constant current stresses. The inset shows the MTF (t_{50}) as a function of current stress to determine the current exponent n.

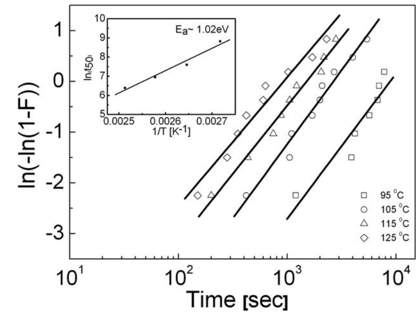

FIG. 3. Weibull plots of the cumulative time-to-switch off (t_{sw}) distributions for memory cells with a 70 nm $Ge_{0.3}Se_{0.7}$ thin film at different temperatures (constant current stress: -20 μA). The inset shows the Arrhenius plot for the MTF $\ln(t_{50})$.

tudes was applied to memory cells with a 70 nm $Ge_{0.3}Se_{0.7}$ integrated thin film in the LRS. A maximum measurement time of 10^4 s was set for all experiments. A resistance increase of one order of magnitude was specified as the failure criterion throughout the study. Figure 2 shows the cumulative distribution of the measured t_{sw} for different current stresses fitted with a Weibull function. Note that the distribution appears as a straight line in the Weibull plot. The statistical distribution of failure processes which result from weakest-link type of effects where many small defect sites compete with each other to be the one that causes the first failure can typically be described by means of the Weibull function[13,15]

$$F(t) = 1 - \exp[-(t/\tau)^{\beta}]. \quad (1)$$

Here, F is the cumulative failure probability, where τ is the characteristic failure time for $F=0.63$ and β the slope parameter of the distribution. The slope parameter represents the slope of a straight line which is obtained by plotting $\ln[-\ln(1-F)]$ for a Weibull distribution against $\ln(t)$. The slope parameter is an important factor in reliability analysis. A low value of the slope parameter indicates a strong reduction of the retention time. We observed that the slope parameter depends on the current stress value and decreases with increasing current stress: β=2.5, 1.95, 1.7, and 1.5 for -20, -30, -40, and -50 μA, respectively. While the physical reasons for the failure process and its relation to the time-to-switch off probability distribution are not fully understood at present, it is likely that under constant current stress different physical factors such as joule heating effects, electromigration, local electric field strength, and redox processes at weak points of the filament could simultaneously play an important role. As $\beta > 1$, we conclude that the degradation process is of intrinsic nature.

To get more insight, the degradation of the LRS with current density and temperature was studied by using Black's equation[16] based on the mean time to failure (MTF),

$$t_{50}(\mathrm{MTF}) = A j^{-n} \exp(E_a/k_B T), \quad (2)$$

where A is a constant, j is the current density, n is the current exponent, E_a is the activation energy, k_B is the Boltzmann constant, and T is the operating temperature. The value of n characterizes the role of the current density in the degradation process and values $n > 2$ have been attributed to joule heating effects.[17] Within the range of the current stress chosen in our experimental study, we found $n \sim 1.8$, as shown in the inset of Fig. 2. In principle, our evaluation should be based upon the current density along the conducting filamentary structure which might change during the stressing experiment. Thus, the local current density might alter in course of the experiment due to local shrinkage of the effective filament diameter. We think, however, that the local current density will always scale with the total applied current so that we can rely on the current as the characterizing parameter.

As has been extensively pointed out in literature, values of n in the range of 1–2 might indicate electromigration-induced failure processes.[17] Our observation, $n < 2$, is another evidence that joule heating is not the essential mechanism for the degradation. Joule heating does not seem to play an essential role as one has to reverse the polarity of the applied current to disrupt the filament after forming. Nevertheless, a slight increase in temperature which indirectly affects the degradation process cannot be ruled out.

The activation energy in Black's equation is another important parameter to verify a possible mass transport electromigration process. Therefore, we have determined the t_{sw} distributions under a constant current stress of -20 μA at different temperatures for a 70 nm $Ge_{0.3}Se_{0.7}$ film integrated in cross-point structures. The Cu top electrode was covered with a 30 nm sputtered Pt film to prevent oxidation at higher temperatures. Figure 3 shows Weibull plots of the cumulative failure distribution as a function $\ln(t_{sw})$ for different temperatures. As can be seen, nearly the same slope parameter, β =2.5, is found, indicating that the underlying failure process does not change within the temperature range examined. The activation energy for the mass transport was calculated from an Arrhenius plot of the MTF t_{50}, as shown in the inset of Fig. 3. The obtained value, E_a=1.02 eV, might be associated with Cu mass transport electromigration-induced failure processes.[17]

The stability of the LRS state of memory cells with different $Ge_{0.3}Se_{0.7}$ film thicknesses was studied under a constant current stress of -20 μA at room temperature. Figure 4 shows the Weibull plots of the cumulative failure distribution for $Ge_{0.3}Se_{0.7}$ films with thicknesses ranging from 30 to 70 nm. We cannot find any difference in the slope parameter β for different thicknesses under the same constant current stress. The characteristic failure time τ increases with increasing thickness which indicates that more extended and longer filamentary structures are more stable under the same stress conditions. As mentioned above, the memory cell resistances in the LRS were found to be independent of the active $Ge_{0.3}Se_{0.7}$ layer thickness 30–70 nm. Recently, Inoue

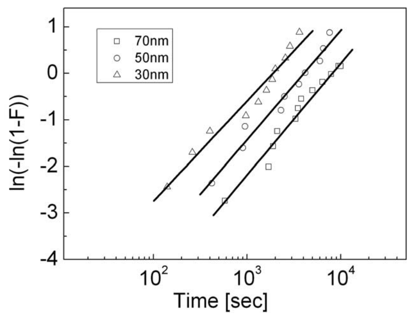

FIG. 4. Weibull plots of the cumulative time-to-switch off (t_{sw}) distributions for memory cells with different $Ge_{0.3}Se_{0.7}$ active layer thicknesses at room temperature (constant current stress: -20 μA).

et al.[18] proposed a switching model for memory cells made of various oxides which is based on an "electric faucet" at the electrode-active layer interface suggesting that resistance switching is due to opening and closing of the faucet without a considerable role of the conduction behavior in the bulk. If that would be the case for our material system, this model could indeed explain the thickness independent resistances observed in our study, but then we would not expect such a clear dependence of the characteristic failure time on the film thickness.

The best possible explanation from our point of view is the self sustained growth behavior of the filament (aggregation and reduction of migrating Cu ions), its fractal characteristics,[19,20] and submetallic behavior (not presented here). One has thus to consider the overall extension of the fractal filamentary structure within the active layer which will be larger for thicker films; thus resulting in comparable resistance values. The tip of the filament could be one the most favorable points for the breakdown and its size may scale with the filament growth. We think, however, that the potential distribution across the whole structure (especially at the dead ends) might take place in such a way that it leads to nearly the same resistance values in the LRS for different $Ge_{0.3}Se_{0.7}$ layer thicknesses.[21] We cannot exclude, however, that the resistances in the LRS will show some scaling behavior with further increase in thickness.

From the theory of the electromigration processes, one knows that the diffusion of atoms in the presence of a high current density arises from the momentum transfer of conduction electrons to defects (electron-wind force) and the direct action of an external electric field on charged defects (direct force).[22] The electron-wind force is proportional to the local current density and the direct force is proportional to the electric field strength at the defect sites. Inside the filamentary structure both forces are expected to decrease with decreasing the potential drop because the current density is proportional to the local potential drop.[22] Qualitatively, local potential drop is likely to decrease with the increase in the filament length thus making it more immune to electromigration-induced degradation processes as well as electrochemical dissolution.

In summary, the stability of the LRS of $Ge_{0.3}Se_{0.7}$ based resistance switching memory cells was studied under accelerated current and temperature stress conditions within the framework of the Weibull statistics. The Weibull slope parameter of the time-to-switch off distributions is controlled by the current stress but not by the thickness of the integrated $Ge_{0.3}Se_{0.7}$ film. We found the Weibull slope parameter to decrease with an increase in current stress but to remain unchanged with the $Ge_{0.3}Se_{0.7}$ thickness variation. The calculated current exponent $n \approx 1.8$ and activation energy $E_a = 1.02$ eV suggest that electromigration could be the main reason for the degradation of the LRS. The small value of the characteristic failure time for thinner integrated $Ge_{0.3}Se_{0.7}$ thin films could be an important issue with respect to the integration point of view for subnanoscale memory and logic devices.

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