Ternary rare-earth metal oxide high-*k* layers on silicon oxide

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Ternary oxides, $GdScO_3$, $DyScO_3$, and $LaScO_3$, deposited by pulsed laser deposition using ceramics targets of stoichiometric composition, were studied as alternative high-*k* gate dielectrics on (100) Si. Their physical characterization was done using Rutherford backscattering, spectroscopic ellipsometry, x-ray diffraction, and transmission electron microscopy on blanket layers deposited on (100) Si, and electrical characterization on capacitors. It is found that $DyScO_3$ and $GdScO_3$ preserve their amorphous phases up to 1000 °C. Other encouraging properties for high *k* applications were demonstrated, including *k*-value ~22, almost no hysteresis or frequency dispersion in $C-V$ curves, and leakage current reduction comparable to that of HfO_2 of the same equivalent oxide thickness. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1886249]

High-*k* materials have been widely studied in recent years to meet the urgent need of industry for alternative dielectrics with a subnanometer equivalent oxide thickness (EOT) (Refs. 1–3) for silicon metal-oxide-semiconductor (MOS) devices. Unfortunately, all the promising candidate materials studied have their own merits and problems. Up to now, no material is found to meet all requirements imposed: the chemical/structural stability in contact with Si at high temperature, the large bandgap and conduction/valence band offsets to Si, high *k*-value and preservation of the amorphous morphology at the CMOS processing thermal budget. HfO_2, the most widely studied material, for instance, has a *k* value around 20, a band gap around 5.6 eV, and conductive/valence band offsets to Si 2.0 eV/2.5 eV.[4–8] However, the thermal stability of amorphous HfO_2, grown using different deposition techniques, is poor. Polycrystalline layers are formed at temperatures much lower (500–550 °C) than the thermal budget of the currently used CMOS processing ($T > 900$ °C).[9,10] Another drawback is related to the fact that HfO_2 is a poor oxygen diffusion barrier, so SiO_2 interfacial layer always forms during annealing in oxygen-containing ambient, which sets a limit of scalability of the EOT.

Recently, ternary rare-earth metal oxides such as $GdScO_3$, $DyScO_3$, and $LaScO_3$ are emerging as high-*k* candidates. A *k*-value of about 20 has been demonstrated with $GdScO_3$, $DyScO_3$, and $LaScO_3$ epitaxial layers deposited on a buffer layer on Si.[11] An optical study on single crystalline $GdScO_3$ and $SmScO_3$ (Ref. 12) demonstrated large band gaps. The authors[13] reported also internal photoemission (IPE) and photoconductivity (PC) measurements of $GdScO_3$, $DyScO_3$, and $LaScO_3$, showing a large band gap around 5.6–5.8 eV and large conduction and valence band offsets to Si. Good oxygen diffusion barrier properties are also expected based on the similarity of their properties to Al_2O_3. Phase diagrams of the Sc-containing ternary systems show relatively low melting temperatures,[14] suggesting high crystallization onset temperatures. This is an obstacle for growth of the epitaxial layer,[11] but good news for those who are looking for amorphous high-*k* layers. In this letter, we present a systematic study on amorphous $GdScO_3$, $DyScO_3$, and $LaScO_3$ layers, deposited using off-axial pulsed laser deposition (PLD).

Blanket layers of $GdScO_3$, $DyScO_3$, and $LaScO_3$ with different nominal thicknesses were deposited directly with PLD (Ref. 11) on 2-in. (100) Si substrates for physical characterizations. Ceramics with stoichiometric compositions were used as deposition targets. The deposition was conducted in a N_2 ambient under a pressure of 5×10^{-4} mbar with a substrate temperature between 550 and 570 °C. SE was used for the measurement of thickness and refractive index, TEM for thickness and morphology, and RBS for atomic coverage per unit area. High-temperature grazing incidence XRD was conducted to study the thermal stability of the amorphous phase. Similar layers were grown, under the same conditions, on 2-in. substrates cut out of 8-in. *p*-type Si (100) wafers with a lateral SiO_2 isolation structure for capacitor formation with wet-etched electrodes, enabling $I-V$ and $C-V$ characterization. In both cases, the layers were grown after a wet IMEC clean, resulting in a chemical oxide of around 0.8-nm thickness. Layers about 80 nm were deposited as calibration samples to be measured by RBS to control the composition of the layers and to determine the deposition rate. It is found that the thick layers have compositions close to stoichiometric, $MScO_{3+x}$, where M stands for the rare-earth metals, and x is about 0.5. The layers with nominal thickness of 5, 10, and 20 nm were deposited using the measured deposition rate. RBS shows the same atomic ratio of M and Sc for the thin layers to the thick ones. The thicknesses of the thin layers are too small to give reliable oxygen content.

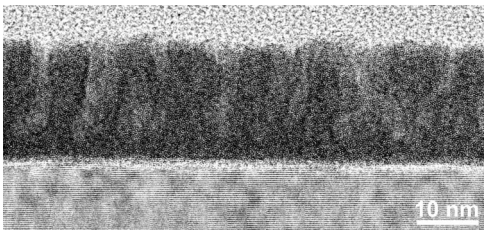

FIG. 1. Cross-sectional TEM image of a $DyScO_3$ layer deposited using PLD onto ~0.8 nm chemical oxide on Si.

To check the lateral uniformity of the layers, RBS and SE measurements have been done on 5 selected spots along the diameter of the 2-in. wafers. TEM observation confirmed the SE thickness, with a marginal difference (<10%). Figure 1 presents a cross-sectional TEM image of the $DyScO_3$ layer with nominal thickness of 10 nm, showing an amorphous layer of about 18 nm in thickness with a rough top surface and ~1-nm thick interfacial SiO_2 layer. SE measurements found a gradient in thickness, symmetric along the wafer radius, and atomic coverage data from RBS show similar profiles. The maximum difference in thickness, from the center to the edge, is about 20%. The densities were calculated from the SE and RBS data. Compared to the bulk crystal densities of the 3 scandates, the measured relative densities are about 70%. This low relative density measured may partly be attributed to the density difference between amorphous and crystalline phases. Also, an overestimation in thickness measurement might have caused an underestimation of the density. In fact, the top surface of the layer is so rough, as revealed by TEM, that both SE and TEM overestimate the thickness by measuring the maximum instead of the average. In addition to these, the low density might indicate also the presence of pores in the layers. The TEM picture in Fig. 1 reveals that the high-*k* layer is composed of two sublayers, a dense one on bottom and a porous one on top. The pores, with contrast different from the bottom sublayer, are relative to the surface roughness, and seem to form open wells in the layer. The depths of the wells are different, and the deepest wells reach the bottom of the top sublayer.

In order to study the morphology of the as-deposited layers and its thermal stability during annealing, high-temperature XRD measurements were conducted as described elsewhere.[15] XRD spectra of $DyScO_3$ measured at different temperatures (not shown) indicate that the layer remains amorphous after annealing at 1000 °C for 30 min, but crystallizes at 1100 °C into hexagonal Dy_2O_3. $GdScO_3$ exhibits almost the same crystallization behavior as $DyScO_3$, while $LaScO_3$ crystallizes at 800 °C into tetragonal $LaScO_3$. The above observation of high crystallization onset temperature suggests $DyScO_3$ and $GdScO_3$ to be highly promising for application as high-*k* gate dielectrics, for which an amorphous structure is preferred. It must be indicated that the onset temperature has been obtained in porous layers, in which the porosity might also influence the results. Further works need to be done on dense layers.

Figure 2 plots the capacitance versus voltage ($C-V$) curves measured on the MOS capacitors using 50 nm sputtered TiN as gate electrode, $DyScO_3$ layers as dielectrics, and *p*-type Si wafers treated by IMEC clean as substrates. The $C-V$ curves measured under forward and reverse voltage sweep direction overlap each other, as shown in Fig. 2(a),

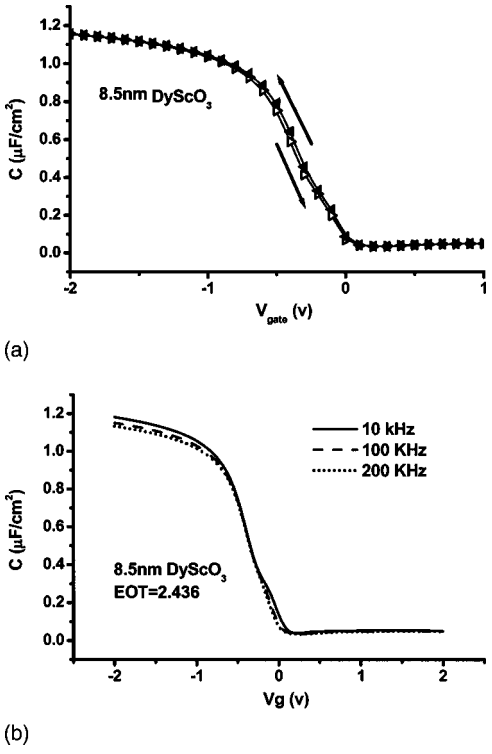

FIG. 2. $C-V$ curves of the *p*-$Si/DyScO_3/TiN$ capacitors measured at 100 kHz using both voltage sweep directions (a) and at different frequencies with voltage swept from accumulation to inversion (b).

indicating a very small hysteresis (<30 mV). The curves also exhibit small humps, implying the presence of slow traps in the scandate layers. $C-V$ curves measured at different frequencies are compared in Fig. 2(b) and show a small dispersion, mainly related to the hump part in the curves. The lower the frequency is, the larger is the hump. This confirms that the hump is due to the presence of slow states, which the contribution to the total MOS capacitance is determined by response time and, therefore, is frequency dependent. The accumulation capacitance is also slightly frequency dependent, which might be due to the effect of series resistance.[16]

To extract the *k*-value of the studied insulators, $C-V$ curves of the capacitors at the center of the wafers with different scandate thickness were analyzed by using Hauser fitting.[16] The EOT, the flat band voltage, and the fixed charge density were obtained from this fitting. Figure 3 depicts the obtained EOT vs physical thickness curves. The experimental data points distribute along a straight line with small dispersion, suggesting the three scandates to have close *k*-values. From the slope of the line, the *k* value can be ex-

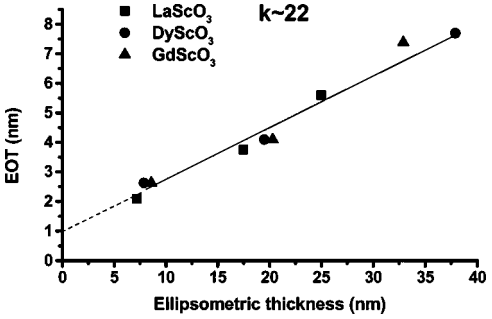

FIG. 3. EOT versus thickness as measured by spectroscopic ellipsometry. The slope of the line gives a *k* value around 22.

tracted as 22 ± 3. Extrapolation of the line to zero SE thickness gives out the thickness of the interfacial layer of about 1 nm, consistent with the results of TEM observations and the nominal thickness of chemical oxide grown during IMEC wet clean using ozonated water.

The leakage currents and breakdown voltage determined from $I-V$ measurements change with the position along the wafer radius due to the thickness gradient. The thicker the layer is, the lower is the leakage current, and the higher is the breakdown voltage. Figure 4 compares the gate leakage current of the scandates measured under the bias of 1 V below the flat band voltage to those of HfO_2 layers in the same MOS structure. The leakage current reduction of the scandate insulators is comparable to HfO_2 insulators in the same MOS structures. This is an encouraging result. In the previous work,[13] the authors studied the energy band alignment of the scandate layers systematically, where the IPE and photoconductivity spectral thresholds were used to determine the energy band diagram. It has been found that the bandgaps relative to Gd, Dy, and La are ~5.6 eV, and the offsets of conduction/valence bands to Si are 2.0/2.5 eV, i.e., close to those in HfO_2. The low leakage current obtained from the capacitor measurements is consistent with the results of energy band alignment determination.

Another feature of the data shown in Fig. 4 is the large deviation in the leakage reduction. Such large deviation should be derived from the poor control of the layer quality in the PLD, which is still an experimental deposition technique. As shown in Fig. 1, the as-deposited layer has a porous top sublayer. It might be the random presence of the pores that results in the data deviation. Figure 4 reveals that the leakage reduction of the scandate layers degrades with the increase of the EOT. This degradation might be also relative to the porosity observed in the top sublayers. From the TEM picture, one can see that the bottom sublayer is about 8 nm. This thickness corresponds to an EOT around 1.5 for materials with a k-value about 20. In the layers thicker than 8 nm, the thickness added to this 8 nm sublayer induces porosity. Its contribution to the leakage reduction is much less than a dense layer. The porosity in the top sublayer is a confusing phenomenon and need further experimental studies.

To conclude, we have demonstrated that the structural and electrical properties of ternary oxides ($LaScO_3$, $GdScO_3$, and $DyScO_3$) are promising for application as high-k dielectrics. These properties include k-value and energy band alignment close to those of HfO_2, good $C-V$ behavior, low leakage levels comparable to HfO_2, and a much higher crystallization onset temperature than HfO_2. For $GdScO_3$ and $DyScO_3$ layers, the dominant phase after annealing at 1000 °C for 30 min is amorphous. Such annealing conditions are harsher than the thermal budget of current CMOS processing. Thus, an amorphous layer with good high-k properties can be expected to preserve its properties through the whole MOS process. In the present work, the layers were deposited on a 1 nm chemical SiO_2, which set a limit of EOT reduction: The lowest EOT achieved here is about 1.7 nm, corresponding to a leakage current around 5×10^{-7} A/cm^2. The work on the capacitors with scandate layers deposited on the hydrogen passivated Si surface is in progress aiming at evaluation of the thermal stability of the interface between the high k layer and Si substrate, which is critical to further scalability of the gate stack.

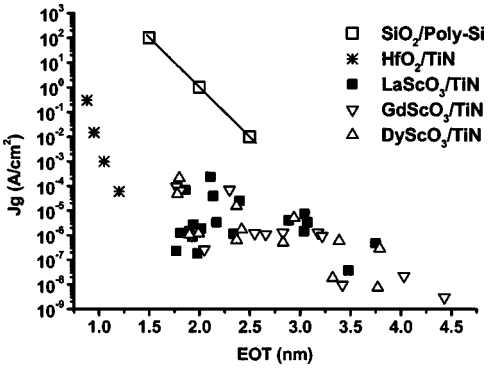

FIG. 4. Gate leakage current measured under a bias of 1 V below the flat band voltage value. All the data were obtained from the capacitors using a TiN electrode except those for SiO_2, which are reference data from the capacitors using a polycrystalline silicon electrode.

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