

Integration of ferroelectric lead titanate nanoislands for direct hysteresis measurements

S. Clemens,^{a)} T. Schneller, and R. Waser^{b)}

Institut für Werkstoffe der Elektrotechnik (IWE2), RWTH Aachen, D-52074 Aachen, Germany

A. Rüdiger, F. Peter, and S. Kronholz

Institut für Festkörperforschung (IFF) and cni—Center of Nanoelectronic Systems for Information Technology, Forschungszentrum Jülich, D-52425 Jülich, Germany

T. Schmitz and S. Tiedke

aixACCT Systems GmbH, D-52068 Aachen, Germany

(Received 24 May 2005; accepted 13 August 2005; published online 29 September 2005)

We report on the integration of fully functional ferroelectric PbTiO_3 nanostructures of typically less than 100 nm lateral extension into a low- k dielectric hydrogen silsesquioxane film. Chemical mechanical polishing of the dielectric layer down to an overall thickness below the nanoparticles height exposes the structures. After confirmation of the piezoelectricity of individual embedded grains, gold electrode pads are deposited to characterize several of these grains in parallel. Evidence of ferroelectric switching is observed and discussed within an equivalent circuit model. This paves the way to a better integration and statistical analysis of ferroelectric nanostructures. © 2005 American Institute of Physics. [DOI: 10.1063/1.2084322]

Nanoscale ferroelectric materials are candidates for high-density, nonvolatile storage media devices like ferroelectric random access memory cells¹ or scanning probe based ferroelectric mass storage media.² In addition to technological challenges that come along with the progressive lateral miniaturization, the characterization of the nanostructures becomes increasingly important. Deviations from bulk behavior are expected with shrinking structure size, nevertheless the scaling of ferroelectric properties is not well understood to date.³ Electrical characterization techniques like direct hysteresis measurements that are carried out on microscopic ferroelectric capacitors routinely today are not yet accomplished on the nanoscale, where the smallest capacitor size is limited to $200 \times 200 \text{ nm}^2$ so far.^{4,5} Recently our group reported on the registered deposition of nanoscale ferroelectric grains on a TiO_2 nucleation matrix,⁶ enabling well-ordered ferroelectric structures with lateral dimensions down to 50 nm. We now present a new technique to embed ferroelectric nanosized grains in a flowable inorganic low- k dielectric layer and to contact them with collective top electrodes. In contrast to prior measurements of ferroelectric structures in parallel,⁷ this technique allows the direct electrical characterization of ferroelectric nanograins with, e.g., variable top electrodes.

Self-assembled ferroelectric PbTiO_3 (PTO) nanoislands are deposited on 1-cm-square platinized silicon substrates by a modified 2-butoxyethanol based chemical solution deposition technique as described elsewhere.^{8,9} The amount of precursor dilution is adjusted to obtain a maximum grain height of 50 nm (Fig. 1).

After this deposition a 60 nm layer of hydrogen silsesquioxane (HSQ)¹⁰ is spin coated onto the samples, filling the

space between the PTO grains and serving as an insulating layer. HSQ is a flowable inorganic polymer of silicon oxide and is widely used as interlayer dielectric due to its high planarization and low dielectric constant ($\epsilon_r=3$ @ 1 MHz). The samples are then heated on a hot plate for 2 min at 150 and 220 °C each to remove the solvent content and to enable a flow of the deposited HSQ film, resulting in a smooth surface with completely embedded PTO structures. The films are cured at 450 °C for 1 h in a rapid thermal processing tool with a nitrogen flow of 200 sccm.

In order to electrically contact the PTO grains, the thin HSQ layer on top of the grains is removed by a chemical mechanical polishing step carried out on a commercial PM4 tabletop polisher.¹¹ A very soft polishing pad (NapTEC) and a slightly harder but therefore chemical resistant OP-Chem pad are used in combination with commercially available Syton SF-1 polishing slurry. This results in a very uniform material removal across the wafer surface. Figure 2 shows embedded PTO grains before and after a polishing step.

The samples are polished down to the pinnacles of the PTO grains with a constant material removal rate of about 7–10 nm/min. A minimum surface roughness of 0.4 nm rms is achieved. Further polishing leads to PTO grains that slightly stick out of the HSQ layer, implying that the removal of PTO goes on slower than the HSQ removal. After the polishing process, the samples are cleaned in acetone under ultrasonic agitation to remove any abrasive particles. To en-

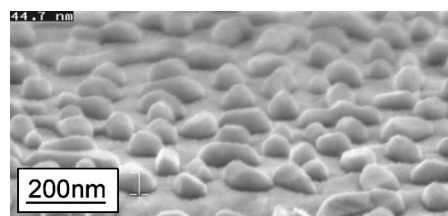


FIG. 1. Scanning electron image of PTO grains on a platinum substrate derived from a 1:5 diluted precursor solution.

^{a)} Author to whom correspondence should be addressed; electronic mail: clemens@iwe.rwth-aachen.de

^{b)} Also at: Institut für Festkörperforschung (IFF) and cni—Center of Nanoelectronic Systems for Information Technology, Forschungszentrum Jülich, 52425 Jülich, Germany.

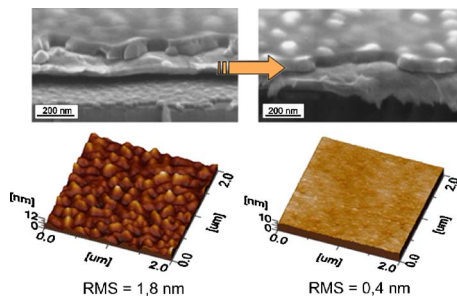


FIG. 2. (Color online) As-embedded PTO grains (left) and PTO grains in HSQ after a 1:30 min polishing time (right). The atomic force images (bottom) show the decrease of surface roughness as a result of the polishing step.

sure that the highest PTO grain tops are indeed electrically accessible, piezoresponse force microscopy (PFM) is carried out. Figure 3 shows the results on a nonpolished and two polished samples of different exposed grain areas. The depicted results show the increase in piezoelectric activity depending on the polishing time compared to a sample with an embedding HSQ layer on top of the PTO grains. The piezoelectric signal indicates the electrical contact between the probe tip and the grains in the case of the polished samples.

Collective gold top electrodes are thermally evaporated using a simple shadow-mask technique. The gold electrodes have a minimum diameter of $75\ \mu\text{m}$.

Direct electrical characterization measurements are carried out on an aixACCT TFAalyzer 2000 ferroelectric test system with FE module. Additional compensation for leakage and dielectric capacitance contributions is applied in some measurements to depict the ferroelectric behavior more clearly.⁴

Even after compensation of large parts of the leakage current, the hysteresis still shows a widening by parasitic currents. However, the results indicate a pronounced switching current peak in the current versus voltage (I - V) graphs. Figure 4(a) shows the uncompensated current response of embedded PTO grains contacted by a $75\ \mu\text{m}$ gold top electrode after a triangular excitation of 10 V at 500 Hz. Note the current peak appearing on the positive voltage loop, indicating a ferroelectric switching of the PTO structures, whereas pure HSQ layers of equivalent thickness (about

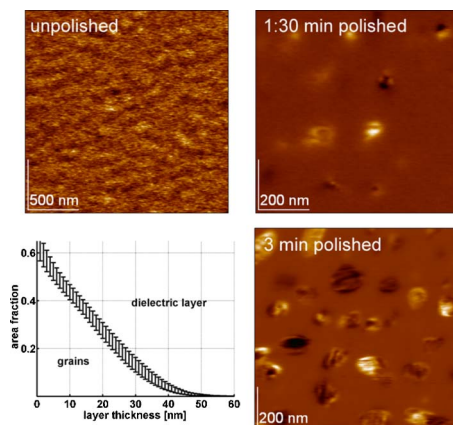


FIG. 3. (Color online) PFM images demonstrating the gain of piezoelectric activity with increasing polishing time. The graph inset (bottom left) displays the expected surface fraction of polished PTO grains against the total layer thickness of HSQ, derived from statistical topographic information of the PTO islands.

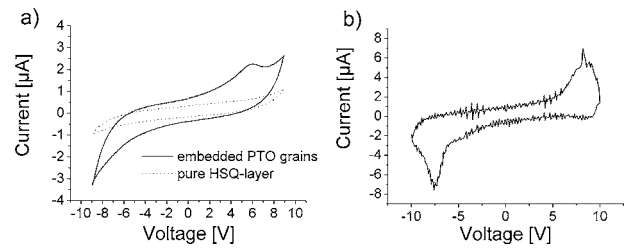


FIG. 4. (a) Current vs voltage (I - V) plot of embedded PTO grains (solid) and of a pure HSQ layer of the same thickness (dashed); (b) I - V curve of embedded PTO grains after compensation of leakage and dielectric capacitance contributions.

50 nm) only show a dielectric current response.

On the negative voltage loop the switching current should appear as well, but is smeared out. This asymmetric switching is attributed to the different bottom and top electrode materials. The main reason for the blurred switching peaks becomes apparent when regarding the equivalent circuit model (Fig. 5). Besides the parasitic capacitance C_{ILD} of the dielectric HSQ layer in connection with a leakage current through R_{ILD} , every single grain is exposed to a distinct capacitance C_i in parallel to a resistance R_i due to a residual HSQ layer on top of the grain or a defective boundary layer that is generated by the polishing step.

The measured current response displays a collective switching signal of several grains at once. Those that are not directly contacted but separated by only a marginal HSQ layer also contribute. Therefore, the switching peak broadens up over a large voltage range. Such an additional in series RC element also accounts for the relatively high coercive fields we observe. The coercive field E_C rises to at least 1.5 MV/cm for the 50-nm-thick PTO grains, if we ignore the voltage drop over the in series elements. An elimination of the residual HSQ layer between top electrode and nanograins can be achieved in two ways that are currently on the way: Chemical mechanical polishing of the grains to the minimum grain height or experiments with grains of a narrow height distribution.⁶ In order to improve the signal quality in the present setup, the current flow through the parasitic capacitance C_{ILD} and resistance R_{ILD} of the dielectric layer is compensated in the measurement shown in Fig. 4(b) at an excitation voltage of 10 V at 1 kHz.

Different pulse patterns are applied to distinguish between ferroelectric switching and relaxation in the material. The sample is prepolarized prior to the different pulse sequences we apply. The delay time between the prepolarizing pulse and the subsequent pulses is varied between 0.1 and 30 s. Whereas for pure dielectric HSQ layers no switching charge is left after holding times that exceed a second, a

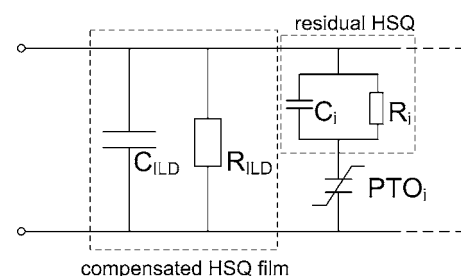


FIG. 5. Equivalent circuit model for embedded grains of different heights in a dielectric layer.

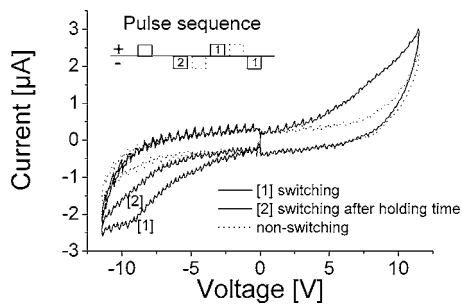


FIG. 6. Current response of embedded PTO grains on switching and non-switching pulses. The pulse cycle applied is shown in the top left of the image.

remaining switching charge is detected for the PTO embedded samples. The current response of embedded PTO grains generated by a pulse sequence of 12 V at 2.5 kHz is shown in Fig. 6. Here the prepolarizing pulse is set to 10 V, the delay time to 3 s and switching and nonswitching pulses are alternating. Although the switching peaks are smeared because of aforementioned reasons, the first pulse after prepolarization switches more charge than the nonswitching pulses. This polarization is remanent.

In conclusion, we have performed direct electrical hysteresis measurements on nanoscale ferroelectric PTO islands

typically smaller than 100 nm and integrated into a low- k dielectric HSQ layer. This parallel measurement paves the way for a direct electrical characterization of ever shrinking ferroelectric nanostructures including their switching properties.

¹O. Auciello, J. F. Scott, and R. Ramesh, *Phys. Today* **51**, 22 (1998).

²T. Tybell, P. Paruch, T. Giamarchi, and J.-M. Triscone, *Phys. Rev. Lett.* **89**, 097601 (2002).

³A. Rüdiger, T. Schneller, A. Roelofs, S. Tiedke, T. Schmitz, and R. Waser, *Appl. Phys. A: Mater. Sci. Process.* **80**, 1247 (2005).

⁴T. Schmitz, K. Prume, B. Reichenberg, A. Roelofs, R. Waser, and S. Tiedke, *J. Eur. Ceram. Soc.* **24**, 1145 (2004).

⁵S. Tiedke, T. Schmitz, K. Prume, A. Roelofs, T. Schneller, U. Kall, R. Waser, C. S. Ganpule, V. Nagarajan, A. Stanishevsky, and R. Ramesh, *Appl. Phys. Lett.* **79**, 3678 (2001).

⁶S. Clemens, T. Schneller, A. v. d. Hart, F. Peter, and R. Waser, *Adv. Mater. (Weinheim, Ger.)* **17**, 1357 (2005).

⁷D. J. Jung, M. Dawber, A. Ruediger, J. F. Scott, H. H. Kim, and K. Kim, *Appl. Phys. Lett.* **81**, 2436 (2002).

⁸R. Waser, T. Schneller, S. Hoffmann-Eifert, and P. Ehrhart, *Integr. Ferroelectr.* **36**, 3 (2001).

⁹R. W. Schwartz, T. Schneller, and R. Waser, *C. R. Chimie* **7**, 433 (2004).

¹⁰Supplied as FOx-12 (flowable oxide), Dow Corning Inc.

¹¹PM4 precision lapping and polishing machine, Logitech Ltd. (Glasgow, UK).