# Dysprosium scandate thin films as an alternate amorphous gate oxide prepared by metal-organic chemical vapor deposition

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Dysprosium scandate ($DyScO_3$) thin films were deposited on Si substrates using metal-organic chemical vapor deposition. Individual source precursors of Dy and Sc were used and deposition temperatures ranged from 480 to 700 °C. Films were amorphous with low root mean square roughness ($\leqslant 2$ Å) and were stable up to 1050 °C annealing. Electrical characterization yielded *C-V* curves with negligible hysteresis ($<10$ mV), high dielectric constant ($\sim 22$), and low leakage currents. The electrical properties of the $DyScO_3/SiO_x/Si$ stacks were stable up to 800 °C for films on native oxide; however, this limit increased to 900 °C for films on special chemically grown oxide, suggesting further improvement with proper diffusion barrier. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2402121]

Dielectric materials with sufficiently high dielectric constant (high $k$) are needed as early as 2007 (Ref. 1) to replace $SiO_2/SiON$ in the future complementary metal oxide semiconductor (CMOS) technology with a subnanometer equivalent oxide thickness. Structural invariance of the thin gate oxide layer within CMOS process thermal budget is preserved with $SiO_2$ ($\varepsilon=3.9$) and now with SiON ($\varepsilon=7.0$). If one considers this as a major criteria the presently favored group IVB oxides, $HfO_2$ and $ZrO_2$, have to be alloyed with high concentrations of Si or Al in order to stabilize the amorphous structure; however, this alloying reduces the dielectric constant ($k$) to the values of $\varepsilon_r \sim 10-12$ (Ref. 2) for the silicates of Hf and Zr. Hence, this silicate with medium $k$ may facilitate a smooth transition from conventional gate dielectrics to high-$k$ dielectrics ($k>20$). In order to reach this target another class of dielectrics with even higher dielectric constants and lower leakage currents is needed. Rare-earth based multicomponent oxides in the amorphous state are being considered as the next generation dielectrics after the silicates.[3] Reported work on these types of materials mainly concentrated on the pulsed laser deposition/molecular-beam or electron beam deposition and these reports suggest a very high potential for these materials in the semiconductor industry.[4–7] An approach by atomic layer deposition of $YScO_3$ and metal-organic chemical vapor deposition (MOCVD) of $DyScO_3$ films were reported recently.[8,9] Our present effort was to realize films of the rare-earth scandate, $DyScO_3$, using advanced precursors in an industry friendly high throughput MOCVD process.

In this work, $DyScO_3$ film depositions were carried out in a liquid injection MOCVD reactor (Aixtron 2600G3 which can handle five 6 in. wafers simultaneously equipped with a liquid delivery Trijet vaporizer).[10] $Dy(EDMDD)_3$ and $Sc(EDMDD)_3$ precursors (EDMDD =6-ethyl-2,2-dimethyl-3,5-decane dionato) were supplied by Asahi Denka, Japan, and were dissolved in octane with 0.05*M* concentration. This precursor solution was injected by a TRIJET system with a flow rate in the micro-liter regime. Film depositions were carried out in the temperature range of 480–700 °C and the reactor pressure was between 2 and 8 mbars. Oxygen and argon were used as an oxidizer and carrier, respectively.

Si (100) substrates with their native oxide were generally used for the deposition and some wafers with a chemically grown $SiO_2$ (IMEC cleaned[11]) were also used for comparison. The composition and areal mass density of the films were routinely determined by x-ray fluorescence (XRF) and checked with Rutherford backscattering spectrometry (RBS). X-ray reflectance and ellipsometry measurements were additionally done to obtain the physical thickness and the density of the layers. Surface morphology and microstructure were investigated with atomic force microscopy (AFM), x-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). Electrical tests of the metal insulator semiconductor (MIS) capacitors were performed with sputter deposited Pt top electrodes, which had undergone a post-deposition forming gas anneal at 450 °C for 20 min.

Stoichiometric films, $Dy/Sc \sim 1$, could be deposited within the temperature range from 480 to 700 °C. AFM investigations showed a smooth surface morphology of the films, with a rms roughness of $\leqslant 0.2$ nm, which was achieved independent of the film thickness (2–15 nm). Figure 1 shows a cross sectional HRTEM of a 560 °C deposited, ~4 nm thick $DyScO_3$ on $SiO_x/Si$ which had undergone an annealing in nitrogen at 900 and 1000 °C, depicting the amorphous nature of the $DyScO_3$ film upon high temperature annealing. An interlayer (IL) of $\sim 2 \pm 0.3$ nm thickness was present between the as-deposited amorphous film and Si (100) substrate (TEM not shown), and IL thickness increased

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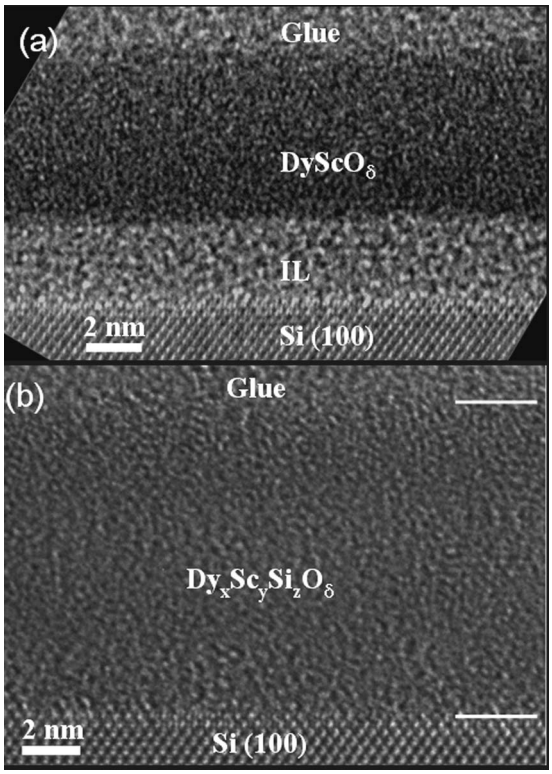


FIG. 1. HRTEM micrograph of a 560 °C deposited, 4 nm thick $DySO_3$ film on $SiO_x$/Si annealed at 900 and 1000 °C; the amorphous structure and interlayer are verified.

to ~2.6±0.3 nm upon annealing at 900 °C [Fig. 1(a)]. It is clear from Fig. 1(b) that interdiffusion and stability of this interlayer ($SiO_x$) are a concern at high temperature, e.g., 1000 °C. Detailed TEM analysis over different regions revealed the disappearance of $SiO_x$ interlayer in most of the regions, but at some regions the interlayer was visible for this 1000 °C annealed sample. This behavior is suggestive of the quality of the native oxide over the wafer surface: region with dense $SiO_2$ can suppress this diffusion but the region with less dense $SiO_x$ accelerates this interdiffusion. This was verified with the *C-V* characteristics of films deposited on specially treated Si surfaces (IMEC cleaned[9,11]), where the reduction in capacitance was not observed after 900 °C annealing (not shown).

XRD established an amorphous structure of the films, Fig. 2. Nevertheless, we observe a broad peak around 30°, which indicates some short range order. Under annealing in purified nitrogen the amorphous structure and the short range order peak are stable up to 1000 °C. At higher temperatures there is indication for phase segregation to binary oxides, especially Dy oxides as reported earlier.[4] Remarkably, in contrast to $N_2$ annealing, $O_2$ annealing at 1050 °C results in the nearly complete disappearance of the broad peak around 30°, which indicates a change of the short range order structure. RBS indicates strong interdiffusion from Si into the $DyScO_3$ layer and vice versa as well as indiffusion of additional oxygen at a temperature around 1050 °C. This interdiffusion is supported by the observed density changes, which are summarized in the inset (Fig. 2). Up to annealing temperatures of 800 °C we observe no changes in the density, but for $T \sim 950$ °C there is, for both atmospheres, a small decrease in density and a corresponding increase in thickness. Consistent with the XRD larger differences are

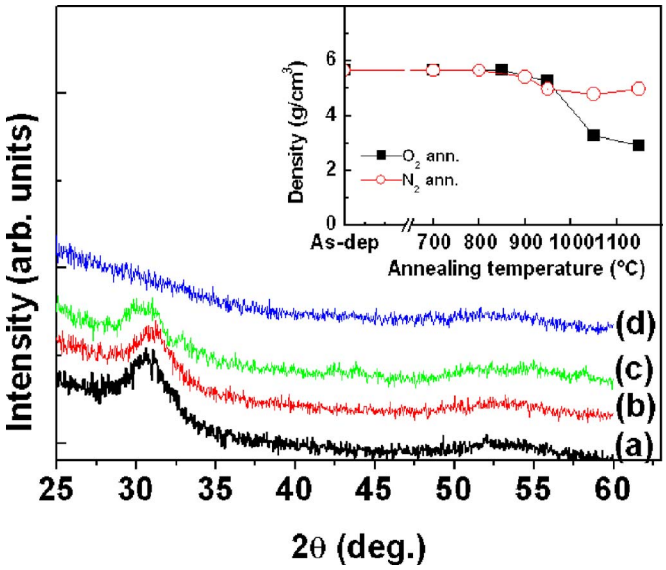


FIG. 2. (Color online) XRD pattern of $DyScO_3$ films deposited on $SiO_x$/Si substrates and annealed at various temperatures in nitrogen atmosphere: (a) 800 °C, (b) 900 °C, (c) 1050 °C and oxygen atmosphere, and (d) 1050 °C. The inset shows variation of density as a function of annealing temperature, which is suggestive of strong interdiffusion under $O_2$ and less significant interdiffusion under $N_2$ for $DyScO_3$ films on Si with native oxide.

observed at 1050 °C with much smaller changes under nitrogen atmosphere. In short, stability of the as-deposited film's amorphous structure at a temperature as high as 1050 °C is verified and there is no increase of the surface roughness of the films along with these annealing treatments but interdiffusion is a concern above 800 °C for $DyScO_3$ films on Si with native oxide.

Electrical properties of MIS capacitors with various thicknesses of $DyScO_3$ were studied by *C-V* and *I-V* characteristics. After an additional postdeposition annealing at 700 °C in $N_2$ there was no difference for films deposited at different temperatures. *C-V* curves showed very low hysteresis (<10 mV) for these films, Fig. 3. Flatband voltage ($V_{fb}$) was not significantly dependent on the film thickness or equivalent oxide thickness (EOT), and the extracted fixed charge density from the EOT versus $V_{fb}$ plot (inset of Fig. 3)

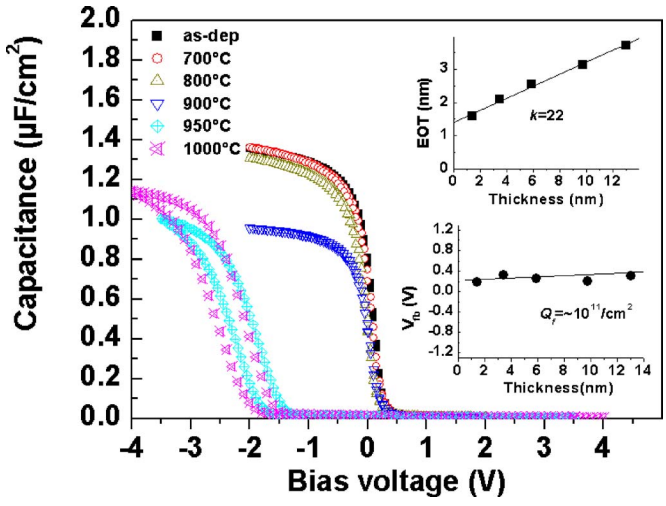


FIG. 3. (Color online) Capacitance-voltage characteristics of the films annealed in $N_2$ at various temperatures for 20 s. Inset shows EOT and $V_{fb}$ as a function of film thickness; the slope of the EOT fit gives a *k* value of ≈22 and the slope of the $V_{fb}$ fit yields fixed oxide charge density of ~$10^{11}$/cm².

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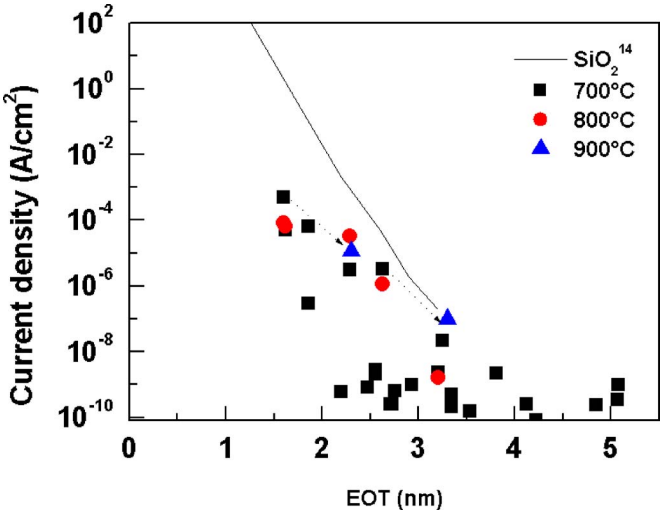


FIG. 4. (Color online) EOT vs current density (at −1 V) for the 700 °C annealed films; annealing at 800 °C shows similar EOT-*J* values for the same samples, but annealing at 900 °C reduced the leakage current at the cost of EOT.

was $\sim 10^{11}/\mathrm{cm}^2$. From the slope of the linear fit of EOT versus thickness (inset, Fig. 3) a $k$ value of $\approx 22$ is derived which is comparable to the best values reported for $HfO_2$.[12,13] The $y$ offset of 1.5 nm corresponds essentially to the nonoptimized interlayer. These promising dielectric data are combined with very low leakage currents ($10^{-3}-10^{-10}$ A/cm$^2$ for film with EOT of 1.5–5.5 nm) compared to $SiO_2$ films, as can be seen from Fig. 4.[14] A direct comparison of leakage current density at $(V_{fb}-1)$ V of this scandate film with the atomic layer deposited $HfO_2$ films (Ref. 13) having same EOT also shows comparable leakage current even without optimizing the interlayer. In the latter, instantaneous formation of a $SiN_x$ interlayer due to the nitrogen containing precursors prevented the Si diffusion and showed lower EOT and leakage current.[13] This type of diffusion barrier effect of the IL might be used for $DyScO_3$ films on Si as well to reduce the leakage current and EOT further.

Annealing studies on the *C-V* characteristics, Fig. 3, show a reduction in $C_{max}$ at temperatures above 800 °C for films deposited on Si with native oxide due to the interlayer growth and/or interdiffusion. A higher temperature annealing resulted in a very drastic shift in the $V_{fb}$ without much additional reduction in capacitance suggestive of the diffusion of Dy and Sc through the interlayer. This shift in the $V_{fb}$ and the reduction in the $C_{max}$ can be reduced with specially treated Si surface. Our experiment on the IMEC cleaned Si [chemically grown $SiO_2$ on Si (Ref. 11)] resulted in the same capacitance till 900 °C annealing and the reduction was observed at 1000 °C without much shift in the $V_{fb}$. This indicates that by optimizing the stability of the interface, interdiffusion can be suppressed and even higher temperatures might be achievable.

To summarize, stoichiometric $DyScO_3$ thin films with very smooth surface morphology could be realized with liquid injection MOCVD. Electrical investigation shows very low leakage current densities and *C-V* curves with negligible hysteresis and low fixed charge density. Dielectric constant was around 22 for this amorphous material and thus it is interesting for scaling down the EOT for ≤45 nm node. Although the amorphous structure is retained up to 1050 °C, interdiffusion, which deteriorates the electrical properties, must be considered at temperatures above 800 °C for films on Si with native oxide. Remarkably, this decrease in the capacitance can be delayed till 900 °C by using specially treated Si surface (IMEC clean[11]). As these reactions depend on the details of the processing, there is much room for optimization, especially considering that the high temperature annealing is performed after electrode deposition, i.e., for a capsulated gate oxide. In addition, these advanced dielectric films will most probably combine with metal gates, which require a different thermal budget. Hence, there is a good chance that the superior properties of this new gate oxide can survive the gate processing.

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