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Meinen Eltern

Abstract

Ion-sensitive field-effect transistors (ISFETs) are employed as bioelectronic sensors for the cell-transistor coupling and for the detection of DNA sequences. For these applications, thermally grown SiO_2 films are used as standard gate dielectric.

In the first part of this dissertation, the suitability of high-k dielectrics was studied to increase the gate capacitance and hence the signal-to-noise ratio of bioelectronic ISFETs: Upon culturing primary rat neurons on the corresponding high-k dielectrics, Al_2O_3, yttria stabilised zirkonia (YSZ), $DyScO_3$, CeO_2, $LaAlO_3$, $GdScO_3$ and $LaScO_3$ proved to be biocompatible substrates. Comprehensive electrical and electrochemical current-voltage measurements and capacitance-voltage measurements were performed for the determination of the dielectric properties of the high-k dielectrics. High dielectric constants of the produced Al_2O_3, YSZ und $DyScO_3$ films facilitated the processing of ISFETs with considerably higher input capacitances than the standard SiO_2 ISFETs. The achieved breakdown fields of the Al_2O_3, YSZ und $DyScO_3$ films ensured their reliable employment as ISFET gate dielectric. Good stability against electrostatic charging and small interface state densities were concluded from small hysteresis in the capacitance-voltage measurements.

In the second part of the dissertation, standard SiO_2 ISFETs with lower input capacitance and high-k dielectric Al_2O_3, YSZ und $DyScO_3$ ISFETs were comprehensively characterised and compared with each other regarding their signal-to-noise ratio, their ion sensitivity and their drift behaviour. One of the results was that the transconductance and the signal-to-noise ratio of the high-k ISFETs did not improve according to their higher input capacitance. It is assumed that high source and drain feed line resistances and the invalidity of the long-channel field-effect transistor equation for the employed ISFETs are the underlying reasons. The ion sensitivity measurements showed that the YSZ ISFETs were considerably more sensitive to K^+ and Na^+ ions than the SiO_2, Al_2O_3 und $DyScO_3$ ISFETs. Hence YSZ ISFETs are suited to study the impact of the ion sensitivity of the gate dielectric in the cell-transistor coupling mechanism. In long-term drift measurements, the YSZ ISFETs drifted much longer and further than the other ISFETs. Higher porosity of the YSZ films is assumed as underlying reason.

In the final third part of the dissertation, bioelectronic experiments were performed with the high-k ISFETs. Alternating deposition of oppositely charged polyelectrolyte layers, a model experiment for DNA detection, was successfully carried out with Al_2O_3 and $DyScO_3$ ISFETs. In first DNA detection experiments with Al_2O_3 ISFETs, small hybridisation signals were measured. Coupling between YSZ and $DyScO_3$ ISFETs and the HL-1 heart cell line was performed successfully in proof of principle experiments. The shape of the signals, which were measured from HL-1 cells with YSZ ISFETs, differed

considerably from the corresponding measurements with SiO_2 and $DyScO_3$ ISFETs: After the onset of the K^+ current, the action potentials measured with YSZ ISFETs showed a strong drift in the direction opposite to the K^+ current signal. In the YSZ ion sensitivity measurements, it was shown that this drift is an intrinsic property of YSZ. Therefore, in a general conclusion, it is assumed that the signal shapes measured in cell-transistor coupling experiments are influenced by the chemical properties of the gate oxide surface. First coupling experiments between HEK 293 cells, which were transfected with a K^+ ion channel, and YSZ ISFETs affirmed the assumption from the HL-1 experiments that the characteristic drift behaviour of YSZ ISFETs influences the measured signal shapes.

In summary, especially $DyScO_3$ has proven to constitute an excellent bioelectronic interface for field-effect transistors with high input capacitance: The $DyScO_3$ films exhibited a high dielectric constant and good chemical stability in the ion sensitivity measurements and the long-term drift measurements. Furthermore, the biocompatibility of the $DyScO_3$ films was demonstrated in successful coupling experiments with electrically active cells.

Zusammenfassung

Ionensensitive Feld-Effektransistoren (ISFETs) werden als bioelektronische Sensoren für die Zell-Transistor-Kopplung und für die Detektion von DNA-Sequenzen verwendet. Als Standard-Gatedielektrikum kommen hierbei thermisch gewachsene SiO_2-Schichten zum Einsatz.

In der vorliegenden Dissertation wurde zunächst untersucht, inwiefern high-k Dielektrika geeignet sind, die Gatekapazität und damit das Signal-Rausch-Verhältnis von bioelektronischen ISFETs zu erhöhen: Beim Kultivieren von primären Rattenneuronen auf den entsprechenden high-k Dielektrika erwiesen sich Al_2O_3, yttriumstabilisiertes Zirkonoxid (YSZ), $DyScO_3$, CeO_2, $LaAlO_3$, $GdScO_3$ und $LaScO_3$ als biokompatible Substrate. Zur Bestimmung der dielektrischen Eigenschaften der high-k Dielektrika wurden umfangreiche elektrische und elektrochemische Strom-Spannungs-Messungen und Kapazitäts-Spannungs-Messungen durchgeführt. Hohe Dielektrizitätskonstanten der produzierten Al_2O_3-, YSZ- und $DyScO_3$-Schichten ermöglichten die Herstellung von ISFETs mit deutlich höherer Eingangskapazität als die bisher verwendeten SiO_2-Standard-ISFETs. Die erzielten Durchbruchsfeldstärken der Al_2O_3-, YSZ- und $DyScO_3$- Schichten gewährleisteten ihren zuverlässigen Einsatz als ISFET-Gatedielektrika. Kleine Hysteresen in den Kapazitäts-Spannungs-Messungen ließen auf geringe Oberflächenzustandsdichten und gute Stabilität gegen elektrostatisches Aufladen schließen.

Im zweiten Teil der Dissertation wurden Standard-SiO_2-ISFETs mit geringerer Eingangsgatekapazität und high-k dielektrische Al_2O_3-, YSZ- und $DyScO_3$-ISFETs umfassend in Bezug auf ihr Signal-Rausch-Verhältnis, ihre Ionensensitivität und ihr Driftverhalten charakterisiert und miteinander verglichen. Hierbei zeigte sich, dass sich die Transkonduktanz und das Signal-Rausch-Verhältnis der high-k ISFETs nicht ihrer höheren Eingangskapazität entsprechend verbesserten. Es wird angenommen, dass hohe Source- und Drain-Zuleitungswiderstände und die Ungültigkeit der Langkanal-Feld-Effekt-Transistor-Gleichung für die verwendeten ISFETs die Ursachen hierfür sind. Bei den Ionensensitivitätsmessungen reagierten die YSZ-ISFETs erheblich empfindlicher auf K^+- und Na^+-Ionen als die SiO_2-, Al_2O_3- und $DyScO_3$-ISFETs. Daher sind YSZ-ISFETs geeignet, den Einfluss der Ionensensitivität des Gatedielektrikums im Zell-Transistor-Kopplungsmechanismus zu untersuchen. In Driftlangzeitmessungen drifteten die YSZ-ISFETs sehr viel länger und weiter als die anderen ISFETs. Als Ursache wird eine höhere Porosität der YSZ-Filme angenommen.

Im abschließenden dritten Dissertationsteil wurden mit den high-k ISFETs bioelektronische Experimente durchgeführt. Die abwechselnde Abscheidung entgegengesetzt geladener Polyelektrolytschichten, ein Modellexperiment für die DNA-Detektion, wurde mit Al_2O_3- und $DyScO_3$-ISFETs erfolgreich durchgeführt. Bei ersten

DNA-Experimenten mit Al_2O_3-ISFETs wurden kleine Hybridisierungssignale gemessen. Die Kopplung zwischen YSZ- und $DyScO_3$-ISFETs und der HL-1 Herzzelllinie wurden in proof of principle-Experimenten erfolgreich durchgeführt. Die von HL-1 Zellen mit YSZ-ISFETs gemessenen Signalformen wichen erheblich von den entsprechenden Messungen mit SiO_2- und $DyScO_3$-ISFETs ab: Nach dem Einsetzen des K^+-Stromes zeigten die mit YSZ-ISFETs gemessenen Aktionspotentiale eine starke Drift in die dem K^+-Stromsignal entgegengesetzte Richtung. In den YSZ-Ionensensitivitätsmessungen war gezeigt worden, dass diese Drift eine intrinsische Eigenschaft von YSZ ist. Daher wird in einer allgemeinen Schlussfolgerung angenommen, dass die bei der Zell-Transistor-Kopplung gemessenen Signalformen von den chemischen Eigenschaften der Gateoxidoberfläche beeinflusst werden. Erste Kopplungsexperimente zwischen HEK 293 Zellen, die mit einem K^+-Ionenkanal transfisziert waren, und YSZ-ISFETs bestärkten die Vermutung von den HL-1 Experimenten, dass das charakteristische Driftverhalten der YSZ-ISFETs die gemessenen Signalformen beeinflusst.

Zusammenfassend erwies sich insbesondere $DyScO_3$ als hervorragendes bioelektronisches Interface für Feld-Effekt-Transistoren mit hoher Eingangskapazität: Die $DyScO_3$-Filme hatten eine hohe dielektrische Konstante und bewiesen bei den Ionensensitivitätsmessungen und den Driftlangzeitmessungen gute chemische Stabilität. Darüber hinaus wurde die Biokompatibilität der $DyScO_3$-Filme in erfolgreichen Kopplungsexperimenten mit elektrisch aktiven Zellen demonstriert.

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1 Introduction

1.1 Motivation for cell-transistor coupling with high-k dielectric ISFETs

Stable long-term recording of the electrical activity of cardiomyocytes and neurons with ion-sensitive field-effect transistors (ISFETs) implies many highly promising, partly visionary applications [Offenhäusser and Knoll, 2001; Fromherz, 2003]: (i) Pharmacological as well as toxicological lab on a chip concepts may allow fast, high-throughput screening of potential drugs for their effects. (ii) The high sensitivity and selectivity of biological recognition systems with signal-amplification cascades, which have been optimised by evolution, may be utilised for the development of biosensors with an unprecedented detection threshold. One evident area of application for such biosensors would be the monitoring of environmental factors. (iii) Multi-site interfacing of neuronal networks with ISFET arrays right on the microscopic level of individual nerve cells would facilitate spatiotemporal mapping of brain dynamics. In conjunction with neuron stimulation from capacitive structures, which could be likewise integrated into the ISFET chip, synaptic communication between the neurons of a neuronal network could be evoked and subsequently recorded by the ISFET array. Such bidirectional cell-transistor coupling, which combines stimulation and recording of electrical cell activity, would help to unravel the nature of information processing in the brain including the fascinating properties of learning and creativity. (iv) The ultimate vision of long-term and bidirectional integration of neuronal networks and digital microelectronics on the level of individual neurons and semiconductor devices constitutes the formation of microelectronic neuroprostheses and bioelectronic neurocomputers with associative memory.

Since the patch-clamp technique is highly reliable and has optimum signal-to-noise ratio, it is the standard method for the recording of electrical cell activity [Hamill et al., 1981]. However, patch-clamping cannot be employed for long-term, multi-site recordings: Since it is an invasive method, recorded cells die within tens of minutes. Furthermore, due to the instrumental complexity of the patch-clamp set-up (microscope and micromanipulator), simultaneous recording from more than several few cells is not possible. Another method for the detection of rapid changes in membrane potential is the probing with voltage-sensitive fluorescent dyes. However, most dyes are toxic on illumination, which makes them unsuitable for long-term recording. Moreover, also here, the instrumental complexity of fluorescent microscopes inhibits a high integration of recording sites.

In principle, non-invasive and multi-site recording of electrical cell activity over longer periods can be achieved by two systems: Microelectrode arrays, i.e. metal lines, which are deposited on a planar substrate and subsequently covered by an insulator except for the sensing area at the end of the respective line [Pine, 1980; Gross et al., 1985]; and

arrays of ISFETs, i.e. semiconductor devices, whose operation is based on the field-effect over their insulating gate oxide (sensing area) (for details see chapter 2). Although assembly and working principle of microelectrodes and ISFETs are rather different (i.e. microelectrodes have a low impedance input, while ISFETs have a high impedance input), their signal-to-noise ratios in extracellular recordings are comparable.

However, the ISFET offers two important advantages over the microelectrode: Firstly, the ion sensitivity of the gate oxide gives rise to a signal component, which is not exhibited by inert metal electrodes: K^+ and Na^+ ions, which are the prevailing ion species involved in electrical cell activity, adsorb selectively to the fraction of the gate oxide surface groups, which terminates with negatively charged O^- atoms (for details see chapter 2.2.3). Hence, the ion sensitivity of the ISFET constitutes an additional information source for the elucidation of the electrical processes occurring in the recorded cell. The ion sensitivity of the ISFET has been studied extensively in the work of this thesis and the corresponding results are presented in chapter 4.3.2.

Secondly, the CMOS (complementary metal-oxide-semiconductor) technology, which has been developed and optimised by the semiconductor industry for the production of integrated circuits, can be adapted for ISFET arrays [Yeow et al., 1997]. Two core elements of CMOS allow to overcome the interconnect restrictions, which inhibit high integration and recording at cellular resolution from metal electrode arrays: Multi-level architectures, which consist of several planar device levels built into the semiconductor on top of each other and connected via vertical metal lines; and multiplexed readout techniques, which facilitate to select only the ISFETs covered with electrically active neurons for recording. The CMOS approach has been applied successfully in the development of an ISFET array of 128 x 128 sensor transistors with pitch 7.8 µm [Eversmann, et al., 2003]. For comparison, the current arrays of metal electrodes are limited to pitch sizes of several tens of µm.

The main obstacle, however, for the realisation of the applications described in the first paragraph has always been and still is the rather poor signal-to-noise ratio in the cell-transistor coupling experiments. In order to enhance the coupling of electrical signals into ISFETs, the thickness (capacitance) of their SiO_2 gate oxide has continuously decreased (increased): The first cell-transistor coupling was achieved in 1976, when electrical signals of muscle fibres were recorded by an ISFET with a gate oxide thickness of 50 nm [Bergveld et al., 1976]. The first recording of electrical activity from an individual invertebrate neuron was performed in 1991 with an ISFET, which had a gate oxide thickness of 20 nm [Fromherz et al., 1991]. The first ISFET recordings from vertebrate neurons [Vassanelli and Fromherz, 1998] and cardiomyocyte layers [Sprössler et. al, 1999] were exhibited with 10 to 12 nm thick SiO_2 gates.

This increase in the gate oxide capacitance of the ISFET follows the trend set by the metal-oxide field-effect transistor (MOSFET), the prevailing device in microelectronic circuits: Since the invention of the integrated circuit (IC) and planar technology,

respectively, in the early 1960s, the MOSFET device density on IC chips has up to date doubled approximately every 18 months, which is known as Moore's law [Moore, 1965]. The reason underlying MOSFET downscaling is the demand for lower costs per device and faster ICs due to shorter switching times. According to the design rules of constant-field scaling, which keeps crucial parameters of the downscaled MOSFET such as the transconductance and the power density constant, the gate capacitance must increase with the same factor as the surface dimensions of the MOSFET decrease [Muller and Kamins, 2002]. Hence, during the process of downscaling, the gate capacitance of the MOSFET has increased continuously.

Despite the likewise increase in the gate capacitance, however, the thickness threshold for a reliable SiO_2 gate dielectric, which is suited for long-term usage, is quite different for MOSFETs and ISFETs: While the physical limit in metal – oxide – semiconductor (MOS) structures is given by 1.0 to 1.2 nm SiO_2 (only a few atomic layers!) [Wilk et al., 2001], the limit in electrolyte – oxide – semiconductor (EOS) structures has shown in the experiments of our group to be on the order of 10 nm SiO_2. The mobility of the ions contained in the electrolyte is generally believed to account for the required larger gate dielectric thickness in ISFETs: According to the gate-source voltage applied during operation, ions penetrate the ISFET gate oxide and lead to much faster dielectric breakdown than in MOSFETs.

Since the late 1990s, the MOSFET community has studied intensively the suitability of high-k dielectrics, i.e. oxides with a dielectric constant higher than SiO_2, as replacement for the SiO_2 gate dielectric. The underlying reason was that the gate capacitance required by the MOSFET downscaling approached the physical thickness limit of SiO_2 for being a reliable dielectric. High-k dielectric films exhibit the same capacitance as SiO_2 films at a thickness, which is larger than the corresponding SiO_2 film by the inverse of the ratio between their dielectric constants. Therefore, high-k dielectric films exhibit lower leakage currents and higher stability against dielectric breakdown than the corresponding SiO_2 films of the same capacitance.

In the work presented in this thesis, the suitability of high-k dielectrics as replacement for SiO_2, which is the standard dielectric of ISFETs employed in cell-transistor coupling [Offenhäusser and Knoll, 2001; Fromherz, 2003], was studied comprehensively for two reasons: Firstly, in line with the MOSFET community, it was expected that high-k dielectrics allow to increase the capacitance of the gate oxide beyond the limit set by SiO_2 for reliable ISFET operation. Consequently, signals from electrogenic cells should couple stronger into high-k dielectric ISFETs than into standard SiO_2 ISFETs. Provided that the noise level is kept constant, high-k dielectrics would exhibit larger signal-to-noise ratios.

Secondly, the high-k dielectric films were expected to differ in their surface chemistry, in particular in their ion sensitivity to K^+ and Na^+, from the SiO_2 films. Consequently, cell-transistor coupling to high-k dielectric ISFETs should allow to study

the impact of the ion sensitivity of the respective gate material on the recorded signals, which constitutes a currently debated issue in the literature [Brittinger and Fromherz, 2005; Wrobel et al., 2005].

1.2 Motivation for DNA detection with high-k dielectric ISFETs

In recent years, DNA detection has become a standard technique in biotechnology and medical diagnostics. Most of the employed DNA detection methods take advantage of the highly specific DNA base-pairing (hybridisation) reaction between complementary single-stranded (ss) DNA sequences: After immobilising an micro-array of so-called probe ssDNA sequences onto a surface, the analyte (target) ssDNA binds specifically to its complementary probe DNA (for details see chapter 2.3.1). Subsequently, the location of hybridisation in the array and thus the sequence of the analyte DNA is identified. Most commonly this is achieved by labelling the analyte DNA molecules before the hybridisation reaction with fluorescent markers, which after the hybridisation can be detected by commercially available optical reader systems [Affymetrix]. Alternatively, also radioactive labelling is used.

However, in order to accomplish a fast, inexpensive and miniaturised detection system, which is suited to be operated in a doctor's surgery, the elaborate labelling step has to be avoided. The direct detection of the intrinsic, negative electrical charge of the analyte ssDNA by means of an ISFET constitutes such a label-free method: When the target ssDNA hybridises with the probe ssDNA, which afore had been immobilised onto the gate oxide, its negative charge gives rise to an ISFET signal identifying the analyte DNA (for details see chapter 2.3.1). The usage of ISFET arrays may also allow parallel screening for many DNA sequences at a time as it is performed nowadays by the fluorescent labelling technique.

Due to their higher gate capacitance compared to standard SiO_2 ISFETs, high-k dielectric ISFETs should record larger DNA hybridisation signals and allow to enhance the signal-to-noise ratio. The main contribution, however, which high-k dielectric gate oxides could make to the field of DNA detection with ISFETs, is the elucidation of the detection mechanism: The current debate in the literature discusses, whether the pH sensitivity of the gate oxide is crucial for the amplitude measured in DNA detection experiments [Landheer et al., 2005; Poghossian et al., 2005; Poghossian et al., 2006] (for details see chapter (2.3.1)). Provided the pH sensitivity plays an important role, high-k dielectric ISFETs would record signal amplitudes, which scale with their intrinsic pH sensitivity.

Hence, in the work of this thesis, it was studied, whether the same probe DNA immobilisation protocol, which has been developed for SiO_2 surfaces [Han et al., 2006a], can also be applied to the high-k dielectrics Al_2O_3, YSZ and $DyScO_3$. Furthermore, proof of principle DNA detection experiments have been performed.

1.3 Thesis outline

Chapter 2 describes the general theory of the ISFET and its coupling to bioelectronic signals of electrogenic cells and DNA. Chapter 3 contains the materials and methods section, which motivates the respective experiments and informs in detail about their execution. Chapter 4 presents in systematic order the results obtained in the work of this thesis: Chapter 4.1 contains the ellipsometric, SEM and AFM surface characterisation of the employed high-k dielectrics Al_2O_3, YSZ, $DyScO_3$ and CeO_2. Chapter 4.2 comprises their dielectric properties (breakdown field, capacitance and dielectric constant, oxide charges) determined from electrical and electrochemical I-V and C-V measurements. Chapter 4.3 presents the properties of the fabricated Al_2O_3, YSZ and $DyScO_3$ high-k dielectric ISFETs themselves. And chapter 4.4 shows the results of successful bioelectronic coupling between high-k dielectric ISFETs and electrogenic cells and DNA, respectively. Chapter 5 summarises the conclusions of this thesis and gives an outlook for future bioelectronic coupling to high-k dielectric ISFETs. Finally, the thesis concludes with the list of the used references and abbreviations in the appendices and with the acknowledgements.

2 The ISFET as bioelectronic interface

The ion-sensitive field-effect transistor (ISFET) was invented in 1972 by P. Bergveld [P. Bergveld, 1972]. It is a derivate of the metal-oxide-semiconductor field-effect transistor (MOSFET), the prevailing device in microelectronic circuits. ISFETs and MOSFETs have identical structures except for the gate electrode, which contacts the gate oxide. While the MOSFET possesses a metal or poly-silicon electrode, in the ISFET the gate oxide is contacted via an electrolyte and the corresponding reference electrode (see figure 2.1).

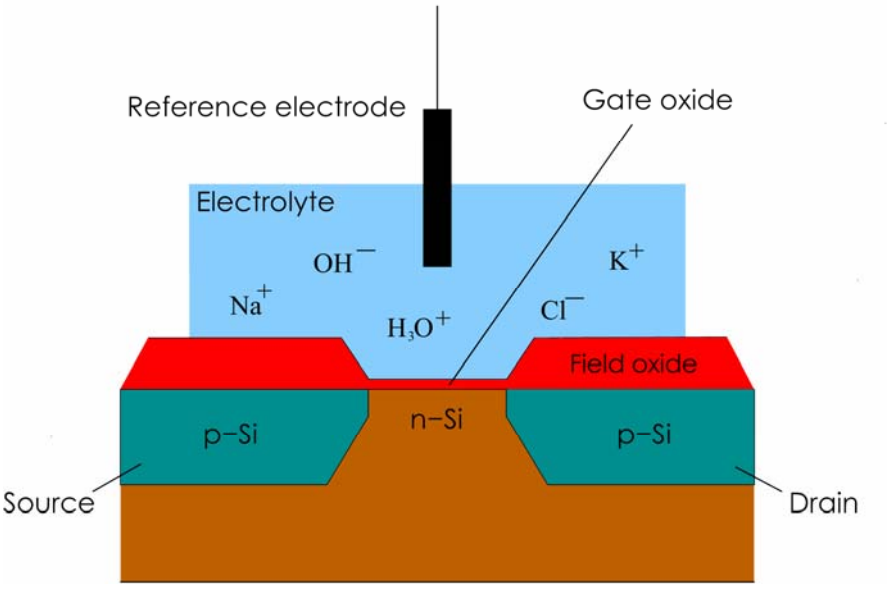


Figure 2.1: Schematic drawing of a p-channel ISFET with its three electrical contacts: The source (p-Si), the drain (p-Si) and the electrolyte with reference electrode. The central vertical structure, which consists of the n-Si region, the thin gate oxide film and the electrolyte, constitutes an EOS diode. Source, drain and feed lines are passivated from the electrolyte by a thick layer of field oxide.

The central vertical structure of an ISFET, which is composed of the electrolyte, the gate oxide and the underlying silicon (see figure 2.1), constitutes a so-called electrolyte – oxide – semiconductor (EOS) diode. Since the properties of this EOS diode determine also most of the properties of the corrresponding ISFET, the EOS diode is the crucial component of an ISFET. In analogous manner, the metal – oxide – semiconductor (MOS) diode determines the properties of an MOSFET.

Due to the prominence of the MOSFET as microelectronic device, the MOS diode has been studied extensively in comparison with the EOS diode and a comprehensive theory of its dielectric properties has been developed [Nicollian and Brews, 1982]. For the theoretical treatment of EOS diodes, the energy-band diagram of the MOS diode has to be adapted to the electrolyte – oxide interface: The energy barrier height is no longer defined by the difference between the metal Fermi level and the oxide conduction band, but the

difference between the valence electron level of the conducting ion species in the electrolyte and the oxide conduction band. This barrier height adaptation is analogue to the case, when the metal of a MOS diode is exchanged for another. In conclusion, the MOS theory can generally be applied to the EOS diode because metal and electrolyte are merely two different electrode types to contact the oxide.

Finally in the comparison between MOS and EOS diode, it should be mentioned that although the energy-band diagrams are equivalent, EOS and MOS diode differ concerning leakage currents and dielectric breakdown in one important point: direct currents (DC) in EOS diodes are always accompanied by electrolysis, normally visualised by gas production at the electrodes, because the electrolyte – oxide interface constitutes an ionic conductor – electronic conductor interface.

As mentioned earlier, the treatment of the MOS diode in the literature is compared with the treatment of the EOS diode considerably more thorough. Hence, the theory of the MOS and not the EOS diode is described in the following chapter. However, all properties account to the EOS diode as well.

2.1 The metal – oxide – semiconductor diode

2.1.1 Tunnelling currents and dielectric breakdown

Current-voltage (I-V) characteristics of MOS diodes show that thin dielectric films are not perfect insulators. At high electric fields (on the order of 10 MV/cm), considerable currents flow over oxide films [Sze, 1981]. Since 10 MV/cm corresponds to 1 V/nm, these field strengths are obtained in thin dielectric films at voltages on the order of only several volts. The underlying process is quantum mechanical tunnelling of electrons through the oxide energy barrier [Autran et al., 2004]. The electron tunnelling mechanisms responsible for leakage currents and dielectric breakdown in oxides are displayed in the energy-band diagrams of figure 2.2.

In general, the probability for a tunnelling process is proportional to $e^{-\Delta E \cdot d}$, where ΔE is the energy barrier height, which is mainly defined by the conduction band offset between oxide and cathode, and d is the tunnelling distance [Bonnell and Huey, 2001]. The barrier height dependence causes the tunnelling probability through a dielectric to vary considerably with the respective material.

During the so-called direct tunnelling process, electrons surmount the energy barrier by tunnelling through the entire dielectric in one step (see figure 2.2). Due to the strong distance dependence for the tunelling probability, only in ultrahin oxide films with thicknesses on the order of 5 nm and below, the direct tunnelling process plays a substantial role [Green et al., 2001].

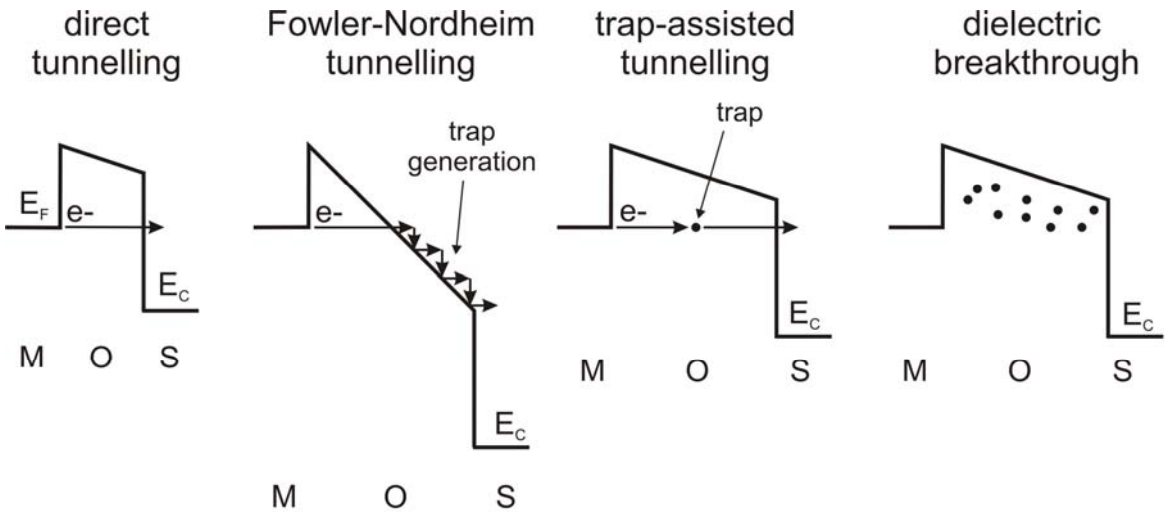


Figure 2.2: Energy-band diagrams of a MOS diode displaying the electron tunnelling mechanisms responsible for leakage currents and dielectric breakdown in oxides: Direct tunnelling through ultrathin dielectrics; Fowler-Nordheim tunnelling at high electric fields generating traps; trap-assisted tunnelling after Fowler-Nordheim stress or in dielectrics with intrinsically high trap densities. The arrows within the oxide indicate the respective tunnelling distances. The small arrows in the Fowler-Nordheim diagram stand for the alternate acceleration and collision of electrons with oxide atoms, whereby traps are generated. Note the required thinner oxide thickness in the direct tunnelling diagram and the required higher electric field in the Fowler-Nordheim diagram. Finally, the graph to the ultimate right depicts the situation after dielectric breakdown: The trap density has risen to a level, where the dielectric material has become conducting along trap paths through the dielectric.
In each diagram, M indicates the metal electrode, O the oxide and S the silicon. E_C stands for the silicon conduction band energy and E_F for the metal Fermi level. Adapted from [Autran et al., 2004] and [Chou et al., 1997].

In thicker oxide films, leakage currents are caused by indirect tunnelling, where the oxide energy barrier is surmounted only in part by one single tunnelling process. Two indirect mechanisms are distinguished (see figure 2.2) [Chou et al., 1997]: During Fowler-Nordheim tunnelling, electrons enter the oxide conduction band after completion of the tunnelling process. The remaining distance is travelled in the conduction band. During trap-assisted tunnelling, electron traps in the band gap serve as intermediate tunnelling sites: Electrons from the cathode tunnel first into a trap and subsequently tunnel out of the trap towards the anode. However, as required by the distance dependence of the tunnelling probability, the maximum distance covered by one single tunnelling process is for indirect tunnelling on the same order of magnitude as for direct tunnelling (~ 5 nm).

The traps involved in trap-assisted tunnelling are composed of structural defects in the dielectric such as atomic vacancies or impurities. Due to the interruption of the structural symmetry, defects have energy levels associated with them, which lie within the band gap of the dielectric [Wagemann, 1992] as shown in figure 2.2. The density of

structural defects and electron traps is an intrinsic property of the respective dielectric film and its fabrication method. Therefore, the extent of trap-assisted tunnelling current can vary considerably with the respective dielectric film.

Furthermore, traps are generated during Fowler-Nordheim tunnelling, when electrons inside the conduction band gain sufficient energy from high electric fields to damage the oxide structure during collisions with oxide atoms (see figure 2.2) [Chou et al., 1997]. Ultimately this trap generation leads to dielectric breakdown, which is a two stage process: During the first stage, the number of charges trapped within the dielectric increases with time forming high electric fields and hence high current regions along their way. During the second stage, the sum of the electric field built up by trapped charges and the field applied to the diode exceeds the dielectric breakdown threshold in some of the weakest points of the dielectric. At these points large currents start to flow, which further heat up the dielectric causing further increase in current flow. This positive feedback loop eventually results in such high trap densities, that upon dielectric breakdown, the dielectric material becomes conducting along trap paths through the dielectric [Green et al., 2001].

2.1.2 Capacitance

Capacitance-voltage (C-V) curves of MOS diodes are based on impedance measurements as a function of applied bias voltage V. The capacitance at the respective bias voltage is subsequently calculated from the corresponding impedance value via an equivalent circuit model for the diode. Normally the model consists of the capacitor of interest in parallel or in series with a resistor [Norton, 2003].

Two subtypes of C-V curves are distinguished depending on the frequency of the alternating current (AC) stimulation during the impedance measurement: The high and the low frequency curve. To understand qualitatively the shape of the ideal high and low frequency C-V curves depicted in figure 2.4, one first has to consider the three different charge carrier situations, which occur at the silicon surface during the bias voltage sweep.

The energy-band diagrams of the three cases for a p-silicon surface are depicted in figure 2.3: When the metal electrode is biased negatively with respect to the silicon ($V < 0$), the silicon valence band bends upward and is closer to the silicon Fermi level E_F. Since the carrier density depends exponentially on the energy difference (E_V-E_F) between the valence band level E_V and E_F, the band bending causes an accumulation of holes (majority carriers) near the silicon surface. This is the so-called accumulation case. When a small positive voltage ($V > 0$) is applied to the metal electrode, the valence band bends downward. The majority carriers are depleted and a space charge region forms. This is called the depletion case. When a larger positive voltage is applied, the bands bend even more downward so that the intrinsic Fermi level E_i at the surface crosses over the Fermi level E_F. Then more electrons (minority carriers) are present at the surface than holes. This is called the inversion case [Sze, 1981].

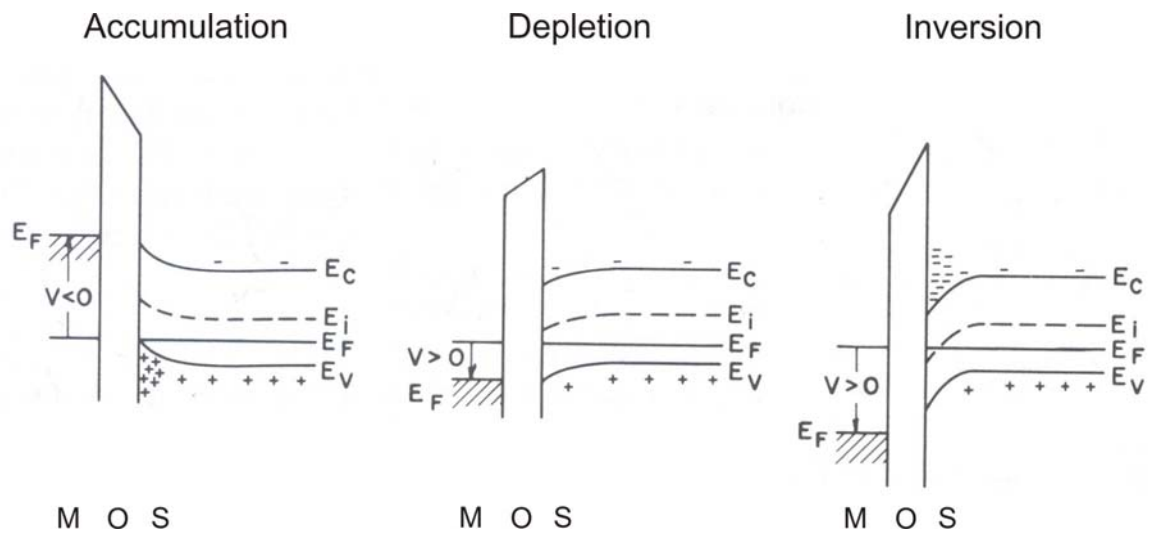


Figure 2.3: Energy-band diagrams of a p-silicon ($E_F < E_i$) MOS diode displaying the three charge carrier situations at the silicon surface, which occur during a bias voltage sweep: accumulation, depletion and inversion. In each diagram, M indicates the metal electrode, O the oxide and S the silicon. E_C and E_V stand for the silicon conduction and valence band energy, respectively. E_i stands for the Fermi energy in intrinsic silicon. E_F in both the silicon and the metal stands for the respective actual Fermi. Adapted from [Sze, 1981].

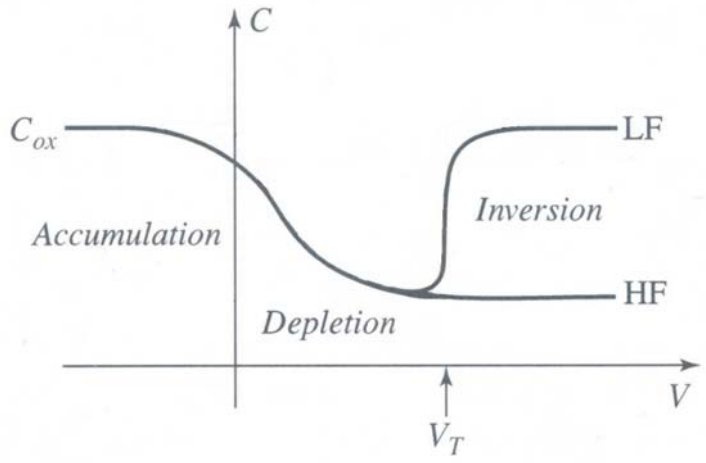


Figure 2.4: High (HF) and low frequency (LF) C-V curves of an ideal MOS diode. In both curves, the oxide capacitance C_{ox} is measured in accumulation. The threshold voltage V_T indicates the onset of inversion. Adapted from [Muller and Kamins, 2002].

As depicted in figure 2.4, ideal high and low frequency C-V curves coincide during accumulation and depletion: In accumulation, the capacitance of the MOS system is equal to the oxide capacitance C_{ox}. Upon driving the silicon surface from accumulation into depletion, the measured capacitance drops because the extending space charge region acts as a capacitor of ever smaller capacitance in series with the oxide capacitor. At the onset of inversion, the low-frequency curve begins to rise up to the initial value of C_{ox} because the

oxide capacitor is now charged and discharged by the generation and recombination of minority carriers at the silicon surface. The high frequency curve, however, stays at low capacitance values, because the minority carrier generation is too slow to follow the high frequency stimulation [Muller and Kamins, 2002].

2.1.3 Oxide charges

Figure 2.5a displays for the silicon – SiO_2 system the four types of oxide charges, which are generally present in silicon – oxide systems: (i) The interface states, which are also called interface trapped charge, are situated at the silicon – oxide interface and can exchange charges with silicon. (ii) The fixed oxide charge is located at or near (within the order of 3 nm) the silicon – oxide interface. Its value is fixed and cannot be charged or discharged over a wide variation of the silicon surface potential. (iii) The oxide trapped charge is associated with structural defects throughout the oxide. (iv) The mobile ionic charge is composed of alkali ions (K^+, Na^+) distributed throughout the oxide. However, movement of alkali ions within the bulk oxide requires device operation at high temperatures and voltages. Therefore, mobile ionic charge can be neglected in the context of this thesis [Sze, 1981].

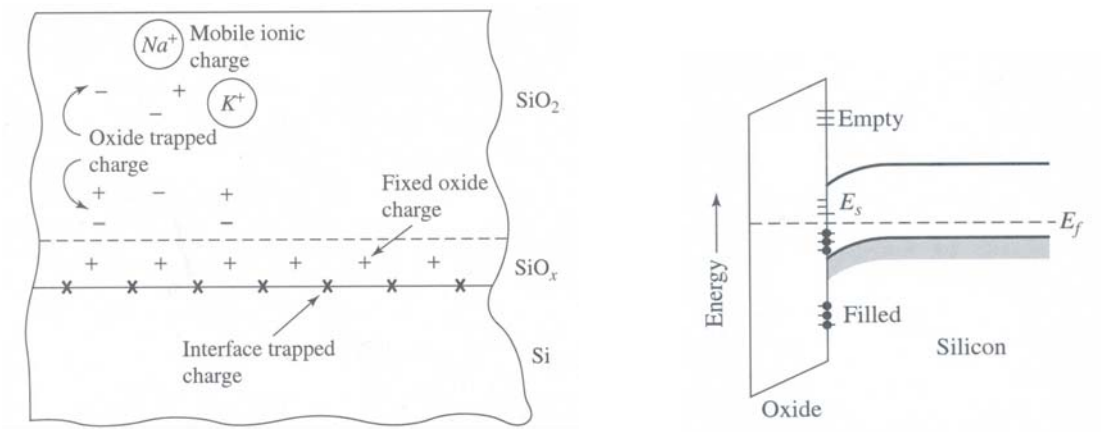
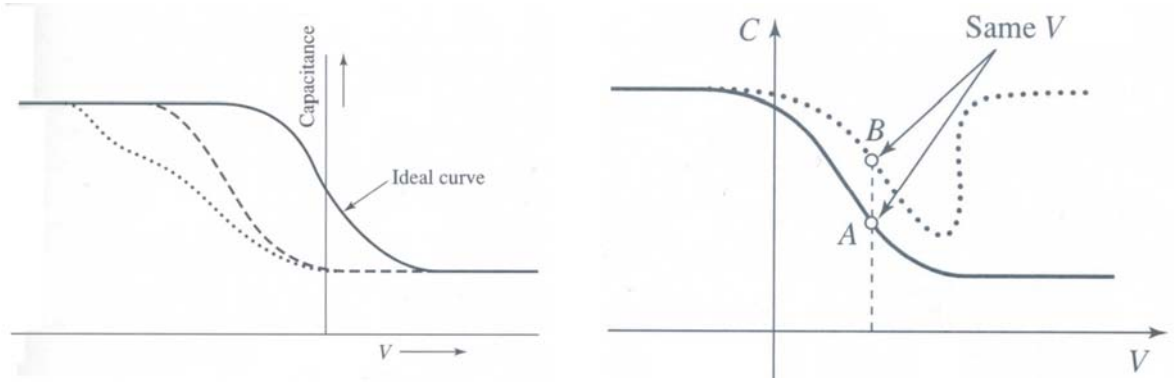


Figure 2.5a: Schematic drawing of a silicon – SiO_2 system and the four types of oxide charges contained therein: Interface trapped charge, fixed oxide charge, oxide trapped charge and mobile ionic charge. Adapted from [Sze, 1981].
b: Energy-band diagram of a silicon – oxide interface: The interface states own energy levels E_s within the silicon band gap due to the interruption of the periodic lattice structure at the silicon surface. The levels are filled up to the Fermi level E_f and empty above. Adapted from [Muller and Kamins, 2002].

As depicted in the energy-band diagram of figure 2.5b, interface states own energy levels within the silicon band gap due to the interruption of the periodic lattice structure at

the silicon surface [Sze, 1981]. When a voltage is applied, the energy levels of the interface traps move up or down with the silicon valence and conductance bands at the surface, while the Fermi level remains fixed. An interface trap is charged or discharged, when its energy level crosses the Fermi level. This change in charge contributes additionally to the capacitance of MOS diodes and alters the measured C-V curve in comparison with the ideal curve without any interface states. Hence, C-V curves allow to study interface state densities qualitatively and quantitatively.



a **b**

Figure 2.6a: The influence of oxide charges on the C-V curves of a MOS diode: The solid line represents an ideal C-V curve. The dotted line represents a low frequency curve in the presence of interface states, which is indicated by the curve stretch-out along the voltage axis and the hump at the bottom of the curve shoulder. The dashed line represents a shifted curve in the presence of fixed oxide charge or oxide trapped charge, which is unevenly distributed over the oxide. Source: [Muller and Kamins, 2002]

b: Typical high (solid line) and low (dotted line) frequency C-V curves of a MOS diode in the presence of interface states. Since interface traps can follow the stimulation in the low but not the high frequency case, higher capacitances are recorded for the low frequency curve at the same bias voltage V (e.g. compare point A and B in the curves). Adapted from [Muller and Kamins, 2002].

During high frequency C-V measurements, the charging and discharging of interface traps cannot follow the AC stimulation. However, interface traps are being charged, when their energy levels cross the Fermi level during the bias voltage sweep. Accordingly, the biasing voltage of the measurement is influenced: More charges in the metal electrode are necessary to create a given silicon surface potential. Therefore, the shoulder of an ideal C-V curve is stretched out along the voltage axis. At lower frequencies, interface traps can additionally follow the AC stimulation signal. Due to charging and discharging of interface states, the capacitance appears to be higher than the capacitance of the corresponding ideal MOS diode without interface states. Hence, in low frequency curves, a hump at the bottom of the curve shoulder indicates interface states in

addition to the curve stretch-out present at any frequency (see the dotted curve in figure 2.6a) [Muller and Kamins, 2002].

Since interface traps contribute only in the low frequency C-V curve to the capacitance, the difference between high and low frequency C-V curves (see figure 2.6b) allows to extract the value of the interface state density D_{it} as follows [Nicollian and Brews, 1982]: The resulting capacitance C_{HF} in the high frequency curve can be described as the oxide capacitance C_{ox} in series with the silicon surface capacitance C_s, which originates from the extension of the space charge region at the silicon surface:

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{2.1}$$

The resulting capacitance C_{LF} in the low frequency curve can be described by introducing the additional interface capacitance C_{it}, which originates from interface states, in parallel with C_s:

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \tag{2.2}$$

Solving equation (2.1) for C_s and inserting the result into (2.2) gives the following equation for C_{it} as a function of applied bias voltage V:

$$C_{it}(V) = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{2.3}$$

C_{it} and the interface state density D_{it} are related to each other by the elementary charge q:

$$D_{it}(V) = \frac{C_{it}(V)}{q} \tag{2.4}$$

D_{it} is actually a function of the silicon surface potential Ψ_s, whereas $D_{it}(V)$ depends also on the voltage drop over the respective oxide. For the transformation of $D_{it}(V)$ to $D_{it}(\Psi_s)$, the relation between Ψ_s and V is obtained as follows [Johnson and Worrell, 2005]: The potential at the silicon surface Ψ_s is the difference between the voltage V applied over the silicon – oxide system and the voltage drop over the oxide V_{ox}:

$$\Psi_s = V - V_{ox} \tag{2.5}$$

Since C_{ox} is a series capacitance, the voltage drop over C_{ox} is given by

$$V_{ox} = \frac{C_{LF}}{C_{ox}} \cdot V \tag{2.6}$$

C_{LF} (and not C_{HF}) is used for the calculation of Ψ_s because only in the low frequency case, where the traps follow the stimulation, the quasi-static state corresponding to V is reached at the silicon surface. Combining equations (2.5) and (2.6) gives

$$\Psi_s(V) = \int_{V_0}^{V} \left(1 - \frac{C_{LF}(V)}{C_{ox}} \right) dV \tag{2.7}$$

The integration over V is required because C_{LF} is a differential capacitance, which strongly depends on V. V_0 is the reference voltage and corresponds to the reference surface potential $\Psi_0 = \Psi_s(V_0) = 0$. In practise, the integral is approximated by exchanging dV for the voltage step size during the measurement of C_{LF}.

The fixed oxide charge can be regarded as a charge sheet located in the transition layer of the silicon – oxide interface (see figure 2.5a), which causes an additional voltage over the oxide. Hence, in comparison with ideal C-V curves, the curves of MOS diodes containing fixed oxide charge are shifted along the voltage axis as displayed by the dashed line in figure 2.6a. Furthermore, C-V curve shifts are also caused by oxide trapped charge, which is unevenly distributed over the oxide [Muller and Kamins, 2002].

The structural defects serving as oxide charge traps are either already an intrinsic property of the specific oxide film and its deposition method or have been generated during Fowler-Nordheim tunnelling. Charging or discharging of traps occurs upon voltage application through the introduction and extraction of charge carriers into and out of the oxide. Charged traps are again discharged by opposite voltage sweeps. However, the charging and discharging event of one specific trap do not occur at the same bias voltage: In both sweep directions, the charging event is delayed in comparison with the bias voltage, at which the energy levels of carrier origin and destination are equal. The reason for this is that electron tunnelling is the underlying mechanism of trap charging: The charging event is delayed by the tunnelling energy barrier. Therefore, hysteresis in C-V curves indicates the presence and the charging of traps inside the dielectric [Muller and Kamins, 2002].

2.2 The ion-sensitive field-effect transistor

Figure 2.7 depicts the schematic drawing of a p-channel ISFET in operation: Acceptor ions are implanted into regions of an n-wafer in such a way that a pnp-structure is formed. The p-regions are called source and drain. The source is defined as the p-region, which is held at higher potential during the application of a drain-source voltage V_{DS}, so that the majority carriers (holes in the p-channel ISFET) are driven from source to drain. The n-region between source and drain is covered by a thin insulating oxide film, the so-called gate oxide. During device operation a second voltage, the so-called gate-source voltage V_{GS}, is applied over the oxide layer via the source and the electrolyte. V_{GS} controls the hole density in the inversion channel (yellow area in figure 2.7) at the surface of the central n-Si region. Since the hole density in the channel determines the resistance between source and drain, the drain-source current is a strong function of the gate-source voltage. The electrical contact with the electrolyte is made by a reference electrode. In order to limit the capacitive coupling of signals into the ISFET to the area of the gate oxide, the drain and

source regions and all feed lines are shielded from the electrolyte by thick layers of so-called field-oxide.

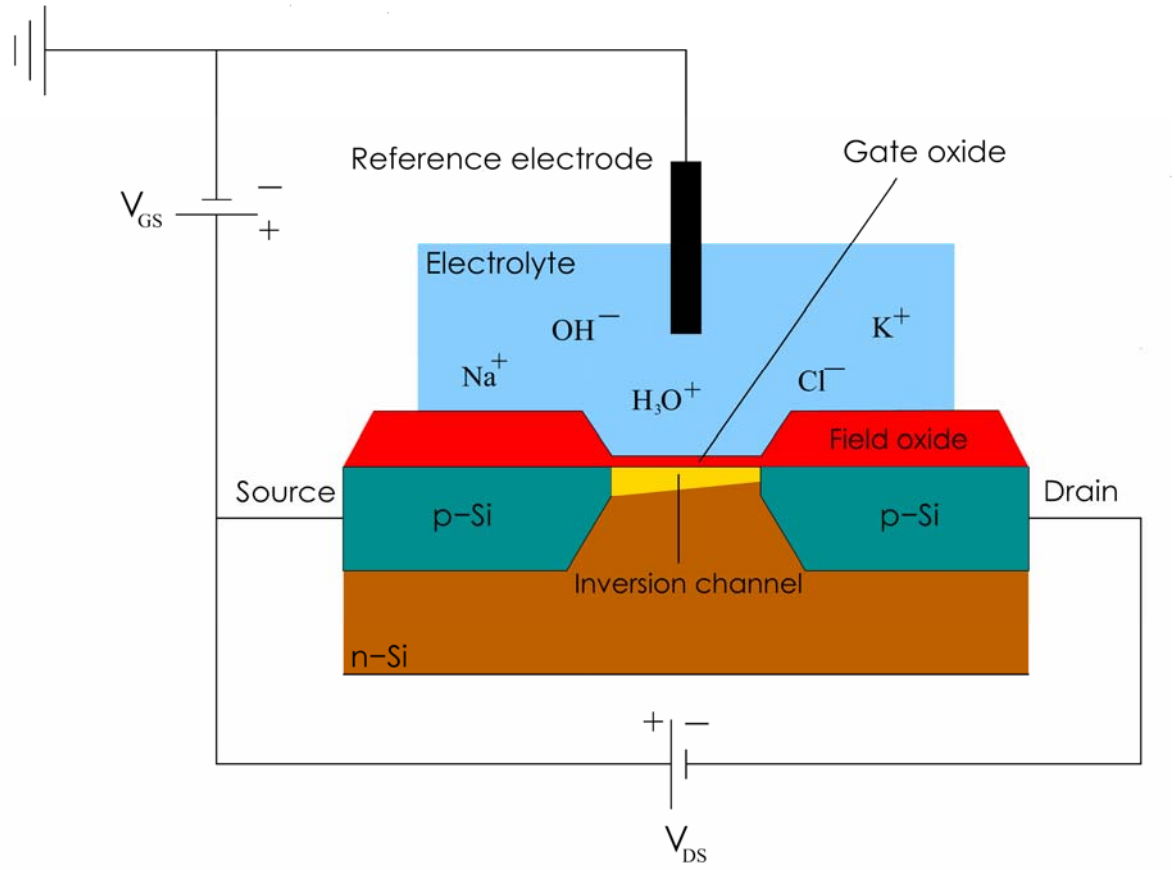


Figure 2.7: Schematic drawing of a p-channel ISFET in operation. The drain-source voltage V_{DS} is applied between source and drain, the gate-source voltage V_{GS} between gate and source. The drain-source current is a strong function of V_{GS}, because V_{GS} controls the hole density in the inversion channel (yellow area) and accordingly the channel resistance. The ground is applied to the electrolyte gate contact to avoid electrolysis.

In the following treatment of the ISFET characteristics, it will be referred solely to the p-channel ISFET, which is composed of a pnp-structure, because only p-channel devices were used in the work of this thesis. However, all considerations apply in analogous manner to the n-channel ISFET of npn-structure.

2.2.1 Characteristics

The output of an ISFET is the drain-source current I_{DS}. Since I_{DS} is a function of both voltages V_{GS} and V_{DS}, ISFETs exhibit two characteristics: The transfer characteristic

$I_{DS}(V_{GS})$ recorded at constant V_{DS} and the output characteristic $I_{DS}(V_{DS})$ recorded at constant V_{GS}. In the following, the principles of ISFET functioning are explained by considering first the course of the transfer characteristic and subsequently the course of the output characteristic.

For enhancement mode ISFETs as used in the work of this thesis, at $V_{GS} = 0$, no current flows from source to drain regardless of V_{DS} except for very low leakage current, because the pn-junction at the source is reversely biased. This is the so-called subthreshold regime in ISFET characteristics. Upon the application of an additional gate-source voltage V_{GS} however, the situation changes suddenly, when V_{GS} exceeds the threshold voltage V_T for charge carrier inversion at the surface of the central n-silicon region: Now holes (minority carriers) are attracted by the electric field, which is associated with the gate-source voltage, and form a thin inversion channel (for detailed band-diagram discussion of the charge carrier situations at the silicon surface see chapter 2.1.2). In figure 2.7, which depicts the schematic drawing of an ISFET in operation, the inversion channel is indicated by the yellow area at the silicon surface below the gate oxide. Since the channel cancels the reversely biased pn-junction at the source, considerable current starts to flow through the channel from source to drain and one says the transistor has opened [Muller and Kamins, 2002].

Increasing the gate-source voltage beyond the threshold voltage V_T causes a very strong increase in I_{DS} as seen in the transfer characteristics $I_{DS}(V_{GS})$ of figure 2.8. The underlying reason is that the density of holes in the inversion channel, which determines the drain-source resistance, is entirely controlled by the electric field associated with V_{GS} (field-effect). The V_{GS} range, in which I_{DS} strongly depends on V_{GS}, is the so-called linear regime in ISFET characteristics, because $I_{DS}(V_{GS})$ is in first order approximation a linear relation as seen in figure 2.8. Finally the transfer characteristic reaches the saturation regime, when I_{DS} ceases to increase despite the application of higher voltages. The reason for the saturation is the ever larger extension of the inversion channel into the n-doped region, which reduces the field-effect due to the ever longer distance between the gate electrode and the location of new hole generation.

Also the output characteristic exhibits a linear and a saturation regime (although the saturation cannot be seen in figure 2.8, because V_{DS} is not driven to sufficiently high voltages): In an open ISFET ($V_{GS} > V_T$), it is clear, that I_{DS} rises with increasing drain-source voltage. However, when V_{DS} exceeds $V_{GS} - V_T$, the voltage at the drain is lower than the threshold voltage for inversion. Consequently, the inversion channel becomes shorter than the channel length. Increasing V_{DS} further leads to an ever shorter inversion channel. In conclusion, I_{DS} saturates because higher V_{DS} voltages are compensated by the higher drain-source resistance due to inversion channel shortening.

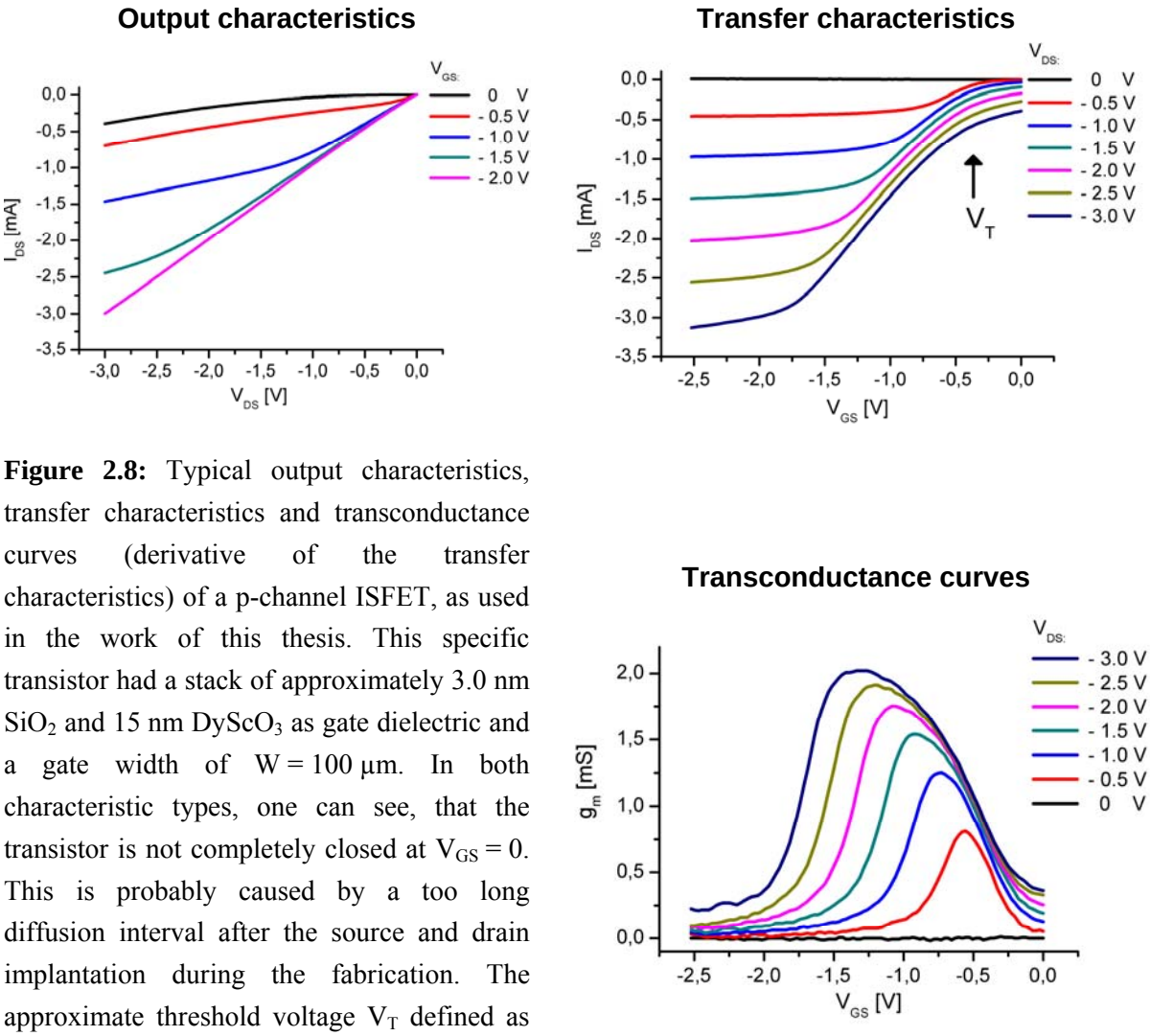


Figure 2.8: Typical output characteristics, transfer characteristics and transconductance curves (derivative of the transfer characteristics) of a p-channel ISFET, as used in the work of this thesis. This specific transistor had a stack of approximately 3.0 nm SiO_2 and 15 nm $DyScO_3$ as gate dielectric and a gate width of W = 100 µm. In both characteristic types, one can see, that the transistor is not completely closed at $V_{GS} = 0$. This is probably caused by a too long diffusion interval after the source and drain implantation during the fabrication. The approximate threshold voltage V_T defined as the onset voltage of inversion in the channel is indicated in the transfer characteristics.

In the following the simplest but useful formula for I_{DS} in the linear regime as a function of V_{GS} and V_{DS}, the long-channel field-effect transistor (FET) equation, is derived. For this purpose, initially the channel dimensions in parallel to the ISFET surface are introduced as L and W, where L is the distance between source and drain and W is the width of the channel. Upon the application of a V_{GS} voltage over the gate oxide but no V_{DS} voltage, the hole density Q_p per unit area parallel to the surface is constant over the entire length L and given by

$$Q_p = C_{ox} \cdot (V_{GS} - V_T), \tag{2.8}$$

where C_{ox} is the gate oxide capacitance per unit area. Applying additionally a drain-source voltage causes Q_p to vary over the channel length because the voltage drop over the gate oxide is now a function of the position between source and drain. Under the assumption of a linear drop of V_{DS} over L, V_{GS} is on average over the entire channel length reduced by 0.5 V_{DS}. Hence, the average hole density in the channel becomes

$$\overline{Q}_p = C_{ox} \cdot (V_{GS} - V_T - \frac{1}{2} V_{DS}) \tag{2.9}$$

The Ohmic law for the channel with its geometrical dimensions incorporated gives the channel conductance σ_{DS} as

$$\sigma_{DS} = \mu_p \overline{Q}_p \frac{W}{L}, \tag{2.10}$$

where μ_p is the hole mobility. The macroscopic Ohmic law of the inversion channel is given by

$$I_{DS} = \sigma_{DS} \cdot V_{DS} \tag{2.11}$$

Combining equations (2.9), (2.10) and (2.11) gives the long-channel field-effect transistor equation

$$I_{DS} = \mu_p C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS}, \tag{2.12}$$

which describes quantitatively very well FETs with channel lengths above 10 µm, but fails completely for channels shorter than 1 µm, where equation (2.12) must be modified considerably [Muller and Kamins, 2002].

The transconductance g_m of an ISFET is defined as the derivative of the transfer characteristic:

$$g_m = \left. \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}} \right|_{V_{DS}=const} \tag{2.13}$$

For ISFET operation, the transconductance is the most important parameter extracted from the characteristics, because it quantifies how much the ISFET signal I_{DS} changes per change in $V_{GS} - V_T$. Typical transconductance curves g_m (V_{GS}) at constant V_{DS} are shown in figure 2.8: According to the underlying transfer characteristic, the g_m value increases in the first half of the linear regime up to its maximum and decreases beyond, when the saturation regime is approached.

2.2.2 Noise

The signal in every electrical measurement system exhibits random variations over time, the so-called noise. Since noise limits the sensitivity of the measurements, it is a very important system characteristic. Due to its random character, the time course of noise is not predictable. However, noise is treated statistically as described in the following. The temporal mean of the measurement quantitiy A (t) is given by

$$\overline{A} = \lim_{T \to \infty} \frac{1}{T} \int_0^T A(t) dt \tag{2.14}$$

The variation of A from $\overline{A}$ at time t is

$$a(t) = A(t) - \overline{A} \tag{2.15}$$

The variance σ^2 of the signal A is defined as the mean square value of a (t):

$$\sigma^2 = \overline{a(t)^2} = \lim_{T\to\infty} \frac{1}{T} \int_0^T [a(t)]^2 dt \tag{2.16}$$

Independently from whether A is a current or a voltage signal, A^2 is proportional to the power of the signal. This justifies the general definition of σ^2 as the total noise power of A. Accordingly S (f) is defined as the noise power density per unit frequency band (1 Hz), which integrated over the entire frequency spectrum gives σ^2:

$$\int_0^\infty S(f) df = \sigma^2 \tag{2.17}$$

where f stands for the frequency.

The typical shape of an electrical power density spectrum is shown in figure 2.9: The peak of the δ-distribution at f = 0 corresponds to the direct current signal $\overline{A}$ and has to be substracted to gain the spectrum of the noise power density, which consists of three parts: In the low frequency region, the noise generally reduces with increasing f and very often S (f) is proportional to 1/f. Accordingly this part of the spectrum is called 1/f noise. In the medium frequency range, the noise power density is normally independent from the frequency. This is the so-called white noise regime. Since the total noise power is definitely finite, S (f) decreases fast towards very high frequencies [Müller, 1990].

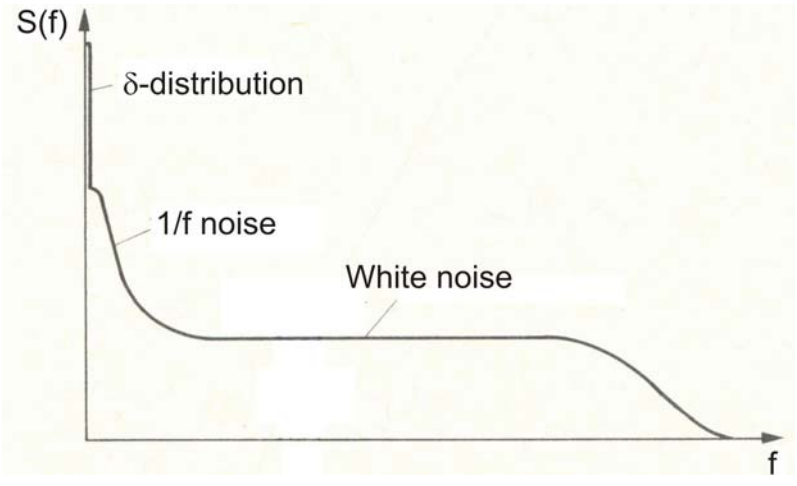


Figure 2.9: Typical shape of an electrical power density spectrum with a δ-distribution at f = 0, the subsequent 1/f noise regime, the constant white noise regime and the final decline towards very high frequencies. Adapted from [Müller, 1990].

Since many effects in electrical systems may cause 1/f noise, numerous theoretical models have been developed. In MOSFETs, the McWorther model [McWorther, 1957] is accounted for 1/f noise: As illustrated in figure 2.10, the statistical capture and emission of single inversion carriers in and from individual traps in the gate oxide causes the number of carriers in the inversion channel to fluctuate. Since the carrier number in the channel

directly determines the drain-source conductivity, these fluctuations give rise to noise in the drain-source current. The assumption of a uniform distribution of the traps in space and energy throughout the silicon – SiO_2 interface and inside the oxide, and secondly the assumption of an exponential dependence of the capture and emission rates upon the trap depth in the oxide (as valid for electron tunnelling processes) result in an expression for S, which is proportional to 1/f. In ISFETs, 1/f noise has been observed that followed the same bias dependency as in standard MOSFETs, indicating that ISFET noise is also dominated by trapping and detrapping processes at the channel – SiO_2 interface and not by other effects such as gate surface reactions [Jakobson and Nemirovsky, 1999]. An empirical equation for the 1/f noise power density S_I of FETs used by analogue circuit designers is given by

$$S_I = \frac{Mg_m^2}{C_{ox}^2 WL} \frac{1}{f^\beta}, \tag{2.18}$$

where M is an empirical parameter and β is a parameter, which is close to 1 in a wide frequency range and in any case varies in a narrow range from 0.8 to 1.2 [Tsividis, 1988]. Transferring the noise power density into the gate-source voltage power regime by dividing S_I by g_m^2 yields

$$S_V = \frac{M}{C_{ox}^2 WL} \frac{1}{f^\beta} \tag{2.19}$$

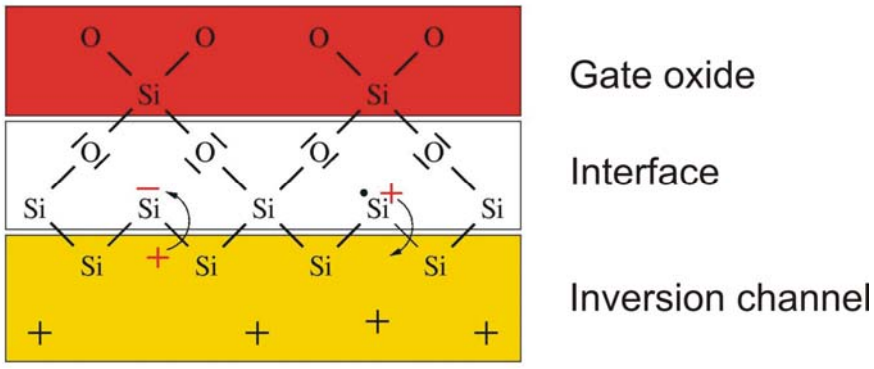


Figure 2.10: Schematic drawing of the charge carrier trapping and detrapping processes at an inversion channel – gate oxide interface, which are responsible for the 1/f noise in MOS- and ISFETs: The red plus sign to the left represents a hole, which is captured by the red electron pair, while the red plus sign to the right represents a hole, which is emitted into the inversion channel.

In FETs, 1/f noise usually dominates the noise up to frequencies on the order of several tens of kHz [Jakobson et al., 1998], which is faster than the characteristic time of electrophysiological cell signals on the order of milliseconds. Therefore, the ISFET sensitivity during cell-transistor coupling is limited by 1/f noise. In conclusion, since 1/f noise is directly related to the number of oxide traps present, high quality of the silicon –

gate oxide interface corresponding to low trap densities constitutes a crucial prerequisite for optimum recording of cell signals with ISFETs.

2.2.3 Oxide surface potential

Terminating oxygen atoms on oxide surfaces form in general OH hydroxyl-groups with hydrogen. As illustrated in figure 2.11, these surface hydroxyl-groups of an ISFET gate oxide are amphoteric and may react with both H_3O^+ and OH^- ions, the pH-determining ions of the electrolyte. The reactions result in either positively charged OH_2^+ groups or negatively charged O^- groups. Depending on which reaction prevails, which is determined by the gate oxide and the electrolyte pH, a positive or negative net charge builds up at the oxide surface. The electrostatic potential corresponding to the surface charge density σ_0 is the so-called surface potential Ψ_0.

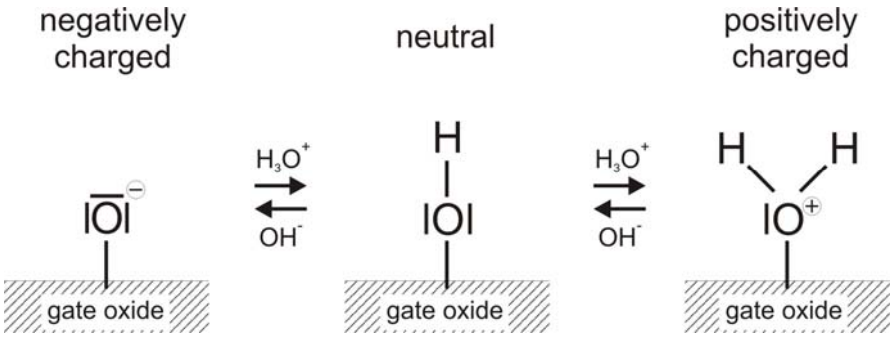


Figure 2.11: Schematic drawing of the amphoteric reactions of the terminating OH hydroxyl-goups (surface reaction sites) on oxide surfaces with the pH-determining H_3O^+ and OH^- ions of an electrolyte. The acid reaction to the right involves H_3O^+ ions and results in positively charged OH_2^+ surface groups, while the base reaction to the left consumes OH^- ions resulting in negatively charged O^- surface groups. To which extent the one reaction exceeds the other is a strong function of the pH and determines the net surface charge.

In the linear ISFET regime, the drain-source current is proportional to $V_{GS} - V_T$ (see equation (2.12)), the difference between the gate-source voltage V_{GS} and the threshold voltage V_T for the formation of the inversion channel. The ISFET is capable of measuring changes in the gate oxide surface potential due to pH changes, because the explicit expression for V_T contains Ψ_0 [Bergveld and Sibbald, 1988]:

$$V_T = E_{ref} - \Psi_0 + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}} + 2\Phi_f \qquad (2.20)$$

Φ_f is the potential difference between the actual Fermi level in the silicon between source and drain and the Fermi level in intrinsic silicon. A potential change of $2\Phi_f$ at the silicon surface is generally defined as the onset of inversion, because it corresponds to the

potential, at which the minority carrier density at the surface is equal to the majority carrier density in the bulk. All other parameters of equation (2.20) are additional voltage drops over the gate oxide, which result from the specific doping level of the silicon, the gate oxide charges, the composition of the electrolyte and the reference electrode: E_{ref} is the contribution of the reference electrode; χ^{sol} is the surface dipole potential of the electrolyte; Φ_{Si} is the silicon electron work function; q is the elementary charge; C_{ox} is the capacitance of the gate oxide; Q_{ox}, Q_{ss} and Q_B are the charges located in the oxide, the charges located in interface states and the depletion charge, respectively.

Upon electrolyte pH changes, all contributions in equation (2.20) are constant except for Ψ_0 and χ^{sol}. Moreover, since the changes in χ^{sol} are negligible in comparison with Ψ_0 changes, the ISFET drain-source current is in its linear regime a linear function of the gate oxide surface potential Ψ_0 [van Hal et al., 1996]. In the following, a general model of $d\Psi_0/dpH_B$, the change in surface potential per unit bulk electrolyte pH (pH_B) change, is described. The quantity $d\Psi_0/dpH_B$ is called the pH sensitivity of the respective oxide. The model was developed by [van Hal et al., 1996] and agrees very well with experimental data.

The potential difference Ψ_0 between the by definition grounded bulk electrolyte and the oxide surface causes a proton concentration difference between bulk and surface that is according to Boltzmann

$$a_{H_S^+} = a_{H_B^+} \exp\frac{-q\Psi_0}{kT} \tag{2.21}$$

where $a_{H_i^+}$ is the respective activity of H^+ (protons), the subscripts B and S refer to the bulk and the surface, respectively, k is the Boltzmann constant and T is the absolute temperature. Transformation of equation (2.21) yields the Nernst equation, which describes the relation at equilibrium between Ψ_0 and the corresponding difference in pH between bulk and surface:

$$\Psi_0 = \frac{2.3kT}{q}(pH_S - pH_B) \tag{2.22}$$

with (2.3kT/q) = 59 mV at room temperature T = 300 °K.

Now the two parameters of the model for the pH sensitivity $d\Psi_0/dpH_B$ are introduced: The intrinsic buffer capacity β_{int} is a material constant of the respective oxide and defined as the density of surface binding sites (surface oxygen atoms), which is being charged per unit surface pH change:

$$\beta_{int} = \frac{-1}{q}\frac{d\sigma_0}{dpH_S} \tag{2.23}$$

Because of charge neutrality, an equal but opposite charge with respect to σ_0 is built up in the electrolyte solution at the interface (see figure 2.12). The two charges form the so-called double-layer capacitance C_{DL}, which is the second parameter in the model. Its

magnitude is a property of the electrolyte and describes the amount of charge delivered from the bulk electrolyte to the interface upon a change in the surface potential:

$$C_{DL} = \frac{d\sigma_0}{d\Psi_0} \tag{2.24}$$

Combining equation (2.23) and (2.24) yields the equation for the sensitivity of Ψ_0 to pH changes at the oxide surface:

$$\frac{d\Psi_0}{dpH_S} = -\frac{q\beta_{\text{int}}}{C_{DL}} \tag{2.25}$$

Combining the Nernst equation (2.22), which gives the relation between pH_S and pH_B, and equation (2.25) yields after some transformations the final expression for the oxide pH sensitivity at room temperature:

$$\frac{d\Psi_0}{dpH_B} = -\alpha \cdot 59mV \tag{2.26}$$

with

$$\alpha = \left(\frac{59mV \cdot C_{DL}}{q\beta_{\text{int}}} + 1 \right)^{-1} \tag{2.27}$$

α is a dimensionless sensitivity parameter with values between 0 and 1. The magnitude of β_{int} and C_{DL} relative to each other determines the deviation of the pH sensitivity from Nernstian behaviour, which corresponds to $d\Psi_0/dpH = 59$ mV: In case $(q \cdot \beta_{int}) >> 59\ \text{mV} \cdot C_{DL}$, the buffer capacity of the oxide is sufficiently large to store the entire charge delivered upon pH changes from the bulk electrolyte to the oxide surface, leading to Nernstian behaviour. However, if $q \cdot \beta_{int}$ is on the order of $59\ \text{mV} \cdot C_{DL}$, the buffer capacity is too small to store the entire charge, resulting in pH sensitivities less than 59 mV/pH. In the following, it will be discussed, how β_{int} and C_{DL} are related to the structure and composition of the specific gate oxide and employed electrolyte solution.

According to the site-binding model [Yates et al., 1974], the charging of oxide surfaces is the result of a thermodynamic equilibrium between the surface hydroxyl-groups (surface reaction sites) and the H_3O^+ and OH^- ions of the electrolyte. The corresponding surface reactions are shown in figure 2.11. According to the law of mass action, the surface reaction site fractions, that are O^--, OH- or H_3O^+-terminated, are described by the dissociation constants K_a and K_b for the acid and the base reaction, respectively, of figure 2.11. Further introducing the density of reaction sites N_s and the surface proton activity $a_{H_S^+}$ allows to express the surface charge density σ_0 as a function of the oxide properties N_s, K_a and K_b and the electrolyte pH. Final differentiation of σ_0 to pH gives the pH-dependent intrinsic buffer capacity of an oxide as

$$\beta_{\text{int}} = N_s \frac{K_b a_{H_S^+}^2 + 4K_a K_b a_{H_S^+} + K_a K_b^2}{(K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2)^2} 2.3 a_{H_S^+} \tag{2.28}$$

Several models of the double-layer capacitance at a solid – electrolyte interface have been reported. The most elaborate is the Gouy-Chapman-Stern model, which describes the compensation of a surface charge by two consecutive layers of counterions as depicted in figure 2.12: In the inner so-called Stern layer the ions are directly adsorbed to the surface and immobile. By contrast, the outer so-called diffuse layer is composed of mobile ions, which obey Poisson-Boltzmann statistics [Stern, 1924].

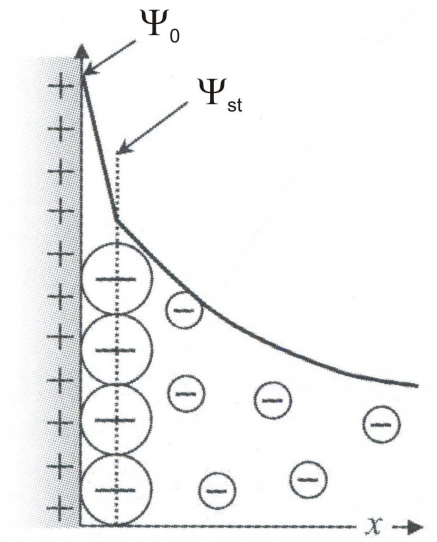


Figure 2.12: Schematic drawing of the counterion concentration and the course of the electrostatic potential in an electrolyte as a function of the distance x from a charged surface according to the Gouy-Chapman-Stern model. The distance between the dotted line and the surface represents the half of the hydrated ion radius, which defines the thickness and thereby the voltage drop in the Stern layer. The counterion concentration in the outer diffuse layer follows Poisson-Boltzmann statistics, which results for sufficiently low surface potentials (< 50 – 80 mV) in an exponential decline of the electrostatic potential starting from the potential Ψ_{St} at the Stern layer – diffuse layer interface. Adapted from [Butt et al., 2003].

The capacitance per unit area of the Stern layer C_{St} can be estimated by the plate capacitor formula: Introducing the half of the hydrated ion radius r_{ion} as the relevant distance between the charge sheets (see the dotted line in figure 2.12) yields

$$C_{St} = \frac{2\varepsilon_0 \varepsilon_{St}}{r_{ion}} \tag{2.29}$$

where ε_0 is the permittivity of vacuum and ε_{St} is the dielectric constant in the Stern layer, which is reduced with respect to the bulk electrolyte.

According to the Boltzmann equation, the ion concentrations $c_i(x)$ in the diffuse layer as a function of the distance x from the Stern layer – diffuse layer interface are given by

$$c_i(x) = c_i^0 \exp\left(\frac{-z_i q \Phi(x)}{kT}\right) \tag{2.30}$$

where i indicates the ion species present in the electrolyte, c^0 and z stand for the respective bulk concentration and valence, and Φ is the electrostatic potential. Combining the Boltzmann equation (2.30) with the Poisson equation, which relates the charge density with the potential, yields the Grahame equation, which expresses the surface charge density as a function of the potential at the Stern layer – diffuse layer interface Ψ_{St}. For a monovalent 1:1 salt the Grahame equation is given by:

$$\sigma_0 = \sqrt{\left(8kT\varepsilon_0\varepsilon_B c^0\right)}\sinh\left(\frac{q\Psi_{St}}{2kT}\right) \tag{2.31}$$

where ε_B is the dielectric constant of the bulk electrolyte and c^0 is the bulk salt concentration. Differentiating the Grahame equation (2.31) gives the differential capacitance of the diffuse layer C_{DL} as

$$C_{DL} = \sqrt{\frac{2q^2\varepsilon_0\varepsilon_B c^0}{kT}}\cosh\left(\frac{q\Psi_{St}}{2kT}\right) \tag{2.32}$$

Since Stern and diffuse layer are two capacitances in series, the total differential double layer capacitance in the Gouy-Chapman-Stern model is given by

$$C_{DL} = \left(\frac{r_{ion}}{2\varepsilon_0\varepsilon_{St}} + \frac{1}{\left(\frac{2q^2\varepsilon_0\varepsilon_B c^0}{kT}\right)^{\frac{1}{2}}\cosh\left(\frac{q\Psi_{St}}{2kT}\right)}\right)^{-1} \tag{2.33}$$

The surface reaction sites of oxides are most reactive to the pH-determining ions H_3O^+ and OH [Bergveld and Sibbald, 1988]. However, counter ions are assumed to adsorb onto the resulting charged surface groups and to make an additional contribution to the surface potential [Bergveld and Sibbald, 1988; Vlasov et al., 2003]. During electrical activity of electrogenic cells, primarily K^+ and Na^+ ion currents flow over the membrane, which consequently change the K^+ and Na^+ ion concentration in the cleft between the ISFET gate and the cell [Wrobel et al., 2005]. Accordingly, it is believed that the oxide surface potential is altered during cell-transistor coupling by the reaction of K^+ and Na^+ ions with negatively charged O^- surface groups as displayed in figure 2.13. In analogy with the pH sensitivity, the pK and pNa sensitivities of oxides are defined as $\left.\frac{d\Psi_0}{dpK}\right|_{pH,pNa=const}$ and $\left.\frac{d\Psi_0}{dpNa}\right|_{pH,pK=const}$, respectively.

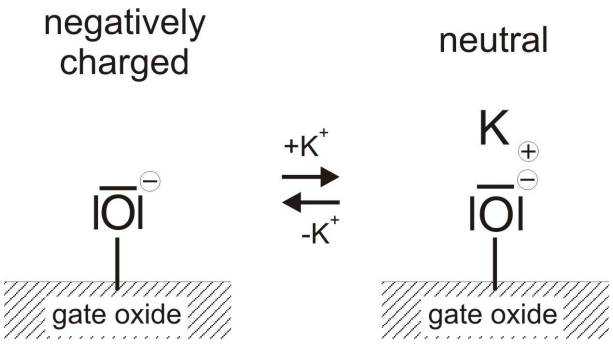


Figure 2.13: Schematic drawing of the reaction, which determines the pK sensitivity of oxides: A negatively charged O^- surface group is compensated by a K^+ ion. Replacing K^+ by Na^+ gives the reaction, which in analogous manner is responsible for the pNa sensitivity of oxides.

2.2.4 Long-term drift

During ISFET operation a slow and monotonic change in the threshold voltage is generally observed, the so-called drift. It occurs over several hours, during which its velocity reduces continuously. Its time course is normally described very well by an exponential decay with drift velocities on the order of 10 mV/min at the beginning of the operation.

Several reasons can be responsible for ISFET drift [Jakobson et al., 2000]: For instance changes in the reference electrode potential due to leakage currents, which polarise the reference electrode, or temperature variations possibly induced by drain-source current heating. However, the most important origin is the so-called inherent drift, which is also responsible for the varying drift behaviour of ISFETs with different gate oxides. Due to experimental indications, it is generally assumed, that a hydrated surface layer forms in oxides, that are exposed to an aqueous solution. During exposure for hours, the hydrated layers are believed to reach thicknesses on the order of several nanometres [Jamasb et al., 1998]. The ion species, which are according to their charge attracted by the gate-source voltage, penetrate the hydrated layer, thereby reducing the effective thickness of the gate oxide. Consequently the oxide capacitance C_{ox} increases, which according to equation (2.12) is proportional to the drain-source current.

The long-term drift has no detrimental effects on cell-transistor coupling experiments, because cell signals have characteristic times on the order milliseconds, while the drift can be compensated via an electronic feed-back loop with a characteristic time on the order of 10 seconds. During the detection of charged biomolecules with ISFETs, however, drift is the main noise source and may cover the measurement signals: The establishment of the equilibrium surface potential during biomolecule experiments takes times on the order of seconds to minutes and the corresponding signals are on the order of only several mV. Simply waiting for the saturation of the drift does not necessarily solve the drift problem, because the inevitable solution exchange upon the administration of the

biomolecules to be detected causes new drift, although to less a degree than at the beginning of the operation.

2.3 The coupling of bioelectronic signals to ISFETs

2.3.1 Charged biomolecule detection

In the following, the theory of the electronic detection via ISFETs of both highly charged polyelectrolytes, which serve as DNA model, and of the negatively charged DNA itself is described. In both cases the ISFET signals originate from adsorption of the respective charged macromolecule to the gate surface. The signal magnitude is determined by the charge density of the involved macromolecule. Since polyelectrolytes possess a considerably higher charge density than DNA, they constitute an excellent model system to demonstrate the feasibility of DNA detection with ISFETs by proof of principle. Furthermore, polyelectrolyte detection experiments with large signals are suited to study the currently debated mechanisms underlying DNA detection.

In the normal polyelectrolyte experiments, the macromolecules adhere due to physical adorption caused by the electrostatic interaction with an oppositely charged gate surface. For these experiments, the surface charge can be tuned by choosing the gate oxide or silanising the oxide surface with a silane layer that terminates with an acid or base chemical group, and by setting the pH of the polyelectrolyte solution.

By contrast, the special polyelectrolyte DNA adheres to the gate surface due to chemical adsorption: Single-stranded (ss) DNA molecules are detected by their respective sequence of the four nucleobases adenine (A), thymine (T), cytosine (C) and guanine (G), which contains the genetic information. In the base pairing (hybridisation) reaction between two ssDNAs, the bases adenine and thymine bind to each other via two hydrogen, while cytosine and guanine bind to each other via three hydrogen bonds. The affinity between two ssDNAs is optimum when they are complementary to each other, which means that all bases along their sequences match for binding. However, the binding affinity strongly decreases when one or more base pairs along a short DNA molecule do not match. In the preparation of DNA detection experiments, so-called probe ssDNA is immobilised onto the gate oxide by chemical surface modification and covalent binding via crosslinker molecules. During the actual detection measurement, the gate is exposed to the sample solution containing the so-called target ssDNA. Because of the high specificity of the hybridisation reaction, only the ssDNA, which is fully complementary to the probe ssDNA, or ssDNAs with very few mismatches adsorb to the gate and evoke an ISFET signal. For DNA chips, usually an array of different probe ssDNA sequences is used. By knowing the position and the sequence of the immobilised probe ssDNAs, the unknown sequence of target ssDNAs can be determined. In conclusion, it is the specificity of the

DNA hybridisation reaction, which allows to examine whether a certain DNA sequence is present in the sample solution or not.

Although it is well-known that the adsorption of the charged polyelectrolyte and DNA molecules to the gate surface constitutes the basis of the ISFET detection signals, the dominating signalling mechanism itself is unknown. Currently, three mechanisms of how the adsorption signals primarily couple into the ISFET are discussed [Landheer et al., 2005; Poghossian et al., 2005; Poghossian et al., 2006]: (i) The intrinsic charge of the adsorbing macromolecules changes the gate surface potential of the ISFET leading to a change in the ISFET threshold voltage. (ii) The adsorption of the macromolecules leads to a displacement of the electrolyte from the ISFET channel and accordingly to a decrease in the effective gate capacitance. (iii) The adsorption of the charged macromolecules attracts counterions and causes ion redistribution in the intermolecular spaces. The corresponding ion concentration and in particular pH changes at the gate surface evoke changes in the surface potential.

2.3.2 Electrogenic cells

Electrogenic cells are biological cells, which are electrically active. Three types of electrogenic cells are distinguished: neurons from the brain, skeletal myocytes from skeletal muscles and cardiomyocytes from the heart. In all three cell types, the electrical activity is based on ionic currents over the cell membrane.

All biological cells are surrounded by an approximately 5 nanometre thick cell membrane, which separates the intracellular aqueous solution, the cytosol, from the extracellular aqueous solution. Figure 2.14 depicts the schematic drawing of a cell membrane: It is formed by a double layer of phospholipids, which are composed of a hydrophilic head group and a hydrophobic tail. The phospholipids are arranged in the energetically most favourable way: The hydrophilic head groups face both the intracellular and the extracellular aqueous solution, while the hydrophobic tails are screened from the aqueous solutions.

The ionic composition of the cytosol and the extracellular medium differ considerably. Figure 2.15 gives typical cytosolic and extracellular concentrations of a mammalian cell for K^+, Na^+, Ca^{2+} and Cl^-, which are the ion species primarily involved in the electrical activity of electrogenic cells. Furthermore, the arrows in figure 2.15 indicate the direction of the respective negative ion concentration gradient, i.e. the direction of the respective diffusive transport over the cell membrane.

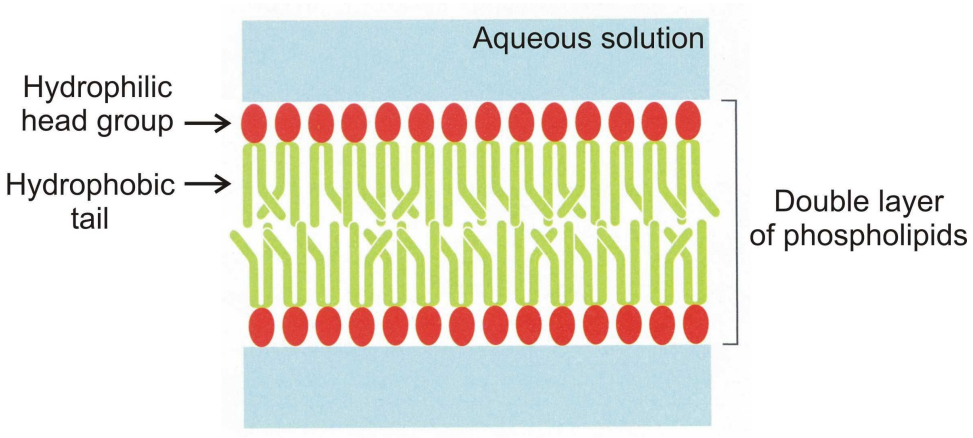


Figure 2.14: Schematic drawing of a cell membrane: The hydrophilic head groups (red ellipses) of the phospholipids face the cytosol and the extracellular medium, while the hydrophobic tails (green lines) are screened inside the double layer. Adapted from [Alberts et al., 2004].

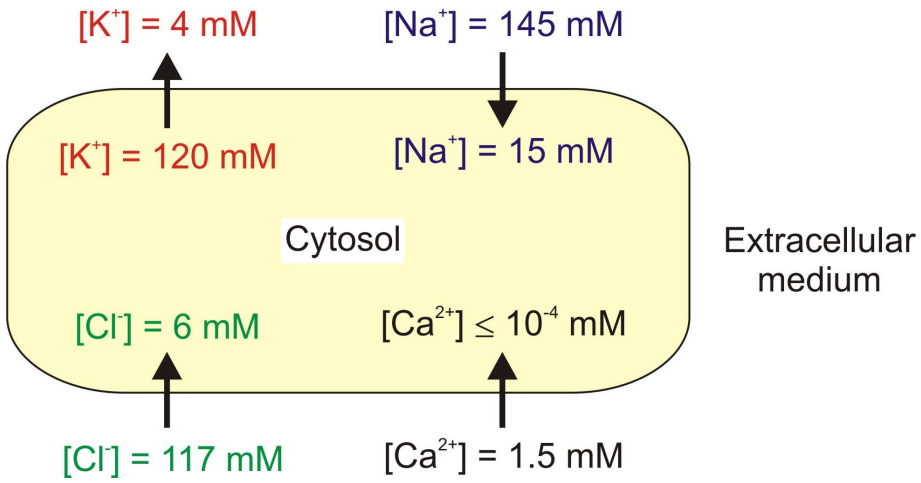


Figure 2.15: Schematic drawing of the cytosolic and extracellular K^+, Na^+, Ca^{2+} and Cl^- concentrations in mammalian cells. The arrows indicate the corresponding negative concentration gradients, which constitute the basis of electrical activity in electrogenic cells. Adapted from [Greger, 2001].

The large concentration gradients ranging from one order of magnitude for Na^+ up to four orders of magnitude for Ca^{2+} (see figure 2.15) are established and maintained by so-called active transport proteins. These proteins are incorporated into the cell membrane and continuously transport ions against their negative concentration gradient over the membrane. Two types of active transport are distinguished: During primary active transport, the energy required for the ion transfer is gained from the breakdown of phosphate compounds such as adenosine triphosphate (ATP). In contrast, secondary active transport utilises the energy, which is released during the transfer of one ion species along

its negative concentration gradient, to transport another species against its negative concentration gradient over the membrane.

The membrane potential is defined as the difference in electrostatic potential between the cytosol and the extracellular medium, i.e. the voltage drop over the membrane. It is primarily determined by the concentration gradient of the ion species with the highest permeability through the membrane: Due to diffusion, this ion species flows along its negative gradient to balance the concentrations. However, the net flow charges the cytosol and the extracallular space violating electroneutrality. Therefore, the net flow along the negative concentration gradient dies down, when the membrane potential has reached the electrochemical equilibrium potential E^B described by the Nernst equation at room temperature:

$$E^B = \frac{59mV}{z_B} \cdot \ln \frac{[B]_{in}}{[B]_{out}}, \tag{2.34}$$

where B stands for the ion species with the highest permeability over the cell membrane, [B] is the concentration of B, the subscripts in and out refer to the intracellular and the extracellular medium, respectively, and z_B is the valence of ion species B.

For most cells and in particular also for electrogenic cells at rest, i.e. during the absence of electrical activity, K^+ is the ion species with the highest membrane permeability. Since $[K^+]_{in} >> [K^+]_{out}$, the so-called resting potential is generally negative. It lies near E^{K^+} and the observed values range from -120 to -40 mV [Schmidt and Thews, 1995]. The idealisation of considering only the ion species with the highest membrane permeability causes the true resting potential to deviate from equation (2.34). The exact resting potential V_R is calculated by considering all ion species with non-negligible concentration gradients and permeabilities. Normally only the monovalent K^+, Na^+ and Cl^- ions are relevant giving the so-called Goldman equation at room temperature as

$$V_R = 59mV \cdot \ln \frac{P^K[K^+]_{out} + P^{Na}[Na^+]_{out} + P^{Cl}[Cl^-]_{in}}{P^K[K^+]_{in} + P^{Na}[Na^+]_{in} + P^{Cl}[Cl^-]_{out}}, \tag{2.35}$$

where P stands for the respective ionic permeability through the membrane in the absence of electrical activity.

The electrical activity of electrogenic cells consists of transients in the membrane potential away from the resting potential, the so-called action potentials (AP). The transients are caused by the opening of pores in the membrane, the so-called ion channels, which selectively permit only one specific ion species to traverse the membrane by diffusive transport. Due to the opening of channels, suddenly the corresponding ion species has the highest membrane permeability. Consequently, the membrane potential moves towards the electrochemical potential of this ion species, which is determined by the cytosolic and extracellular ion concentrations according to the Nernst equation (2.34).

Ion channels are made of proteins. Three types are distinguished: voltage-gated channels, which open when the membrane exceeds the corresponding threshold voltage; ligand-gated channels, which open when the corresponding specific ligand (binding-partner) has bound; and stretch-activated channels, which open in response to mechanical stress. Generally the opening and closing of several ion channels for different ion species is involved in APs. The sequence of channel openings and closings determine the time course of the membrane potential during the AP. Common to the AP of all electrogenic cells is that it ends with the highest membrane permeability of the ion species, which determines the resting potential, causing the membrane potential to return to the resting potential.

2.3.3 The extended point-contact model of the cell-transistor coupling

The point-contact model was originally developed by [Regehr et al., 1989] for the coupling of indium tin oxide multi electrode arrays with electrogenic cells. Upon its application to cell-transistor coupling, however, discrepancies have been reported between predictions of the purely electrical model, which were based on membrane currents measured by the patch-clamp technique, and the corresponding actual ISFET recordings [Vassanelli and Fromherz, 1999; Straub et al., 2001]. Basically, these discrepancies consist firstly in the experimental observation of slow ISFET signal components not present in the corresponding membrane current: During both the onset and the end of potassium recordings, the ISFET reaches the respective steady-state signal much slower than the potassium current in the patch-clamp recording. Secondly, the ISFET records higher signal amplitudes than predicted by the model. Recent publications [Brittinger and Fromherz, 2005; Wrobel et al., 2005] suggest changes in the gate oxide surface potential due to ion concentration changes in the narrow space between cell and gate during potassium signals to account for these discrepancies. In the following, the current model of the cell-transistor coupling is described, which consists of two components: the traditional point-contact model [Regehr et al., 1989] and the simulation of ion concentration changes in the cleft [Brittinger and Fromherz, 2005; Wrobel et al., 2005], which alters the oxide surface potential.

Figure 2.16 shows the equivalent circuit of the traditional, purely electric point-contact model. According to its name, the model describes the contact between cell and ISFET by a single point. The potential of this point, which is located in the cleft between cell membrane and gate, constitutes the ISFET input and is called junction potential V_J. Moreover, the model contains three further distinct potentials in specific points: The membrane potential V_M in the cytosol, the voltage V_S applied to the source and the ground in the bath electrolyte. The electrical circuit elements modelling cell membrane, cleft and gate oxide, which couple these potentials with each other, are described in the following.

Both the so-called junction membrane (JM), which connects V_M with V_J, and the free membrane (FM), which connects V_M with the bath electrolyte, are represented by so-called Hodgkin-Huxley elements [Hodgkin and Huxley, 1952]: C_{JM} and C_{FM} are the respective membrane capacitances, which have values per unit area on the order of 1 µF cm^{-2} [Adam et al., 1988]. In parallel to C_{JM} and C_{FM}, G_{JM}^{i} and G_{FM}^{i} are the membrane conductances of all ion species i relevant during the AP. G_{JM}^{i} and G_{FM}^{i} are time-dependent and determined by the status (open or closed) of the respective ion channel. The electrochemical potentials E^{i}, which drive the membrane DC currents of the ion species i, are determined by the corresponding ion concentration gradients over the membrane according to the Nernst equation (2.34).

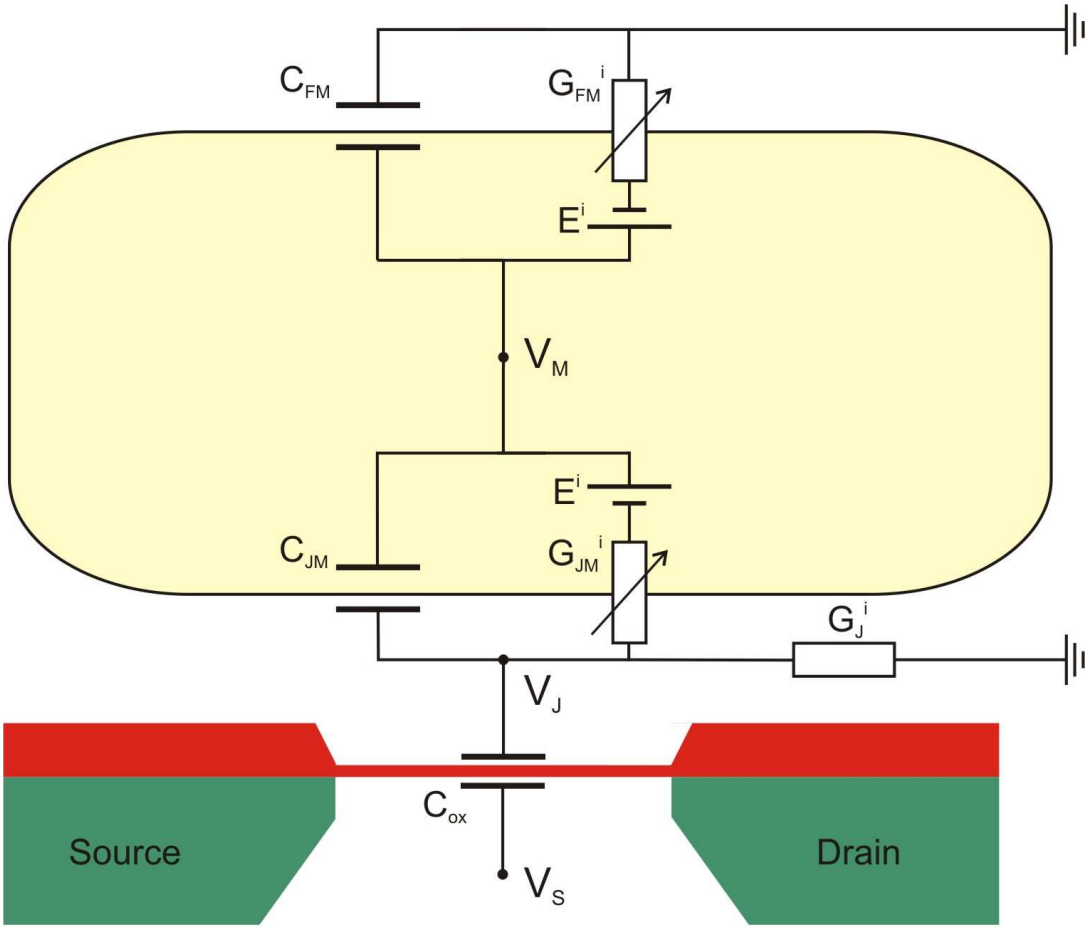


Figure 2.16: Equivalent circuit of the purely electric point-contact model containing the following distinct potentials: The membrane potential V_M in the cytosol, the junction potential V_J in the cleft, the potential V_S applied to the source and the ground in the bath electrolyte. These potentials are connected with each other via the Hodgkin-Huxley elements representing the cell membrane, the junction conductance G_J between cleft and bath electrolyte and the gate capacitance C_{ox}. Adapted from [Wrobel et al., 2005].

The cleft between membrane and gate, which connects V_J and the bath electrolyte, has heights on the order of 60 to 110 nm [Braun and Fromherz, 1998]. Because of its small height, the cleft constitutes a resistor, which is in the equivalent circuit of figure 2.16 represented by the junction conductance G_J. Finally, V_J and V_S are coupled to each other via the capacitance of the gate oxide C_{ox}.

According to Kirchhoff´s law of electroneutrality, the sum of all currents into and out of the cleft (contact point), i.e. the ohmic and capacitive membrane current I_M^O and I_M^C, the current I_{ox} over the gate oxide and the junction current I_J from the cleft into the bath electrolyte, equalises:

$$\begin{aligned} 0 &= I_M^O + I_M^C + I_{ox} - I_J \\ &= \sum_i G_{JM}^i \left(V_M(t) - V_J(t) - E^i\right) + C_{JM} \cdot \frac{d\left(V_M(t) - V_J(t)\right)}{dt} + C_{ox} \cdot \frac{dV_J(t)}{dt} - G_J V_J(t) \end{aligned} \tag{2.36}$$

Equation (2.36) can be simplified by two approximations [Ingebrandt et al., 2005]: Firstly, the capacitive current over the gate oxide is negligible:

$$C_{ox} \cdot \frac{dV_J(t)}{dt} \approx 0 \tag{2.37}$$

Secondly, V_J is much smaller than V_M leading to

$$V_M(t) - V_J(t) \approx V_M(t) \tag{2.38}$$

Inserting equation (2.37) and (2.38) into (2.36) gives the expression for the junction potential in the point-contact model:

$$V_J(t) = \frac{1}{G_J}\left(\sum_i G_{JM}^i \left(V_M(t) - E^i\right) + C_{JM} \cdot \frac{dV_M(t)}{dt}\right) \tag{2.39}$$

Equation (2.39) shows the high impact, which the junction conductance G_J has for the signal magnitude in cell-transistor coupling: The smaller G_J, the larger is the ISFET input signal V_J. Hence, for optimum cell-transistor coupling, it is crucial that the gate is sealed excellently from the bath electrolyte, which is provided primarily by the body of the recorded cell, but in a dense layer also by adjacent cells.

Due to the small volume of the cleft between cell membrane and gate oxide, the influx of K^+ ions from the cytosol and the drain of Na^+ ions into the cytosol during an AP changes the ion concentrations c_J^i in the cleft. The Nernst-Planck-Poisson theory describes the c_J^i (**r**, t) and the corresponding electrostatic potential Ψ (**r**, t), which are functions of location **r** and time t, by the following two coupled differential equations [Wrobel et al., 2005]: The Nernst-Planck equation correlates the changes in the c_J^i with the source terms λ_i, which represent the ionic currents over the cell membrane between cleft and cytosol due to electrical cell activity, and the ionic currents between cleft and bath electrolyte, which are induced by diffusion and potential gradients:

$$\frac{\partial c_J^i}{\partial t} = D_i \nabla \cdot \left(\nabla c_J^i + c_J^i \frac{z_i F}{RT} \nabla \Psi\right) + \lambda_i, \tag{2.40}$$

where D_i and z_i stand for the respective diffusion coefficients and valences, F and R for the Faraday and the gas constant, and T for the absolute temperature. The first and the second summand in the bracket constitute the diffusion term and the ohmic current term, respectively. The Poisson equation gives the relation between the net charge concentration and the corresponding potential:

$$\Delta\Psi = -\frac{4\pi F}{\varepsilon}\sum_i z_i c_J^i \,, \tag{2.41}$$

where ε is the dielectric constant of the solution. The boundary conditions required for the solution of the equations (2.40) and (2.41) are given by the cleft geometry.

However, the system of coupled differential equations (2.40) and (2.41) cannot be solved in a simple analytical way. Therefore, numerical approximations have been used to calculate the ion concentrations in the cleft for a K^+ source term, which corresponds to typical K^+ currents flowing during electrical cell activity from the cytosol into the cleft [Wrobel et al., 2005]. Another solution, which used a similar K^+ source term, was based on Nernst potentials between the cleft and the bulk instead of the Poisson equation [Brittinger and Fromherz, 2005], although the Nernst equation is only defined across a membrane in a static state with no current flowing.

According to both calculations, the K^+ concentration in the cleft rises 6 to 12 mM above the original cleft concentration of approximately 4 mM. Such large relative concentration changes in c_J^i (up to three fold the original bulk electrolyte concentration c_0^i) definitely generate an additional ISFET signal due to the ion sensitivity of the gate oxide (for details see chapter 2.2.3), which is not considered in the purely electrical point-contact model underlying equation (2.39). Consequently, the effective junction potential is approximated by the following equation [Ingebrandt, 2001]:

$$V_J(t) = \frac{1}{G_J}\left(\sum_i G_{JM}^i\left(V_M(t) - E^i\right) + C_{JM}\cdot\frac{dV_M(t)}{dt}\right) + \sum_i \frac{d\Psi_0}{dpi}\cdot\log\frac{c_J^i(t)}{c_0^i} \tag{2.42}$$

The first summand in equation (2.42), which is equal to equation (2.39), represents the electrical contribution to V_J according to the point-contact model (equivalent circuit of figure 2.16). The second summand represents the signal contribution of the ion sensitivities $\frac{d\Psi_0}{dpi}$ of the ISFET to the ion species i, where the pi are the negative base-10 logarithms of the corresponding ion concentrations.

In both publications mentioned in the last paragraph, not only the ion concentrations c_J^i in the cleft, but also the time course of the electrical signal component of V_J has been simulated with the following results: The time course of the simulated electrical signal matches the experimentally observed fast ISFET signal component, which closely follows the time course of the corresponding membrane currents recorded by the patch-clamp technique. The simulated time course of the c_J^i is significantly slower than the electrical signal, however, it is still faster than the experimentally observed slow ISFET

signal component. To explain this deviation, slow kinetics of the ion surface binding reactions have been suggested [Brittinger and Fromherz, 2005]. In conclusion, it is believed that the ion sensitivity of the gate oxides combined with the characteristic diffusion time in the cleft during the particular experiment account for the slow signal components in cell-transistor coupling.

3 Materials and Methods

3.1 Thin dielectric film fabrication

3.1.1 Thermally grown ultrathin SiO_2 films

For high capacitance thin films the following structure was used: silicon – thermally grown SiO_2 – high-k material. This stack structure was chosen for two reasons: Firstly, SiO_2 is known to have interface state densities with silicon by one order of magnitude lower than high-k materials [Wilk et al., 2001]. And secondly, it is difficult to avoid the formation of a SiO_2 interlayer during metal oxide deposition onto silicon: Oxygen is present, the reaction of oxygen with silicon to SiO_2 is thermodynamically favourable under most conditions [de Almeida and Bauvol, 2004] and film deposition operates at considerable temperatures. To achieve high-quality SiO_2 interlayers thermal oxidation was preferred.

Immediately before all oxidations, the samples were cleaned as follows: After immersion in Piranha solution (30 % (w/v) H_2O_2 : 96 % (v/v) H_2SO_4 = 2 : 1) and subsequent dipping in HF, a standard RCA clean [Kern and Puotinen, 1970] was performed, followed by a final HF dip to obtain SiO_2-free, hydrogen terminated silicon surfaces [Higashi and Chabal, 1993]. Three different oxidation processes were used for comparison: Dry furnace oxidation in pure O_2 atmosphere at 820 °C, wet furnace oxidation in an H_2O atmosphere at 600 °C and rapid thermal process oxidation in a mixed atmosphere of O_2 and N_2O (1:1) at 950 °C.

3.1.2 Pulsed laser deposited high-k dielectrics

All high-k dielectric thin films (Al_2O_3, yttria stabilised zirconia with a ZrO_2 : Y_2O_3 ratio of 9 : 1 (YSZ), $DyScO_3$, CeO_2, (La,Gd)ScO_3, $LaAlO_3$) presented in this thesis were produced via pulsed laser deposition (PLD). PLD was the method of choice, because it offers two important advantages over competing thin film deposition methods: Firstly, one deposition takes only 10 min. And secondly, the resulting PLD films preserve the stoichiometric composition of the target. The reason for this is the high energy transfer rate of the laser pulses, which greatly exceeds within nanoseconds the evaporating temperature of all elements contained by the target material. Hence the vapour composition is independent from the vapour pressure of the single target elements [Blank et al., 2004].

Figure 3.1 shows a schematic drawing of the applied on-axis PLD configuration. A KrF excimer laser of 248 nm wavelength is placed outside the vacuum chamber and focused through a window onto the surface of the target. The 25 ns laser pulses hit the surface with an energy density of approximately 5 J/cm^2 [Schöning et al., 2001]. The laser beam vapourises stoichiometrically the target surface and subsequently ionises the ablated species to form a plasma. Then the plasma expands into the vacuum chamber. In vacuum, the angular distribution of the plasma is determined by collisions of the ablated species

among themselves. Since the pressure gradient in the vapour near the target surface is largest perpendicular to the surface, the axis of the plasma is oriented along the target surface normal. In on-axis configuration, the substrate is situated perpendicular to the plasma axis (see figure 3.1). Upon arrival, plasma species sublimate on the substrate. A SiC heater controls the substrate temperature during deposition.

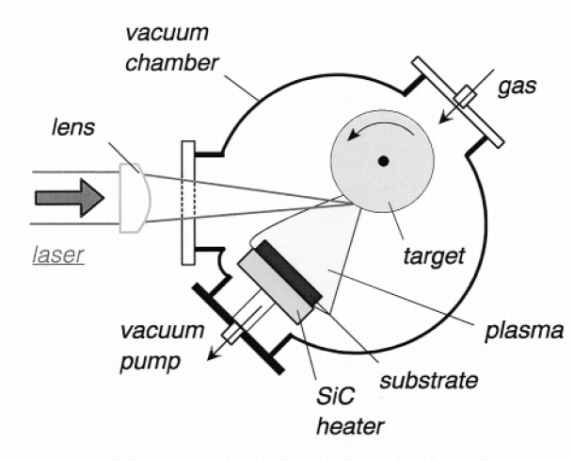


Figure 3.1: Schematic drawing of the PLD off-axis configuration. Source: [Schöning et al., 2001]

The properties of the resulting thin films strongly depend on the conditions during deposition. The most important ones are the vacuum background gas and pressure and the substrate temperature. A standard O_2 pressure of $2 \cdot 10^{-3}$ mbar was used for all materials. The substrates were normally heated to approximately 550 °C during Al_2O_3 and YSZ and 450 °C during $DyScO_3$ deposition.

Yttria stabilised zirconia (YSZ), which is ZrO_2 that is stabilised in its cubic crystal structure by addition of Y_2O_3, was originally chosen as dielectric, because it is the only known oxide, which has the potential to grow epitaxially on silicon. Epitaxial films have in general the advantage of exhibiting higher dielectric constants than amorphous films [Young et al., 2003]. Since the epitaxial growth strongly depends on the deposition conditions, the substrate temperature during YSZ deposition was scanned between 550 °C and 800°C for optimum epitaxial growth. In YSZ films, the required avoidance of an amorphous SiO_2 interlayer during epitaxial growth is most probably due to the dissociation of SiO_2 by Zr, because Zr is known to exhibit a higher affinity to O than Si [Ingebrandt, 1998].

3.1.3 Covalently bound organic monolayers

Two different procedures were used to prepare dielectric organic monolayers on silicon attached via covalent Si – C bonds: In the first method UV light (254 nm) was applied to deliver the activation energy, while the second method employed very mild preparation conditions by using visible light (447 nm). In both cases, the monolayers were formed

from cleaned, hydrogen terminated silicon surfaces (for details see [Faber et al., 2005]) and pure dodecene ($CH_3(CH_2)_9CH{=}CH_2$), a C_{12} alkane derivate with one double bond.

For the UV light method, the radical chain reaction depicted in figure 3.2a is proposed as underlying mechanism [Linford et al., 1995]. Due to the Si – H bond strength of 3.5 eV, a wavelength smaller than 350 nm is required to perform Si – H bond cleavage. Hence a different reaction mechanism is suggested for the visible light method, which is shown in figure 3.2b [Sun et al., 2005]: Upon excitation surface electrons are temporarily moved to the bulk and leave behind a delocalised radical cation at the surface. In Si – Si-containing radical cations the Si – Si bond is not very strong, allowing its cleavage and the attachment of the organic molecule. Transfer of one hydrogen atom to the organic molecule results in a Si radical at the surface. The monolayer formation continues with the radical chain mechanism of figure 3.2a.

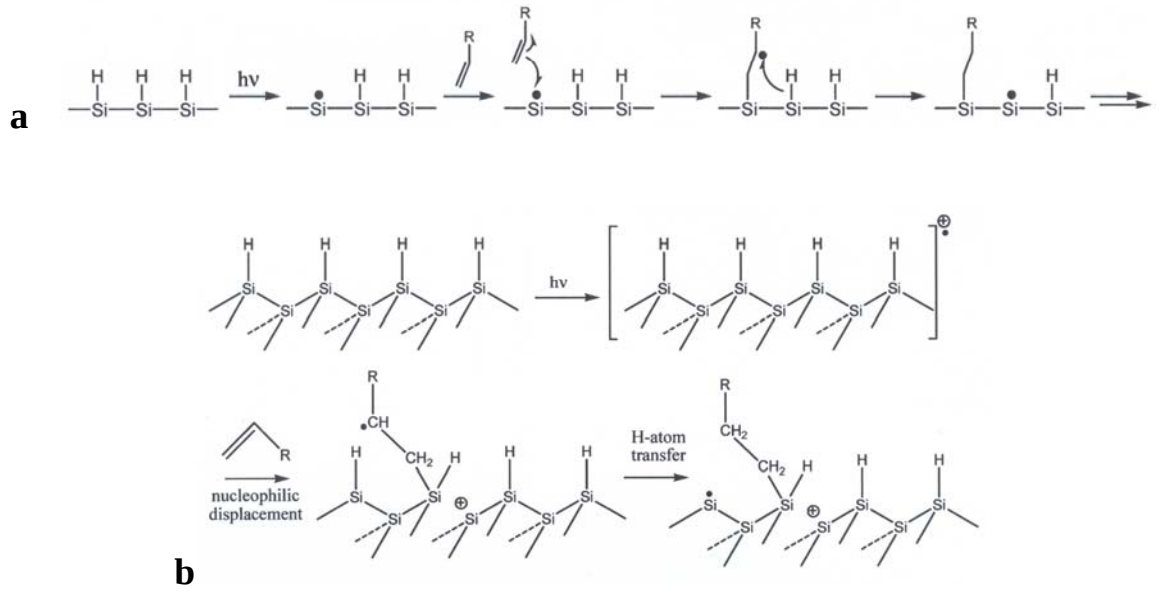


Figure 3.2a: Proposed radical chain mechanism for the formation of organic monolayers under UV light conditions. Adapted from [Sun et al., 2005].
b: Proposed mechanism for the formation of organic monolayers under visible light conditions. Source: [Sun et al., 2005]

3.2 Thin film analysis

3.2.1 Rutherford backscattering spectroscopy

The PLD deposition rate (film thickness per pulse) was determined from 100 – 150 nm thick test films before each PLD experiment with Rutherford backscattering spectroscopy (RBS) to compensate for uncontrollable parameters such as energy density variations in the laser ouput. Furthermore, the crystallinity of YSZ films on (100) silicon surfaces was checked.

The RBS method uses H^+ or He^+ ions (1.4 MeV He^+ ions were employed in the work of this thesis), which are directed onto the thin film to be examined. The penetration depth is on the order of 1 µm. Most ions are scattered in forward direction by the electrostatic potential of the atomic nuclei. Few ions, which hit nearly centrally an atomic nucleus, are scattered at high angles up to 180°. In RBS, the energy of these backscattered ions is measured.

The energy of the elastically backscattered ions depends on the mass of the scattering atom. Therefore, each element of the studied thin film has a characteristic maximum backscattering energy. Additionally, the ions suffer from energy loss on their way through the thin film to and from the scatter centre due to electronic excitations of the solid. This leads to broadening of the element-specific backscattering spectral line towards the lower energies. Combined with the characteristic energy loss rate, the spectral line width is used to determine the thin film thickness.

If the ions hit a single crystal normal to a lowly indexed Miller plane, the probability for scattering is highly reduced in comparison with an arbitrary direction. This effect is called channelling and a measure for the crystallinity of the probe [Hillebrecht and Kisker, 1992].

3.2.2 Ellipsometry

Although the deposition rate was determined by RBS before each PLD experiment, the resulting film thickness could deviate up to 10%. Therefore all PLD deposited thin films, which were employed for the electrochemical characterisation or deposited on transistor chips as gate dielectric, were checked for their thickness by ellipsometry. Initially the refractive indices of YSZ and $DyScO_3$ were determined because of the lack of literature values. Furthermore, ellipsometry was used to characterise the film thickness homogeneity of ultrathin thermally grown SiO_2 and high-k materials by surface scanning.

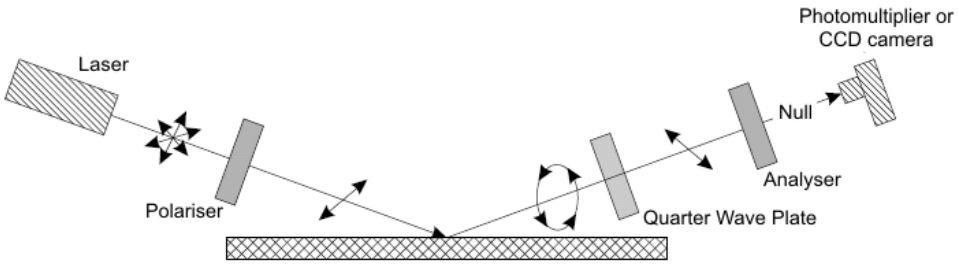


Figure 3.3: Schematic drawing of the light path in a nulling ellipsometer. The laser light passes three optical elements (two polarisers and one quarter wave plate) and is reflected at the surface. Each time the state of polarisation is changed as indicated by the arrows. Adapted from [Tompkins, 1993].

Two nulling ellipsometer instruments were used (EP3, Nanofilm; SE 400, Sentech, for some SiO_2 measurements). Figure 3.3 shows a schematic drawing of the light path in a nulling ellipsometer. Monochromatic light (532 nm in the EP3 and 632.8 nm in the SE 400) from the laser is linearly polarised by the polariser. Upon reflection on the interfaces of the thin film, the light is elliptically polarised. The quarter wave plate is used to make the light linearly polarised again. A second polariser (analyser) detects the plane of polarisation by searching for the angle at which the detector receives the least light intensity (nulling condition). The angular positions of polariser, quarter wave plate and analyser are used to calculate Δ and Ψ, the output values of ellipsometry.

Δ and Ψ are related to the Fresnel coefficient R^p for the electrical field component parallel to the plane of incidence and R^s for the perpendicular component as follows:

$$\frac{R^p}{R^s} = \tan\Psi \cdot e^{i\Delta} \tag{3.1}$$

Equation (3.1) gives the meaning of Δ and Ψ: $\tan\Psi = \frac{|R^p|}{|R^s|}$ is the ratio of the intensity changes upon reflection of the parallel and the perpendicular component. $\Delta = \delta_p - \delta_s$ is the difference in phase shift upon reflection between the parallel and the perpendicular component.

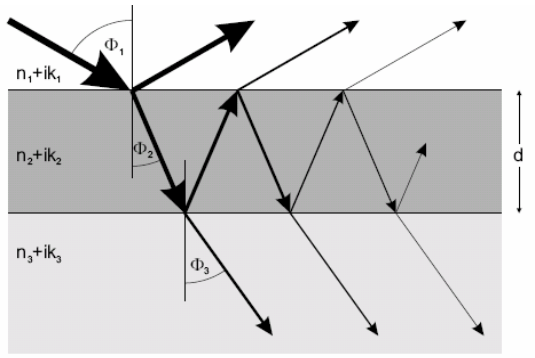


Figure 3.4: Schematic drawing of the reflection on a one-layer system. The complex refractive indices n_j+ik_j determine the Fresnel coefficients of the system. The information of the film thickness d is stored in the interference of the reflections on the two interfaces via the film phase thickness. Adapted from [Tompkins, 1993].

Figure 3.4 depicts the reflection on a one-layer system. The Fresnel coefficients of the system R^p and R^s depend on the the Fresnel coefficients $r_{12}^{p/s}$ and $r_{23}^{p/s}$ of the two interfaces between the media 1, 2 and 3 as follows:

$$R^p = \frac{r_{12}^p + r_{23}^p \exp(-i2\beta)}{1 + r_{12}^p\, r_{23}^p \exp(-i2\beta)} \qquad R^s = \frac{r_{12}^s + r_{23}^s \exp(-i2\beta)}{1 + r_{12}^s\, r_{23}^s \exp(-i2\beta)} \tag{3.2}$$

β is the film phase thickness and is a function of the film thickness d:

$$\beta = 2\pi\left(\frac{d}{\lambda}\right)(n_2 + ik_2)\cos\Phi_2, \tag{3.3}$$

where λ is the wave length of the laser, Φ_2 is the angle of the light inside the film with respective to the surface normal (see figure 3.4) and (n_2+ik_2) is the complex refractive

index of the film. Accordingly, the thickness of the film can be calculated from equation (3.1), if the refractive indices of the three involved media are known. Since equations (3.2) give an iterative rule of how to form the Fresnel coefficients for the system with one additional layer, also multilayers can be treated. Multi-angle measurements allow to determine a second unknown parameter by fitting, such as the refractive index of the thin film or a second film thickness in a multi-layer, because the Fresnel coefficients strongly depend on the angle of incidence [Tompkins, 1993].

3.2.3 Scanning electron microscopy

Thin films of high-k materials and of SiO_2 were characterised by scanning electron microscopy (SEM). Due to its unique resolution range from centimetres down to several nanometres, SEM allows to study both the macroscopic homogeneity and the microscopic features of surfaces.

In SEM, a focussed electron beam with an energy of 2 to 50 keV scans the surface inducing the emission of secondary electrons. A detector measures the secondary electron signal, which is imaged as a function of primary beam position. Since the electronic work function strongly depends on the surface geometry and on the elements contained therein, SEM resolves both the surface topography and variations in its composition. Moreover, secondary electrons are not only emitted from the surface but also from regions of up to 1 µm inside depending on the primary beam energy. Therefore also variations in the vertical composition of thin films, for instance thickness variations in films on top of flat substrates, can be imaged via SEM [Hillebrecht and Kisker, 1992].

Dielectric materials are being charged by the primary electron beam during SEM imaging. Charged surfaces result in image artefacts due to very high secondary electron emission. To prevent charging, insulators are often covered by a thin, sputtered and conducting film of materials such as gold or graphite. However, the thickness of all dielectric films studied in this thesis was sufficiently small (< 15 nm), that most primary electrons traversed into the silicon substrate keeping the charging to moderate levels. Therefore, sputtering of a conducting film was not necessary.

3.2.4 Atomic force microscopy

To complete the structural analysis, atomic force microscopy (AFM) measurements were performed on thin films of high-k materials and of SiO_2. Due to atomic resolution in vertical direction and a resolution of several nanometres in lateral direction, AFM is capable of statistical characterisation of the microscopic surface roughness.

AFM is based on the repulsive interaction between surface atoms and the ultimate atom of a tip. The tip is attached to a cantilever. In the applied AFM tapping mode, a piezo-electric crystal, which is driven near the resonance frequency of the cantilever,

causes the cantilever to oscillate. The oscillation amplitude is monitored via a laser beam that is deflected off the cantilever onto a photodiode. The interaction between surface atoms and the ultimate tip atom damps the amplitude. During surface scanning by the tip, the damping is kept constant by varying the distance between surface and tip using another piezo-electric crystal. The position of this crystal is imaged as a function of tip scanning position [Bonnell and Huey, 2001].

During AFM measurements, the interaction with the tip might harm the surface and lead to image artefacts. To exclude this error source, the scanning area was enlarged after each measurement to assure that there was no contrast between the cut-out of the last measurement and the surrounding.

3.2.5 Water contact angle measurements

Silanisation of O_2 plasma treated hydrophilic SiO_2 surfaces with amino group-terminated silanes to bind single-stranded DNA molecules via an additional crosslinker is routinely done in our group [Han et al., 2006a; Han et al. 2006b]. To determine whether the same routine, which is described in chapter 3.6, can be applied to the high-k oxides Al_2O_3, YSZ and $DyScO_3$, the water contact angle of the oxide surfaces before and after silanisation was measured.

Young´s equation gives the relation between the contact angle θ of a water drop with a surface (see figure 3.5) and the interfacial tensions γ_s of the solid – air interface, γ_w of the water – air interface and γ_{sw} of the solid – water interface:

$$\gamma_w \cdot \cos\theta = \gamma_s - \gamma_{sw} \tag{3.4}$$

If the solid – water interface is energetically more favourable than the bare solid ($\gamma_{sw} < \gamma_s$), the contact angle is smaller than 90° and the surface is called hydrophilic. If vice versa the interfacial tension of the solid – water interface is higher than that of the bare solid surface ($\gamma_{sw} > \gamma_s$), the contact angle exceeds 90° and the surface is called hydrophobic.

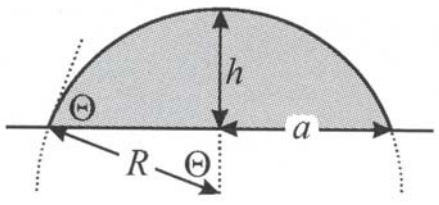


Figure 3.5: Schematic drawing of a small sessile water drop with contact angle θ, height h and contact radius a. Source: [Butt et al., 2003]

The sessile drop method was employed to determine the contact angles: A small water drop of 5 µl in volume was placed on the surface. The drop´s contour was recorded by a camera and fitted to a cicular cross-section as predicted for small drops by the Young-Laplace equation, which gives the general relation between interface curvature, interfacial tension and pressure difference between two adjoining phases. After defining the planar

surface in the recorded image to the software, the contact angle was calculated from the geometric relation $\tan\left(\frac{\theta}{2}\right)=\frac{h}{a}$, where h is the height and a the contact radius of the drop (see figure 3.5) [Butt et al., 2003.].

3.3 Electrical characterisation of thin dielectric films

3.3.1 Electrochemical I-V and C-V measurements on thin dielectric films

To study the suitability as gate material in ISFETs, the properties of ultrathin SiO_2 and high-k dielectric films were investigated electrochemically. Current-voltage (I-V) characteristics of the respective EOS diodes were recorded to determine the dielectric breakdown voltages indicated by an exponential rise in current density. Capacitance-voltage (C-V) curves on the same structures were used to extract several further quantities allowing to judge the quality of the dielectric film: The oxide capacitance, the dielectric constants of the PLD deposited high-k films and the hysteresis, which constitutes a qualitative measure for the trapping of charge carriers inside the dielectric. Shifts along the voltage axis were determined by the flat-band voltage, which was extracted from the intercept of the linear portion in the Mott-Schottky plot $[C_{ox}/C(V)]^{-2} - 1$ with the voltage-axis [Johnson and Worrell, 2005]. Furthermore, the curve shape constitutes a qualitative measure for the interface state density.

For both I-V and C-V measurements, a three-electrode set-up was employed. The introduction of an additional counter electrode had the advantage of keeping the reference electrode currentless during the measurements. Therefore, the reference potential of the electrolyte was precisely determined at all times. Figure 3.6 depicts the C-V set-up: The impedance of the EOS diode was determined by an impedance analyser (SI 1260, Solartron), which applied a small AC voltage and recorded the current answer from the system. The bias voltage sweep was performed by a potentiostat (PAR 283, Princeton Applied Research). The measurements were controlled and read out by the EOS measurement software ZPlot 2.0 (Scribner Associates, Inc.). For the I-V voltammetry measurements the DC current as a function of applied voltage was recorded by the potentiostat. The measurements were controlled and read out by the EOS measurement software CorrWare 2.0 (Scribner Associates, Inc.).

All EOS samples had the following structure: aluminium – p-silicon – high capacitance film. As substrate we used (10 x 10) mm^2 cut p (boron)-silicon wafer (4´´, Gritek Polished Wafers) pieces of (100) orientation with a resistivity of (7 – 21) Ω·cm. P-silicon was used as substrate for two reasons: Firstly to mimic the structure of p-channel FETs, into which the high capacitance films were intended to be implemented. And

secondly p-silicon offers the advantage of forming a very simple ohmic contact with aluminium. The aluminium backside contact was made via electron beam physical vapour deposition.

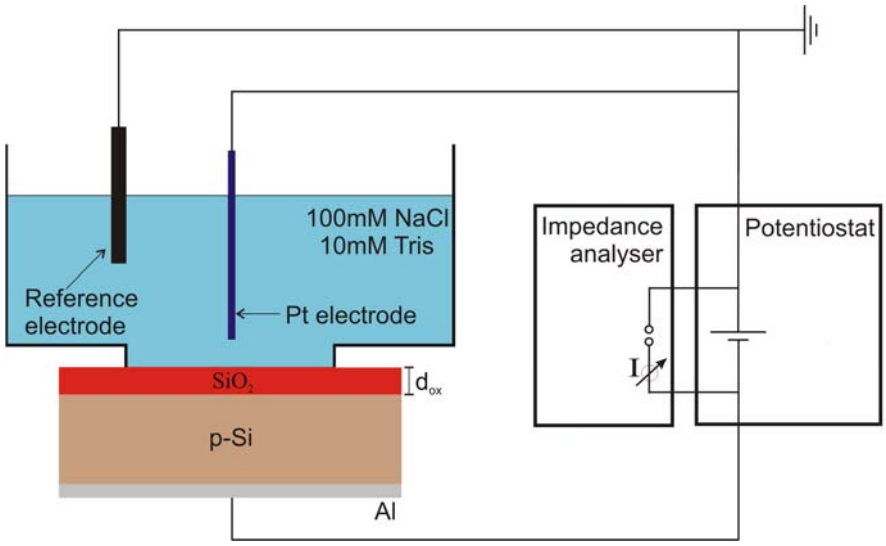


Figure 3.6: Schematic drawing of the electrochemical three-electrode set-up employed during the C-V curve measurements.

In all experiments the electrolyte was made of 100 mM NaCl and 10 mM TRIS (tris(hydroxymethyl)aminomethan) in deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm) providing low resistivity (~ 85 Ω·cm) on the order of physiological solutions and constant pH (~ 9.7). A commercial Ag/AgCl electrode (DRIREF-5SH, World Precision Instruments) served as reference electrode. A platinum (Pt) wire was used as counter electrode because Pt is known to be inert in electrochemical experiments. The electrochemical cell was made of teflon, which is also known to be an inert material. Finally, the employed o-ring was made of Kalrez (Dupont), a very inert elastomer. The o-ring defined the measurement area by its inner diameter of 6 mm.

During the measurement of I-V characteristics, each data point was averaged over 10 s. The voltage was always applied towards accumulation of the p-silicon surface to mimic the dielectric breakdown in p-channel transistors.

The standard AC amplitude and frequency in C-V curve measurements were 10 mV and 1000 Hz, respectively. 1000 Hz were chosen for several reasons: Firstly, this is the order of magnitude as exhibited by electrophysiological signals. Therefore the capacitance recorded at 1000 Hz constitutes the relevant input capacitance during cell-transistor coupling for a respective gate dielectric. Secondly, since the characteristic time of minority carrier generation in silicon is on the order of milliseconds [Muller and Kamins, 2002], the charging and discharging of interface states at the silicon – dielectric interface can follow the 1000 Hz stimulation to a certain degree. Hence, the interface state density can be

evaluated qualitatively by the presence and height of a hump in the C-V curve at the bottom of its shoulder, when the silicon surface energy is within the band gap. And thirdly, the frequency is sufficiently low to keep the influence of the electrolyte resistance R in series with the oxide capacitance C_{ox} minor: In accumulation the employed set-up has a cut-off frequency $\omega = 1/(R \cdot C_{ox})$ on the order of $1/(100\ \Omega \cdot 0.4\ \mu F) = 25$ kHz.

In the analysis the model of a resistor and a capacitor in parallel was used to calculate the capacitance of the EOS system from the measured impedance, because series resistances were negligible in comparison with the oxide resistance. For this model, the circuit impedance Z is given by

$$Z = Z' + iZ'' = \left[\frac{1}{R_p} + i\omega C_p \right]^{-1} \tag{3.5}$$

where Z′ and Z′′ are the real and imaginary parts of the complex impedance, resistance R_p and capacitance C_p are the parallel model parameters and ω is the angular frequency of the stimulation. Solving for C_p in terms of the measured impedance yields the EOS system capacitance as

$$C_p = \frac{-Z''}{\omega(Z'^2 + Z''^2)}. \tag{3.6}$$

Throughout this thesis the term electrochemically active oxide thickness d_{ox} is defined as the film thickness, which corresponds to the measured oxide capacitance C_{ox}. It is generally calculated by the plate capacitor formula

$$d = \varepsilon_0 \varepsilon_{ox} \frac{A}{C_{ox}} \tag{3.7}$$

where C_{ox} is the experimental capacitance measured in accumulation, ε_0 the permittivity of vacuum, ε_{ox} is the respective oxide dielectric constant and A is the area of the capacitor.

In the analysis of the high-k dielectric films, the measured capacitances C_{stack} of SiO_2 – high-k material film stacks were used to determine the dielectric constant of the high-k materials and the thickness of the SiO_2 interlayer as follows: First the equivalent oxide thickness d_{EOT} of the film stacks, which is defined as the thickness of an SiO_2 film with the same capacitance as the stack capacitance C_{stack}, was calculated by the following modified plate capacitor formula, which uses the dielectric constant of SiO_2 ($\varepsilon_{SiO_2} = 3.9$):

$$d_{EOT} = \varepsilon_0 \varepsilon_{SiO_2} \frac{A}{C_{stack}} \tag{3.8}$$

Since C_{stack} is the series capacitance of the SiO_2 interlayer capacitance C_{SiO_2} and the high-k film capacitance $C_{high\text{-}k}$, it can be written as

$$C_{stack} = \left[\frac{1}{C_{SiO_2}} + \frac{1}{C_{high-k}} \right]^{-1} \tag{3.9}$$

Inserting equation (3.9) into (3.8) and replacing C_{SiO_2} and $C_{high\text{-}k}$ by their respective plate capacitor formulas according to equation (3.7) yields

$$d_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} d_{high-k} + d_{SiO_2} \tag{3.10}$$

where $\varepsilon_{high\text{-}k}$ is the dielectric constant of the respective high-k material and d_{SiO_2} is the thickness of the SiO_2 interlayer.

Equation (3.10) constitutes the linear dependence of the stack d_{EOT} values on the high-k material thickness $d_{high\text{-}k}$. Therefore the slope in a plot of d_{EOT} as a function of $d_{high\text{-}k}$ gives the ratio between the dielectric constants of SiO_2 and the high-k material, and the intercept with the y-axis gives the thickness of the SiO_2 interlayer d_{SiO_2}. Accordingly the $\varepsilon_{high\text{-}k}$ and d_{SiO_2} values of the SiO_2 – high-k material film stacks were extracted from linear fits on the d_{EOT} values of SiO_2 – high-k material film stacks with varying high-k material film thickness but identical SiO_2 interlayers. The required $d_{high\text{-}k}$ values were measured by ellipsometry.

3.3.2 Determination of the interface state density in MOS structures

The magnitude of the interface state density (trap density) at the silicon – oxide interface is crucial for the evaluation of the suitability of dielectric films as FET gate oxides, because it determines the 1/f noise in FETs (see chapter 2.2.2). As described in chapter 2.1.3, the comparison of high and low frequency C-V curves allows to extract the interface state density D_{it} quantitatively. The D_{it} measurements were performed on MOS structures, because the cut-off frequency in electrochemical EOS set-ups is generally lower than the typical stimulation (100 kHz and above) during high frequency C-V measurements. This low cut-off frequency in EOS systems originates from the higher electrolyte series resistance and the difficulty to contact small capacitances with correspondingly small contact areas.

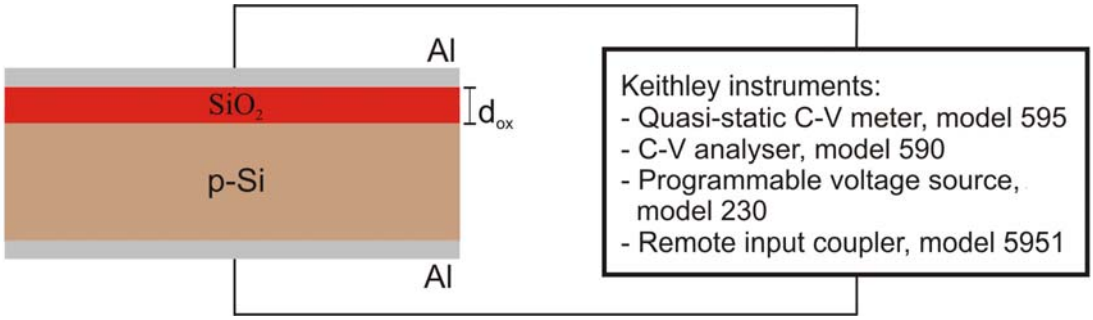


Figure 3.7: Schematic drawing of the applied electronic set-up employed during the determination of the interface state density.

Figure 3.7 depicts a schematic drawing of the employed electronic set-up: The voltage step quasi-static method (quasi-static C-V meter model 595, Keithley) was applied

for the low frequency measurement, where the capacitance is determined by direct recording of the MOS capacitor charging after single bias voltage steps. For the high frequency measurements performed at 100 Hz or 1 MHz, a C-V analyser (model 590, Keithley) was employed. Two further instruments (programmable voltage source model 230, Keithley; remote input coupler model 5951, Keithley) drove the quasi-static C-V meter and the C-V analyser at the same time allowing to perform both measurements simultaneously. This has the advantage, that in both curves the data points of the same bias voltage correspond to identical thermodynamic conditions at the silicon – oxide interface.

The determination of the interface state density from high and low frequency C-V measurements is limited by the oxide thickness: In SiO_2 diodes with oxide thicknesses below 4 nm, quasi-static C-V measurements normally cannot be recorded, because the capacitive current signal due to the stimulation is covered by the leakage currents through the dielectric [Agilent Technologies, 2001]. Therefore the interface state density was determined on 8 to 9 nm thick SiO_2 films.

The SiO_2 films for the MOS diodes were prepared in the same way as the films for the electrochemical characterisation, except for a prolonged oxidation time and in the case of the Si-O-N a higher oxidation temperature to achieve higher thicknesses. Subsequently, aluminium was deposited via electron beam physical vapour deposition onto both wafer sides: Onto the front side during a photolithographic lift-off process (resist AZ 5214, MicroChemicals) to structure squared contact pads ranging from 64 to 200 µm in length; onto the back side after an HF dip to form an ohmic silicon – metal contact. A semiconductor probe station (PM 5, Süss) was used to contact the pads directly and the chip back side via the aluminium probe holder. The measurements were controlled, read out and analysed for the interface state density D_{it} by a measurement software (Metrics-ICS, Keithley) as described in chapter 2.1.3.

3.4 Fabrication and operation of high-k dielectric ISFETs

3.4.1 The planar technology process

The high-k dielectric p-channel ISFETs, which were used in the work of this thesis, were fabricated by planar technology in the clean room (class 100) of the Institute of Bio- and Nanosystems at the Research Centre Jülich. The micrograph of figure 3.8 shows the 4 x 4 array of ISFETs, which was built into each chip: The area of the source contact, which is common to all 16 transistors is indicated by the corresponding text label. The 16 gate areas with a pitch of 200 µm are clearly visible. The drain contacts are the areas, which lead to the gates from the side opposite to the source, i.e. from the top for the upper 8 ISFETs and from the bottom for the lower 8 ones. In the following the process flow

containing 6 photolithographic steps is outlined. It is based on the process described by [Offenhäusser et al., 1997].

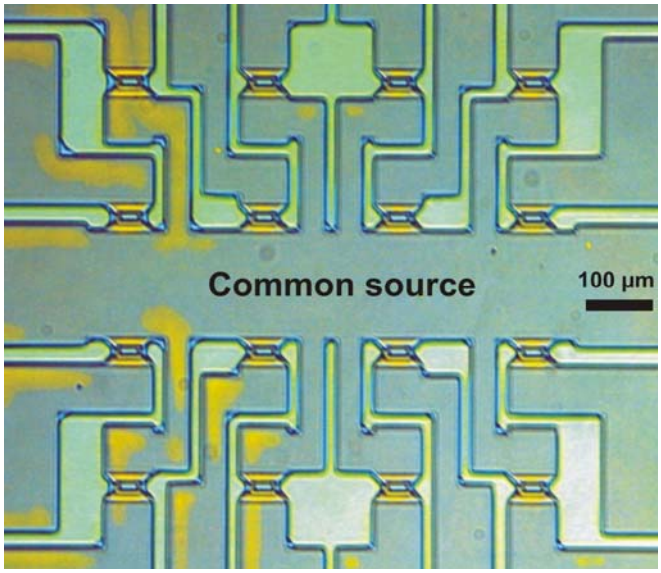


Figure 3.8: Micrograph of the 4 x 4 array of ISFETs with a 3 nm SiO_2 interlayer and a 15 nm $DyScO_3$ film as gate dielectric. The gate width is 25 µm and the pitch of the array is 200 µm. The corresponding text label indictates the source contact common to all 16 ISFETs. The separation regions between the source and drain feed lines are clearly visible.

The p-channel ISFETs were built into n (phosphorus)-silicon wafers (4´´, Wacker) of (100) orientation with a resistivity of (8 – 12) Ω·cm. The gates were 12, 25, 50 and 100 µm in width. Each chip of (5 x 5) mm^2 in dimension contained a 4 x 4 array of equally wide gates. The pitch of the arrays was 200 µm except for the chips with 100 µm wide gates, which had a pitch of 500 µm.

In the first photolithographic step and the following diffusion process, the source and drain feed lines were defined by a strong boron implantation ($8 \cdot 10^{15}$ cm^{-2}, 120 keV). In the second photolithographic step, a lighter boron implantation ($5 \cdot 10^{15}$ cm^{-2}, 80 keV) was performed to define the dimension of the pnp-structure and particularly the gate length. The initial separation of the implanted source and drain regions was 5 µm. During the subsequent diffusion process at 1000 °C for 60 minutes, the drain-source separation was decreased to a final effective gate length of approximately 2 µm.

In the third photolithographic step, the approximately 1 µm thick field oxide, which was grown during the diffusion processes, was etched away in slightly larger areas than the prospective gate regions, which however contained the gate regions. Then a so-called ONO-stack consisting of 50 nm thermal SiO_2, 130 nm low pressure chemical vapour deposition Si_3N_4, and 100 nm plasma-enhanced chemical vapour deposition SiO_2 was deposited. The ONO-stack has the following advantages: Si_3N_4 is denser than SiO_2 and therefore a better protection against penetration of electrolyte ions. However, Si_3N_4 does not adhere very well to silicon. Since it adheres strongly to SiO_2, however, the SiO_2 interlayer was produced before the Si_3N_4 layer. The top SiO_2 layer was deposited, because SiO_2 and more general glass has been established as widely used substrate in cell physiological experiments throughout the scientific community.

In the fourth photolithographic step, the ONO-stack was etched away in the gate area. Figure 3.9a shows the micrograph of a 25 µm wide gate at this process stage. Immediately after a standard RCA cleaning process with a final HF dip, the SiO_2 gate interlayer of approximately 3 nm thickness was oxidised in a furnace at 820 °C for 2 min in pure O_2 atmosphere. Then the respective high-k dielectric was deposited by PLD. The thickness of the SiO_2 interlayer and the high-k dielectric film was always determined by measurements with an imaging ellipsometer (EP3, nanofilm) in the wafer regions between the chips, where all process steps occurring in the gate area were performed as well.

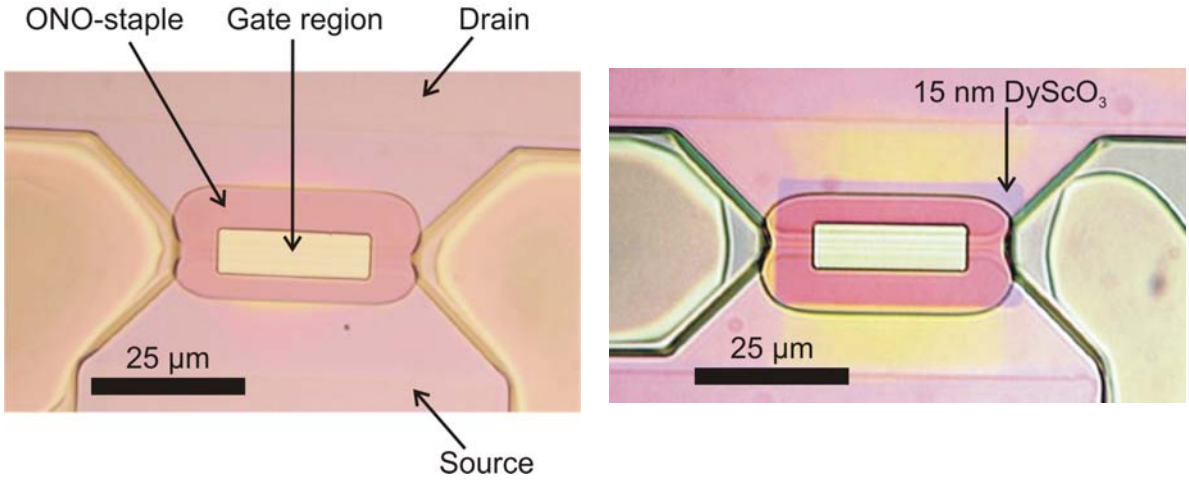


Figure 3.9a: Micrograph of the gate region of an ISFET with a 25 µm wide gate before the fabrication of the gate dielectric. The arrows indicate the gate region, the ONO-stack surrounding the gate, the source and the drain feed lines. The structures diverging to the left and to the right from the gate are the separation regions between the source and drain feed lines.
b: Micrograph of the gate region of an ISFET with a 25 µm wide gate, which has a 3 nm SiO_2 interlayer and a 15 nm $DyScO_3$ film as gate dielectric. The arrow indicates the region (40 x 20 μm^2) , where the $DyScO_3$ film is left after the ion beam etching.

In the fifth photolithographic step, the high-k material was etched away in all regions except for the gate areas by Ar^+ ion beam etching. Figure 3.9b shows the micrograph of a 15 nm $DyScO_3$ film after etching, which is only left on the gate area. The underlying reason was to leave the chip surface as SiO_2, which has been established as substrate in our cell culture for many years. In the sixth photolithographic step, the 16 drain contacts and the 2 contacts of the common source were metallised (200 nm aluminium for an ohmic contact with p-silicon, 200 nm gold as excellent material for both wire and flip-chip bonding) in a lift-off process by electron beam physical vapour deposition (PVD).

To study the impact of the high input (gate) capacitance of the high-k dielectric ISFETs on their performance, also so-called standard SiO_2 ISFETs were used in the work of this thesis. The standard SiO_2 ISFETs were processed in the same way as the high-k

ISFETs except for the gate oxide, which was produced by thermal oxidation in a furnace at 820 °C for 60 min in pure O_2 atmosphere. The resulting SiO_2 thickness was approximately 9 nm.

3.4.2 Chip encapsulation

Depending on the application, the ISFET chips were encapsulated in two different ways. The image of figure 3.10a depicts a chip encapsulated for cell-transistor coupling as follows [Offenhäusser et al., 1997]: First the chip was fixed onto a 28-pin dual in line (DIL) chip carrier (Spectrum Semiconductor Materials) with a flip-chip glue (Epo Tek H20E-PFC, Epoxy Technology). Subsequently, the chip was wire-bonded. Then a funnel of polydimethylsiloxane (Sylgard 182, Dow Corning), which was formed from a custom-made metal template, was attached by using a silicon glue (Sylgard 96-083, Dow Corning) onto the chip centre keeping the ISFET array uncovered (see figure 3.10a). The inner diameter of the funnel was 2.8 mm. Finally a glass ring with an inner diameter of 1.35 cm was glued onto the carrier and the space between funnel and glass ring was filled with the silicon glue. The resulting structure served as a Petri dish with an approximate volume of 400 µl, which allows for culturing of cells on top of the ISFET array.

The image of figure 3.10b depicts a chip encapsulated for biomolecule detection as follows: Again the above mentioned flip-chip glue (Epo Tek H20E-PFC, Epoxy Technology) was used to fix the chip onto the self-made carrier by the flip-chip technique. Subsequently, an underfill glue (Epo Tek U 300, Polytec) was applied to seal the remaining clefts between chip and carrier completely. The planar surface of the carrier allowed to seal a flow-through cell, which was mounted onto the chip for fast electrolyte exchanges, by means of an o-ring.

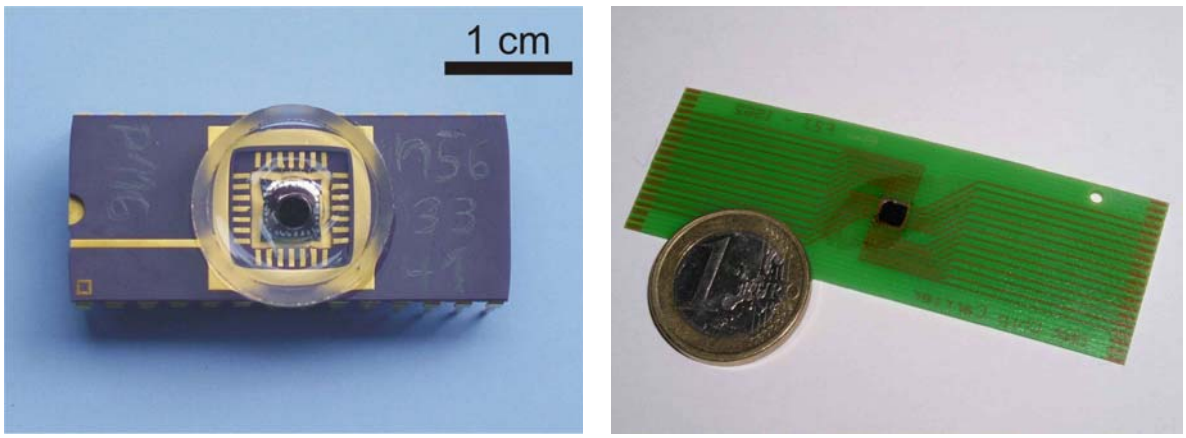


Figure 3.10a: Image of a chip encapsulated for cell-transistor coupling experiments. The uncovered, dark area in the chip centre contains the 4 x 4 ISFET array.
b: Image of a chip encapsulated for ion sensitivitiy and biomolecule detection experiments. The uncovered, dark area in the chip centre contains the 4 x 4 ISFET array.

3.4.3 The electronic amplifier system

Two custom-made electronic amplification systems were used in the work of this thesis depending on the chip encapsulation. The underlying electronic circuit, however, was very similar in both systems. The general circuit, which was developed by [Offenhäusser et al., 1997], [Sprössler et al., 1998], [Krause, 2000] and [Ingebrandt, 2001], is depicted in figure 3.11 and described in the following.

The dashed line in figure 3.11 constitutes the separation between the pre-amplifier and the main amplifier stage. The pre-amplifier consists of 16 current-to-voltage converters, which convert simultaneously all 16 drain-source currents of the ISFET array into voltages. During the measurement of ISFET characteristics, the pre-amplifier outputs were directly transferred to a personal computer (PC) for recording.

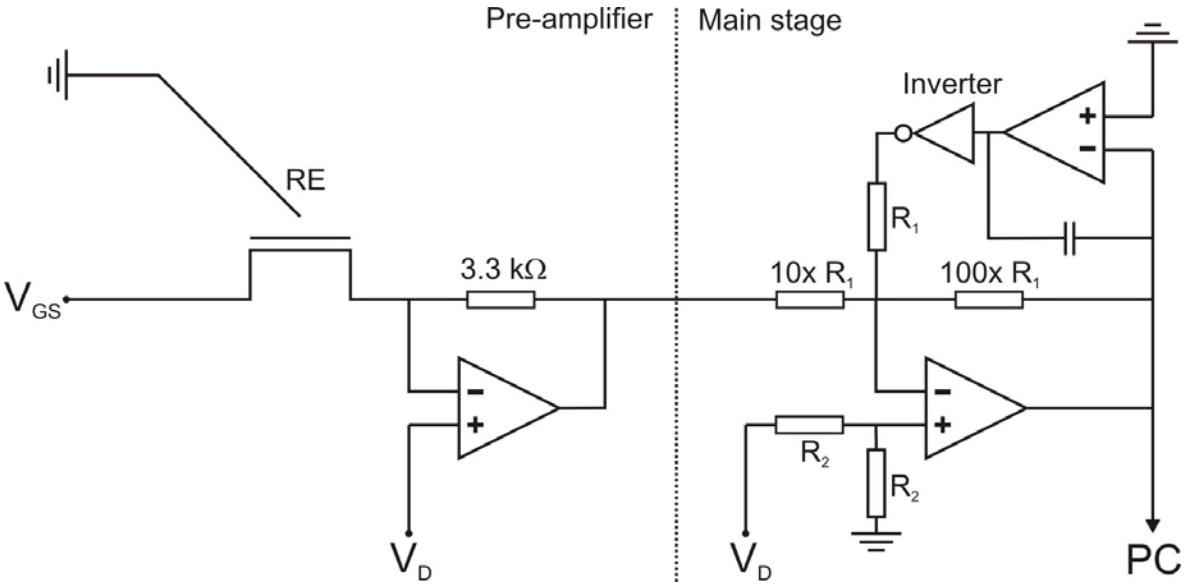


Figure 3.11: Electronic circuit of the amplifier system. The dashed line constitutes the separation between the pre-amplifier and the main amplifier stage. RE indicates the reference electrode, which is immersed into the electrolyte contacting the ISFET gates. The arrow down to the right indicates the amplifier output, which is transferred to the recording PC.

In all sensitive experiments, i.e. cell-transistor coupling, biomolecule detection, ion sensitivity and noise measurements, the main stage was added to the circuit for two reasons: At the beginning of a measurement, it compensated all 16 pre-amplifier outputs to zero by applying the respective compensation voltages to the individual channels. Subsequently, during the measurement, the main stage amplified the compensated signals to gain higher signal resolution. The main amplifier outputs were then recorded by an analogue-to-digital converter (ADC) card (PCI-6071E, National Instruments Corp.), which was mounted inside of the PC. All experiments involving the main amplification stage were performed in the constant voltage mode: The drain-source current signal was

recorded, while constant drain-source and gate-source voltages were applied defining the so-called working point.

The main amplifier had a fixed amplification of 100 in the cell-transistor coupling system, while in the biomolecule detection system it could be tuned to amplifications of 1, 10, 30 and 100. In the cell-transistor coupling system, the ISFET drift was compensated by a feed-back loop with a characteristic time on the order of 10 seconds. No drift compensation was incorporated into the biomolecule detection system because of the expected slow signals in the respective experiments. A heating unit allowed to control the chip temperature via a metal plate, onto which the chip carriers were mounted in both the cell-transistor coupling system and the biomolecule detection system.

As seen in the images of figure 3.12a and b, pre-amplifier and main amplifier were in the cell-transistor coupling set-up physically separated into a head stage and the main amplification stage, while in the biomolecule detection set-up both stages were combined into one unit. During the experiments with both systems, the chips were covered by a metal cap serving as Faraday cage. The electrolyte was always contacted via an Ag/AgCl reference electrode, which was set to ground potential to avoid electrochemical reactions.

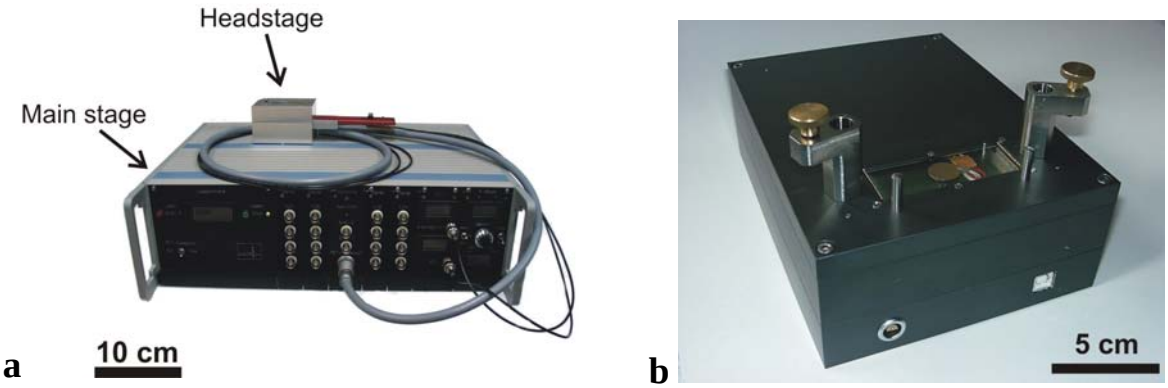


Figure 3.12a: Image of the cell-transistor coupling amplification system with the physical separation of head- and main stage.
b: Image of the biomolecule detection system.

During experiments with the cell-transistor coupling set-up, the gate-source and drain-source voltages were controlled by a custom-made software according to [Sprössler, 1997]. This software also recorded all ISFET characteristics and noise data. During cell-transistor coupling with the spontaneously active cardiomyocyte cell line HL-1, the data of all 16 ISFETs (channels) was recorded simultaneously by the commercial software MED 64 conductor 3.1 (Alpha MED Sciences) with a sampling rate of 10 kHz for each channel. During cell-transistor coupling with the HEK 293 cell line, the data of the recording channel was acquired via the external input of an EPC-9 patch-clamp amplifier (HEKA Elektronik) by the commercial software TIDA (HEKA Elektronik) with a sampling rate of 20 kHz (for details see chapter 3.7.3). In the bioelectronic detection

set-up, all measurements were controlled and read out by another custom-made software [Han et al., 2006b], which had a sampling rate of 1 Hz.

3.5 Characterisation of high-k dielectric ISFFETs

3.5.1 Electrical characteristics

The electrical characteristics of the high-k dielectric ISFETs were recorded to study their influence on the transistor performance in comparison with each other and in comparison with the standard SiO_2 ISFETs of lower input capacitance. Of particular interest was the influence of the gate capacitance on the maximum transconductance at a given drain-source voltage: Under the assumption of equal noise levels in ISFETs with an SiO_2 – high-k material stack and with standard SiO_2 as gate dielectric, higher transconductance values for the high-k material ISFETs correspond to a likewise higher signal-to-noise ratio. Moreover, the identical processing of ISFETs of four different gate lengths (12, 25, 50 and 100 µm) allowed to study also the influence of the gate length on the maximum transconductance. All characteristics recorded to study the influence of the gate capacitance were measured with deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm) as electrolyte. In all cases, a chlorinated silver wire was used as reference electrode.

By default, transfer characteristics were also recorded before all experiments involving ISFETs in order to choose the working point for the respective measurement. Under the assumption of noise being independent from the gate-source voltage, a maximum transconductance corresponds to the working point of highest signal-to-noise ratio and highest sensitivity, respectively. Therefore always a maximum in transconductance was chosen as working point. Upon all experiments, the transconductance value of the employed working point was saved in order to calculate the measured drain-source current signals into the corresponding gate-source voltages during analysis.

3.5.2 Noise power density

The noise levels of the high-k dielectric ISFETs, the standard SiO_2 ISFETs and the ISFETs of gate widths varying between 12 and 100 µm were determined to study the influence of the gate capacitance and of the gate dimension on the signal-to-noise ratio as follows: First the source-drain current noise of the respective ISFET was measured in a transconductance maximum, which represents a typical working point during the bioelectronic experiments performed in the work of this thesis. Subsequently, the recorded noise was divided by the transconductance of the measurement working point to transfer the recorded data into the

equivalent gate-source voltage signal at the input. The resulting noise level in the gate-source voltage gives the minimum signal height required to be detected by the respective ISFET.

Moreover, the spectral noise power densities were calculated from the gate-source voltage noise for two reasons: Firstly, the resulting spectrum gives the noise power density at 1000 Hz, which is the relevant noise level in cell-transistor coupling experiments, because electrophysiological cell signals have characteristic frequencies on the order of kHz. Secondly, the shape of the noise power density spectrum allows to characterise the noise source by comparison with the literature.

All source-drain current noise data was recorded in a dark Faraday cage to exclude extrinsic noise sources such as photonic electron-hole generation and perturbations from electromagnetic fields. Deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm) was used as electrolyte. The sampling frequency f_s was 10 kHz and the noise measurement time was 60 seconds.

The noise power density spectra S (f) in the gate-source voltage regime V_{GS} were calculated by means of the mathematical software matlab 6.5 (The MathWorks Inc.) using Carson´s theorem [Müller, 1990]:

$$S(f) = 2\, f_s \left| F(f) \right|^2, \tag{3.11}$$

where f_s is the sampling frequency of the noise measurement and F (f) is the Fourier transform of the noise data, which in the work of this thesis is given by the Fourier transform of V_{GS}:

$$F(f) = \int_{-\infty}^{\infty} V_{GS}(t)\, exp(-i2\pi ft)\, dt \tag{3.11}$$

Finally the spectra were normalised by dividing S by the recording time of the respective noise measurement to allow their comparison.

3.5.3 Ion sensitivity measurements

The pK and pNa sensitivities of the Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs were determined to study the sensitivity of the respective ISFET to the signal component in cell-transistor coupling, which originates from changes in the surface potential. The measurement solutions had the pK and pNa values of 4, 3, 2, 1 and 0. The covered range from 4 to 0 contains the physiological K^+ and Na^+ concentrations, which lie in the range between 5 and 155 mM (for details see chapter 2.3.2).

All measurement solutions had an ionic strength of 2 M in order to keep the ion activities constant and to avoid large conductivity differences. Each solution was based on deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm) and contained KCl and NaCl, respectively, according to its intended pK and pNa value. $CaCl_2$ was respectively added to such an amount, that the resulting solution was of 2 M ionic strength. To keep the

pH constant, all solutions contained the buffer HEPES in a concentration of 10 mM. Finally the solutions were adjusted to a physiological pH of 7 by addition of TRIS.

The measurements were carried out with a flow-through cell of polymethylmethacrylate (PMMA), which was mounted onto the respective ISFET. Its small volume of approximately 500 µl allowed to perform complete electrolyte exchanges within less than two seconds, while continuously recording the surface oxide potential with the respective ISFET. The pressure required for the solution exchange was exerted via a sringe. During the experiments, the ISFET and the flow-through cell were covered by a metal cap, which served as a Faraday cage providing protection from both electrostatic and photonic disturbances. As reference electrode, a self-made Ag/AgCl liquid junction electrode was used. It consisted of a small tube of plastic, which was filled with a chlorinated silver wire from the one side and with a gel serving as salt bridge from the other side. The gel was composed of 3 M KCl, which was gelificated by addition of 1 % (w/v) of agar.

The surface potential of oxides is generally most sensitive to the electrolyte pH. Although the pH is kept constant during all bioelectronic experiments, for completeness also the pH sensitivities of the Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs were measured. The experiments were carried out in the same way as the pK and pNa experiments. The pH measurement solutions had the values of 5, 6, 7, 8 and 9. The covered range contains the physiological pH value of approximately 7. The following composition of the solutions was chosen to mimic the extracellular cell medium used for the HEK 293 cell line: 5 mM KCl, 5 mM $MgCl_2$, 140 mM NaCl and 5 mM glucose. As buffer, the solutions of pH 5, 6 and 7 further contained 10 mM HEPES, while the solutions of pH 8 and 9 contained 10 mM TRIS. For the pH adjustment, HCl was used for the solutions of pH 5, 8 and 9 and NaOH for the solutions of pH 6 and 7.

3.5.4 Drift measurements

The long-term drift of Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs was measured because drift is the dominating noise source in biomolecule detection experiments. Also during these experiments, the set-up was covered by a metal cap, which served as Faraday cage providing protection from electrostatic and photonic disturbances. The self-made Ag/AgCl electrode described in chapter 3.5.3 was used as reference electrode. The employed electrolyte was deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm).

3.6 Charged biomolecule detection

First the procedures are described, which were applied to both the polyelectrolyte and the DNA detection experiments [Han, 2006c]. Before the actual experiments, the ISFET chip surfaces were cleaned as follows: After filling the chips with ethanol and rubbing their surfaces with cotton buds, the chips were exposed to ultrasound for 10 minutes in deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm). Finally, the chips were exposed to an O_2 plasma (plasma system 100-E, Technics Plasma GmbH) of 200 W for 2 minutes.

During the biomolecule detection experiments, a reproducible, well-defined and uniform supramolecular architecture of the gate surface is crucial in order to minimise the long-term drift, i.e. the main noise source. Hence, after the cleaning procedure, the gate oxide (standard SiO_2 or high-k dielectric) was silanised with 3-aminopropyltriethoxysilane (APTES), which results in an amino-terminated gate surface (see the schematic drawing of the silanisation reaction in figure 3.13).

In practise, the silanisation was performed as follows: The chips were placed in a desiccator containing a few drops of APTES. After sealing the desiccator and heating above 100 °C, the silane vapour reacted with the gate oxide (gas-phase silanisation) for one to two hours under a low pressure of approximately 1 mbar [Han et al., 2006b]. The achieved silane films had thicknesses of 2 ± 0.2 nm, which corresponds to several multilayers, because the distance between the Si atom and a proton of the amino-group in a fully extended NH_2 – silane molecule is equal to 0.7 nm [Han et al., 2006b].

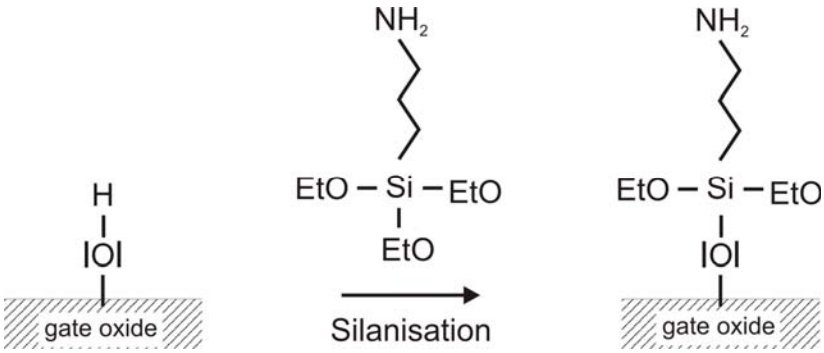


Figure 3.13: Schematic drawing of the gas-phase silanisation reaction between the gate oxide surface and APTES, which results in an amino-terminated surface.

During all biomolecule detection experiments, the solution exchanges were performed with the PMMA flow-through cell described in chapter 3.5.3. The entire electronic set-up was always covered by a metal cap, which served as Faraday cage providing protection from electrostatic and photonic disturbances. The self-made Ag/AgCl electrode described in chapter 3.5.3 was used as reference electrode.

3.6.1 Polyeletrolyte detection

For the layer-by-layer adsorption of oppositely charged polyelectrolytes, the amino-silanised gate oxide was alternately exposed to polystyrenesulfonate (PSS) and polyallyamine hydrochloride (PAH) solution. PSS is charged negatively, PAH positively, and their alternating layers contain similar charge densities [Riegler and Essler, 2002]. The PSS/PAH polyeletrolyte system was chosen for two reasons: Firstly, its layer-by-layer built-up is a well-described, straight-forward protocol [Decher and Hong, 1991; Decher et al., 1992]. And secondly, PSS and PAH possess considerably higher charge densities than DNA, wherefore the PSS/PAH system constitutes an excellent DNA model.

The actual polyelectrolyte detection experiments were based on the protocol developed by [Uslu et al., 2004]: A buffer solution, which contained 10 mM TRIS, 1 mM ethylenediaminetetraacetic acid (EDTA) and NaOH for the adjustment to pH 7, was applied until the long-term drift of the ISFETs had saturated. Since the terminating amino-group of the silane layer is basic, the net surface charge at pH 7 is initially positive. Therefore, the buffer solution was first exchanged for the PSS solution, which consisted of 50 µM PSS (molecular weight (MW) of 60 to 80 kDalton) dissolved in buffer solution. In order to saturate the PSS surface adsorption, the PSS solution was exchanged after 6 minutes for fresh PSS solution, which was again applied for 6 minutes like all following solutions. Then twice buffer solution was applied to flush away all excess PSS molecules and to obtain a constant ISFET signal. The first cycle of polyelectrolyte adsorption was completed by applying twice the PAH solution, which consisted of 50 µM PAH (MW of 60 to 80 kDalton) dissolved in buffer solution. Further layer-by-layer adsorption was achieved by cycle repetitions starting with applying twice the buffer solution.

3.6.2 DNA detection

As described in chapter 2.2.4 and 2.3.1, the ISFET signal from DNA hybridisation on the gate surface is very small and easily covered by drift noise. Therefore, a differential measurement technique, which allows to reduce the noise greatly, was used in the DNA detection experiments: Two types of probe ssDNA were immobilised onto the gates of each chip, each type on half of the 16 gates. The sequence of the employed target ssDNA was complementary to the sequence of the first probe DNA (perfect match (PM)), but fully non-complementary to the second (fully mismatch (FMM)). Hence, a DNA hybridisation signal could only occur in the recordings from ISFETs, whose gates were immobilised with PM probe DNA. However, the drift signals of ISFETs from one chip were highly correlated. The reason for this was, that the gates of the employed ISFET chips were closely spaced (array pitch of 100 or 200 µm), which caused the gate surface potentials, whose changes evoke the long-term drift, to differ hardly. Therefore, by subtracting the signal of a reference ISFET, whose gate was immobilised with FMM probe DNA, from the signal of an ISFET with PM probe DNA immobilised on its gate, the correlated noise,

which is by far larger than the independent noise, was eliminated from the recordings. The effort of immobilising FMM probe DNA onto the reference ISFETs was made to ensure (except for the hybridisation) equal surface chemistry on all gates and consequently equal drift behaviour in all ISFET signals.

In practise, the probe DNA immobilisation was performed as follows: After the above described amino-silanisation, the oxide surfaces were chemically modified by two further reactions. First, in the reaction with a succinic anhydride solution (143 mM succinic anhydride, 87 % (v/v) 1-methyl-2-pyrrolidone and 13 % (v/v) sodium borate buffer) for 2 hours at room temperature, the amino-silanes were prolonged by a crosslinker. As shown in the schematic drawing of the cross-linking reaction in figure 3.14, the resulting surface was terminated with carboxylic groups. This reaction was ceased by rinsing the surface with deionised water (MilliQ, Millipore; resistivity of 18.2 MΩ·cm) and subsequent drying with inert Ar gas.

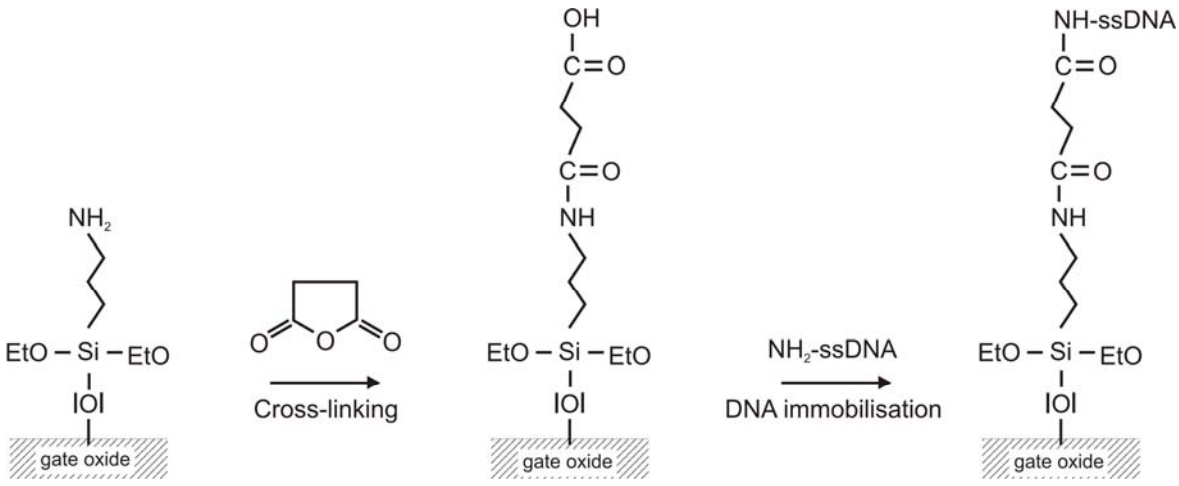


Figure 3.14: Schematic drawing of the chemical surface modifications, which were applied to the silanised gate oxides before the actual DNA detection experiment: The cross-linking and the probe DNA immobilisation reaction. The resulting surface terminates with the probe ssDNA ready for hybridisation with the target ssDNA.

In the second reaction, the two types of amino-terminated probe ssDNA were immobilised on the respective gates through the reaction with the terminating carboxylic group of the crosslinker: By means of a custom-made, video-controlled microspotter system, approximately 65 pl drops of the respective probe DNA solution were spotted onto the gates [Kottuppallil Mathew, 2006]. The 20 nucleobases long sequences of the PM and FMM probe DNA were 5′-amino C6-ATGAACACTGCATGTAGTCA-3′ and 5′-amino C6-TACTTGTGATGTA-CATCAGT-3′, respectively. Both probe DNA solutions contained 3 µM of the respective DNA in morpholine-ethanesulfonic (MES) buffer so1ution, which was composed of 0.1 M 4-MES acid monohydrate, 0.5 M NaCl and

10 mg/ml 1-ethyl-3-(3-dimethylaminopropyl) carbodiimide hydrochloride as condensing agent (pH 7). The immobilisation reaction was carried out overnight at 37 °C. As shown in the schematic drawing of the DNA immobilisation reaction in figure 3.14, the resulting surface offers the terminating probe ssDNA for hybridisation.

At the beginning of the actual DNA detection (hybridisation) experiment, the gates were exposed to standard TE buffer (10 mM TRIS, 1 mM EDTA, NaOH for the adjustment to pH 8) until the long-term drift of the ISFETs had saturated. Then the TE buffer was exchanged for 3 µM target ssDNA dissolved in TE buffer. The hybridisation reaction was given 10 minutes, after which the target DNA solution was exchanged for TE buffer.

3.7 Cell experiments

3.7.1 Biocompatibility

Biocompatibility is an essential prerequisite of high-k dielectrics for their employment as interface in the cell-transistor coupling. Therefore, the non-toxicity of PLD deposited Al_2O_3, YSZ, $DyScO_3$, CeO_2, $(La,Gd)ScO_3$, and $LaAlO_3$ films were tested by culturing embryonic rat cortical neurons on their surfaces. In all cases, silicon chips were used as substrate and the high-k film thicknesses ranged from 70 to 100 nm. Primary mammalian neurons were chosen for the biocompatibility experiments, because they constitute a very sensitive cell system [Banker and Goslin, 1990]. After 10 to 11 days in vitro (DIV), the biocompatibility was judged visually by the general morphology of the neurons and in particular by the outgrowth of axons and dendrites. As control, the neurons were also cultured on thermally grown SiO_2 surfaces, which are known to exhibit excellent biocompatibity.

In the following the employed dissociated cortical neuron culture is described, which was based on the protocol developed by [Brewer et al., 1993]. The embryos were recovered from pregnant Wistar rats at day 18 in gestation. Their cortices were dissected from the brains in Hank´s Balanced Salt Solution (HBSS) (without Ca^{2+} and Mg^{2+}), to which 2 mM $NaHCO_3$, 1 mM sodium pyruvate, 10 mM HEPES, 20 mM glucose and NaOH for the adjustment to pH 7.4 were added. Subsequently, the single cells were dissociated via mechanical trituration in the described HBSS solution by using a fire-polished siliconised Pasteur pipet. Then two volumes of HBSS (with Ca^{2+} and Mg^{2+}) containing the same additives as the above described HBSS and also of pH 7.4, were added. After waiting for three minutes for the non-dispersed tissue to settle, the supernatant was transferred to a new tube and centrifuged at 200 g for two minutes. The pellet was resuspended in 1 ml neurobasal medium, 1x B27 and 0.5 mM L-glutamine per isolated cortical hemisphere.

An aliquot of the cell suspension was diluted 1:4 with trypan blue. The unstained cells were counted in a Neubauer counting chamber. Approximately $4 \cdot 10^6$ cells were recovered on average per cortical hemisphere. The remaining cells were diluted in the neurobasal medium and plated onto the chips at a density of 16 000 cells per cm^2. To enhance the cell growth, the chips were coated with proteins before plating: The chip surfaces were covered for one hour with HBSS (without Mg^{2+} and Ca^{2+}) containing 10 µg/ml poly(D)lysine and 110 µg/ml extracellular cell matrix (ECM) gel. Subsequently, HBSS was removed by aspiration and the chips were rinsed with deionised water. The plated cells were grown at 37 °C in an atmosphere of 5 % CO_2 and 95 % air at a relative humidity of approximately 95 %. Half of the medium was exchanged every three to four days.

3.7.2 Cell-transistor coupling with the cardiomyocyte cell line HL-1

The cardiac muscle cell line HL-1, which was derived from the AT-1 mouse atrial cardiomyocyte tumor lineage by [Claycomb et al., 1998], was chosen as model cell system in the cell-transistor coupling experiments for four reasons: Firstly, HL-1 is a robust cell line simplifying the cell culture. Secondly, since it is a cardiac cell line, HL-1 has the advantage of exhibiting spontaneous APs and does not need to be stimulated. Thirdly, in contrast to primary cardiomyocytes, HL-1 cells exhibit in general always the same AP. Hence, ISFET recordings from HL-1 cells are well suited to compare the properties of different gate dielectrics. And finally, the continued proliferation also after plating onto the ISFET chips allows to perform the coupling experiments, when the HL-1 cells have formed a dense layer and optimally seal the sensing ISFET gate from the bulk electrolyte. In the following, first the electrical activity of the cardiac muscle cell line HL-1 is explained. Subsequently, the protocols of the cell culture and of the coupling experiments are described.

Like primary cardiomyocytes, the HL-1 cells exhibit spontaneous APs, when its cells have formed a dense layer [Sartiani et al., 2002]: The structure of the cell layer is such, that the membranes of neighbouring cells are connected to each other over so-called gap junctions, which allow transduction of membrane potential changes from cell to cell. Some cell region of the layer will adopt the pacemaker function: The spontaneous APs of the pacemaker cells evoke a depolarisation (rise in membrane potential) in their neighbouring cells causing them to exhibit an AP as well, which again depolarises their neighbouring cells. In consequence, the electrical activity in the cell layer spreads from the pacemaker region to all directions.

The signal shape of the HL-1 AP is comparable to the AP of a typical human cardiomyocyte, which is depicted in figure 3.15 and consists of three stages [Schrader, 2001]: Initially, the cell is depolarised from the AP of a neighbouring cell. The depolarisation causes voltage-gated Na^+ channels to open. Hence, during the first stage of

fast depolarisation, the membrane potential moves near the Na^+ equilibrium potential given by the Nernst equation (2.34). During the second stage of the plateau phase, voltage-gated Ca^{2+} channels, which have a slower opening kinetics than the Na^+ channels, keep the cell depolarised although the Na^+ channels have already closed again. The final stage of repolarisation brings the cell back to its resting potential and is caused by voltage-gated K^+ channels, which have a very slow opening kinetics (see figure 3.15). When all K^+ channels have closed again, the cell is ready for the next AP.

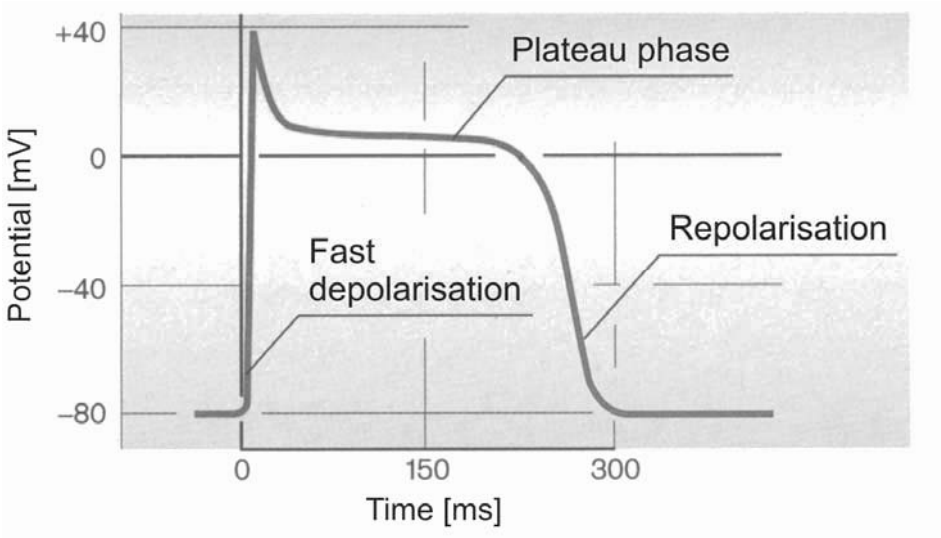


Figure 3.15: Schematic graph of the AP of a typical human cardiomyocyte with the three stages fast depolarisation, plateau phase and repolarisation. Adapted from [Schrader, 2001].

The exponentially proliferating HL-1 cell culture (approximate doubling rate of 24 hours) was maintained in Claycomb medium (JRH Biosciences) supplemented with 10 % (v/v) fetal bovine serum, 100 units/ml penicillin, 100 µg/ml streptomycin, 0.1 mM norepinephrine and 2 mM L-glutamine. The culture was split twice a week as follows: The cells were detached from each other and from the bottom of the culture flask by rinsing several times with bidistilled water containing 0.05 % (v/v) trypsin and 0.05 % (w/v) EDTA, which respectively was removed by aspiration. Soybean trypsin inhibitor was added directly onto the cells to inactivate the enzyme. Claycomb medium was then added, in which the cells were centrifuged at 500 g for five minutes. The pellet was resuspended in Claycomb medium. Finally, one third of the volume was transferred into each of three flasks, which had been gelatine/fibronectin-coated as follows: The day before, the bottom of the flasks was covered with bidistilled water containing 0.02 % (w/v) gelatine and 0.05 % (v/v) fibronectin. Then flasks were incubated at 37 °C overnight. The gelatine/ fibronectin was removed by aspiration directly before adding the cells to the flasks.

For cell-transistor coupling experiments with HL-1 cells, the transistor chips were cleaned and coated as follows: The cells from the last experiment were removed

mechanically by filling the chip with 70 % v/v ethanol and rubbing the surface with cotton buds. Subsequently, the chips were exposed to ultrasound for three minutes in a detergent solution of 2 % v/v Hellmanex (Helma GmbH). After rinsing with bidistilled water to remove the detergent, the chips were exposed to ultrasound for a second time for three minutes in bidistilled water. For sterilisation, the chips were first kept at 160 °C for two hours and then filled with 70 % ethanol for 10 minutes. Finally, the chip surface was coated with gelatine/fibronectin in the same way as described above during splitting the cell culture. The cells were plated onto the chips at such a density, that the cells formed a dense layer, which exhibited spontaneous APs, after three to five days. The medium was exchanged approximately every 24 hours. The cells were grown at 37 °C in an atmosphere of 5 % CO_2 and 95 % air at a relative humidity of approximately 95 %.

In order to reveal all details of the coupled signals and to allow proper comparison between the recordings of ISFETs with different gate dielectrics, the measurements were averaged by a self-programmed software routine (Matlab 6.5, The MathWorks Inc.) as follows: First the positions in time of the individual APs in the respective recording were detected by determining the signal maxima (minima) above (below) a certain threshold. Subsequently, the AP data sets were defined by selecting the time interval before and after the determined maxima (minima), which belonged to the AP. Then the cross-correlation functions between pairs of AP data sets were calculated to determine the corresponding time points in the sets. Finally, the data sets were averaged by superposing the corresponding data points of all AP data sets [Sommerhage].

3.7.3 Cell-transistor coupling with the HEK 293 cell line

The second cell system employed in the cell-transistor coupling experiments was the human embryonic kidney (HEK) 293 cell line [Wrobel et al., 2005], which was stably transfected with a voltage-gated K^+ channel [Frings et al., 1998]. The original HEK 293 cell line, which was created by [Graham et al., 1977] by transformation of human embryonic kidney cells with sheared adenovirus 5 DNA, possesses only a very low density of ion channels. Accordingly, the transfected voltage-gated K^+ channel dominates the electrophysiology of the employed HEK 293 cell line. This electrophysiological simplicity makes the used HEK 293 cells an ideal model to study the basic properties of the cell-transistor coupling. Moreover, the HEK 293 cells offer two further advantages common to all cell lines: Firstly, the robustness of the cells simplifies their culture. And secondly, the continued proliferation also after plating onto the ISFET chips allows to perform the coupling experiments, when the cells have formed a dense layer and optimally seal the sensing ISFET gate from the bulk electrolyte.

During coupling experiments, the voltage-gated K^+ channels were opened by a depolarising voltage pulse applied with the whole-cell patch-clamp technique: A glass pipet with a small aperture of 1 to 2 µm was filled with a chlorinated silver wire as

electrode and HEK 293 intracellular solution of the following composition: 125 mM KCl, 2 mM $MgCl_2$, 10 mM EGTA-KOH, 10 mM HEPES, 5 mM Na-ATP and NaOH for the adjustment to pH 7.4. The as-prepared pipet was brought into contact with the membrane of a cell grown directly on an ISFET gate. By applying a moderate negative pressure to the pipet, the membrane was sucked into the pipet forming a high resistance between the inside of the pipet and the extracellular bath solution on the order of GΩ. Subsequently, the part of the membrane spanning the pipet aperture was removed by applying a more vigorous negative pressure pulse. Since the electrode inside the pipet was now directly in contact with the cytosol, the membrane potential could be set by controlling the voltage between the pipet electrode and the reference electrode in the bulk electrolyte. Amplitude and duration of the employed voltage pulses were on the order of 100 mV and 300 ms, respectively.

The HEK 293 cells have typical intracellular and extracellular K^+ concentrations of 125 mM and 5 mM, respectively, and a resting potential on the order of -70 mV. Hence, after opening the K^+ channels with the depolarising voltage pulse of the patch-clamp pipet, K^+ ions flowed out of the cell. An EPC-9 patch-clamp amplifier (HEKA Elektronik) was operated in the so-called voltage-clamp mode, which allowed to record the K^+ outward current while applying the voltage pulse. Moreover, the changes in the drain-source current of the ISFET were amplified by the custom-made electronics and then fed into the external input of the EPC-9. The software TIDA (HEKA Elektronik) was employed to record simultaneously the membrane currents and the corresponding ISFET signals at respectively 20 kHz. In the analysis, TIDA was also used to average the recordings in order to reveal the details of the coupled signals.

The exponentially proliferating HEK 293 cell culture (approximate doubling rate of 24 hours) was maintained in minimal essential medium (Sigma) supplemented with 2 mM glutamine, 1 % (v/v) nonessential amino acids, 10 % (v/v) fetal calf serum, 100 units/ml penicillin, 0.1 mg/ml streptomycin (M 10 medium). The culture was split weekly as follows: First the cells were washed two times with phosphate buffered saline (PBS) (137 mM NaCl, 2.7 mM KCl, 8.1 mM Na_2HPO_4, 1.5 mM KH_2PO_4) to contain the cells in Ca^{2+}-free solution. Then trypsin (0.5 mg/ml trypsin; 0.2 mg/ml EDTA), an enzyme that cleaves protein chains in the absence of Ca^{2+} was added for 5 minutes at 37 °C and detached the cells from each other and from the substrate. Subsequently, cells were suspended in Ca^{2+} containing M 10 medium and centrifuged for 5 minutes at 200 g. The pellet was resuspended in M 10 medium. Parts of the cells were kept for the culture, while the rest was plated onto the ISFET chips at densities of 70 000 to 100 000 cells per cm^2.

Before plating, the ISFET chips were cleaned and sterilised as described in chapter 3.7.2 and coated with poly(L)lysine as follows: The chips were covered for 30 minutes with PBS containing 0.1 mg/ml poly(L)lysine. Subsequently, poly(L)lysine PBS was removed by aspiration and the chips were rinsed with PBS. The cells were grown at 37 °C in an atmosphere of 5 % CO_2 and 95 % air at a relative humidity of approximately 95 %.

The coupling experiments were performed on day three to five after plating. The medium was exchanged every three days.

4 Results

4.1 Surface characterisation of high-k dielectric thin films

4.1.1 Refractive indices of YSZ, $DyScO_3$, Al_2O_3 and CeO_2

Due to the lack of literature values for the refractive indices at $\lambda = 532$ nm of $DyScO_3$ and of the YSZ composition used in the work of this thesis (10 % mol Y_2O_3), these indices were determined by multi-angle ellipsometry and subsequent fitting. Additionally, the refractive indices of Al_2O_3 and CeO_2 were determined for comparison with the literature. The extinction coefficient k of the complex refractive index was neglected during fitting, because it is zero for dielectrics. As a typical example, figure 4.1 shows the ellipsometric multi-angle data and the corresponding fit for a 175 nm thick YSZ film on an ultrathin SiO_2 layer of 3 nm thickness. For both Δ and Ψ, the fit values agree very well with the measured data (deviation $\leq 0.6°$) in the entire angle range from 50° to 76°.

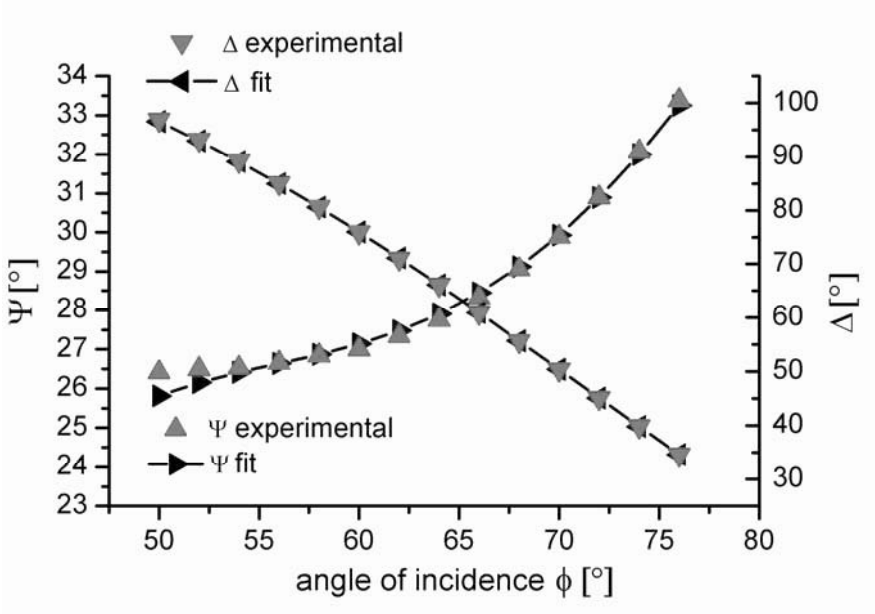


Figure 4.1: Ellipsometric multi-angle measurement (red triangles pointing upwards and downwards) of a YSZ (10 mol % Y_2O_3) film at $\lambda = 532$ nm for the determination of the thickness and the refractive index by fitting. The black triangles pointing to the left and right, which are connected by a black line, are fitted data points corresponding to d = 175 nm and n = 2.22.

Table 4.1 lists the experimentally determined refractive indices and the corresponding literature values as far as available. The measured refractive indices of Al_2O_3 and YSZ agree very well with standard literature values. For CeO_2, a large value range from 1.7 to 2.5 has been reported. The underlying reason is the dependence of the refractive index on the film density and crystallinity, respectively, which are a strong function of the deposition method and the process parameters during the deposition

[Mechin et al., 1998]. The index measured for CeO_2 lies at the upper end of the range suggesting high density films.

Material	Refractive index at $\lambda = 532$ nm	Literature value
YSZ	2.22 (10 mol % Y_2O_3)	2.20 (5 mol % Y_2O_3), $\lambda = 532$ nm [Mechin et al., 1998]
$DyScO_3$	2.17	–
Al_2O_3	1.73	1.77, $\lambda = 486$ nm, 546 nm [Palik, 1998]
CeO_2	2.42	1.7 – 2.5, $\lambda = 550$ nm [Mechin et al., 1998]

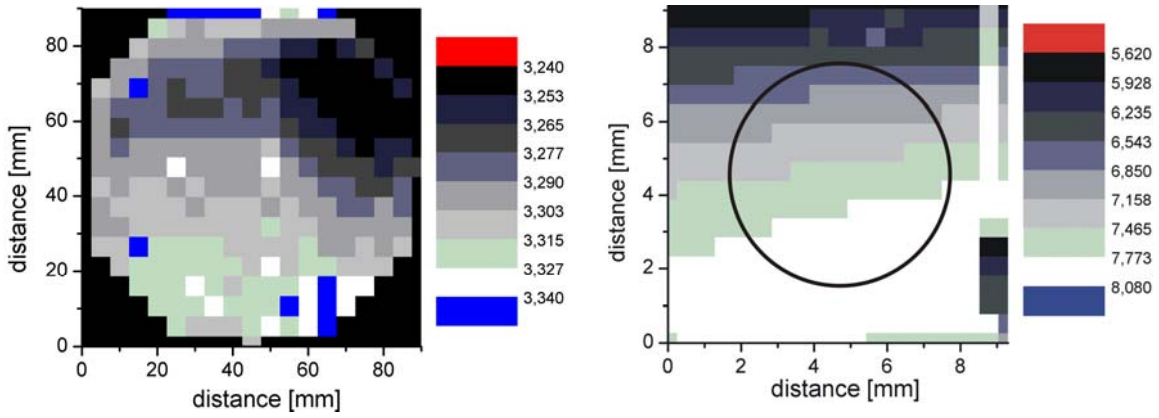
Table 4.1: Refractive indices of PLD deposited high-k dielectrics at $\lambda = 532$ nm determined from ellipsometric multi-angle measurements and the corresponding literature values.

4.1.2 Thickness homogeneity of ultrathin SiO_2 and high-k dielectric films

The ultrathin SiO_2 films with the highest interface quality were achieved by dry furnace oxidation at 820 °C for 2 min in pure O_2. At the beginning of the oxidation interval, the process gas was exchanged from N_2 to O_2 and backwards at its end. Due to the considerable volume of the furnace (approximate length of 2 meters), the homogeneity of the gas exchange over the wafer surface and its reproducibility were questionable. Because of the very short oxidation time, irreproducible or inhomogeneous gas exchange would result in an irreproducible or inhomogenous SiO_2 film thickness, although it is known that the surface morphology of silicon wafers is generally well preserved during thermal oxidation of ultrathin SiO_2 films [Homma et al., 1991; Fujimura et al., 2000].

However, the ellipsometric results showed that the film thickness was highly reproducible: All 2 min oxidations at 820 °C ($N \sim 20$) yielded an ellipsometric film thickness of 3.3 – 3.5 nm. The thickness homogeneity over the wafer surface was determined from ellipsometric surface scanning. Figure 4.2a shows a typical thickness map of an accordingly oxidised 4´´ wafer. The SiO_2 film thickness was extremely homogeneous with a maximum variation over the entire wafer of only 0.1 nm.

Due to the dimension of the PLD sample holder, all high-k dielectric thin films were deposited onto (10 x 10) mm^2 cut wafer pieces. Figure 4.2b shows the ellipsometric thickness map of a 7.5 nm thick $DyScO_3$ film, which was deposited onto a homogeneous 3.5 nm thick SiO_2 layer. The black central circle of 6 mm in diameter represents the o-ring within the electrochemical cell and encloses the relevant area in the electrochemical experiments. Also during the deposition of high-k materials onto transistor chips, all gates were situated inside the black circle.



a **b**

Figure 4.2a: Ellipsometric thickness map of an ultrathin SiO_2 film on a 4´´ silicon wafer after dry furnace oxidation in pure O_2 atmosphere at 820 °C for 2 min. The grid of the data points is 5 mm. The colour code to the right gives the SiO_2 thickness in nm.
b: Ellipsometric thickness map of a thin PLD deposited $DyScO_3$ film, which was deposited onto a thermally oxidised silicon chip (820 °C for 2 min) of 10 by 10 mm in dimension. The grid of the data points is 0.5 mm. The colour code to the right gives the SiO_2 thickness in nm.

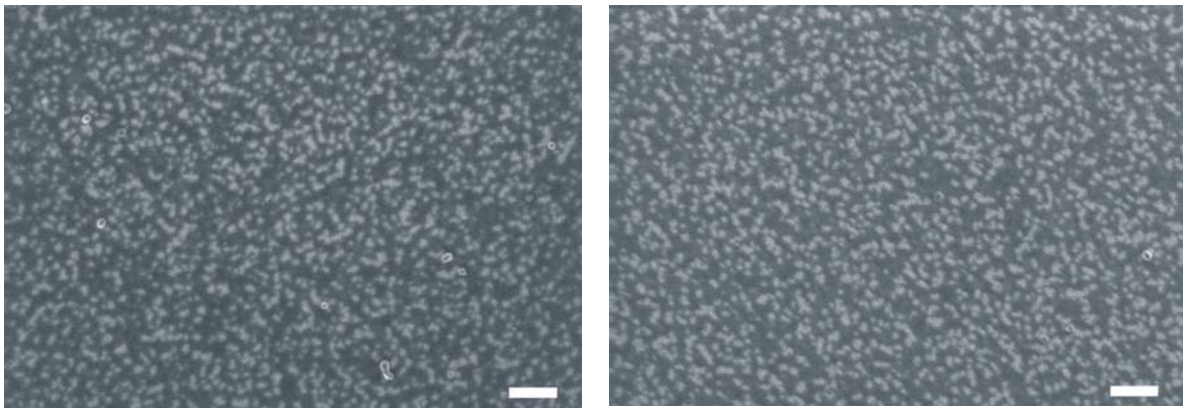
The $DyScO_3$ thickness inside the relevant area ranged from 6.5 nm to 8.1 nm with an arithmetic mean of 7.5 nm. In the central chip region, where all standard thickness measurements of the produced high-k films were performed (adjustment by eye), the film thickness ranged from 7.2 nm to 7.8 nm. This corresponded to a maximum deviation from the mean value of only 4 % indicating excellent macroscopic thickness homogeneity. Since figure 4.2b constituted a typical high-k dielectric thickness map, an error of 4 % was assumed for all ellipsometric thickness measurements of high-k materials.

4.1.3 Surface roughness of ultrathin SiO_2 and high-k dielectric films

Since the thickness measurements with the employed ellipsometers integrated over areas of at least (10 x 10) μm^2 in size, ellipsometry was not suited to investigate the microscopic surface roughness and the important question whether a thin film covers the entire surface densely. Therefore SEM and AFM measurements were performed on films of Al_2O_3, YSZ and $DyScO_3$ of 12 – 14 nm thickness and for comparison on 3.4 nm thick SiO_2 films (dry furnace oxidation at 820 °C for 2 min), onto which all high-k dielectric films were deposited.

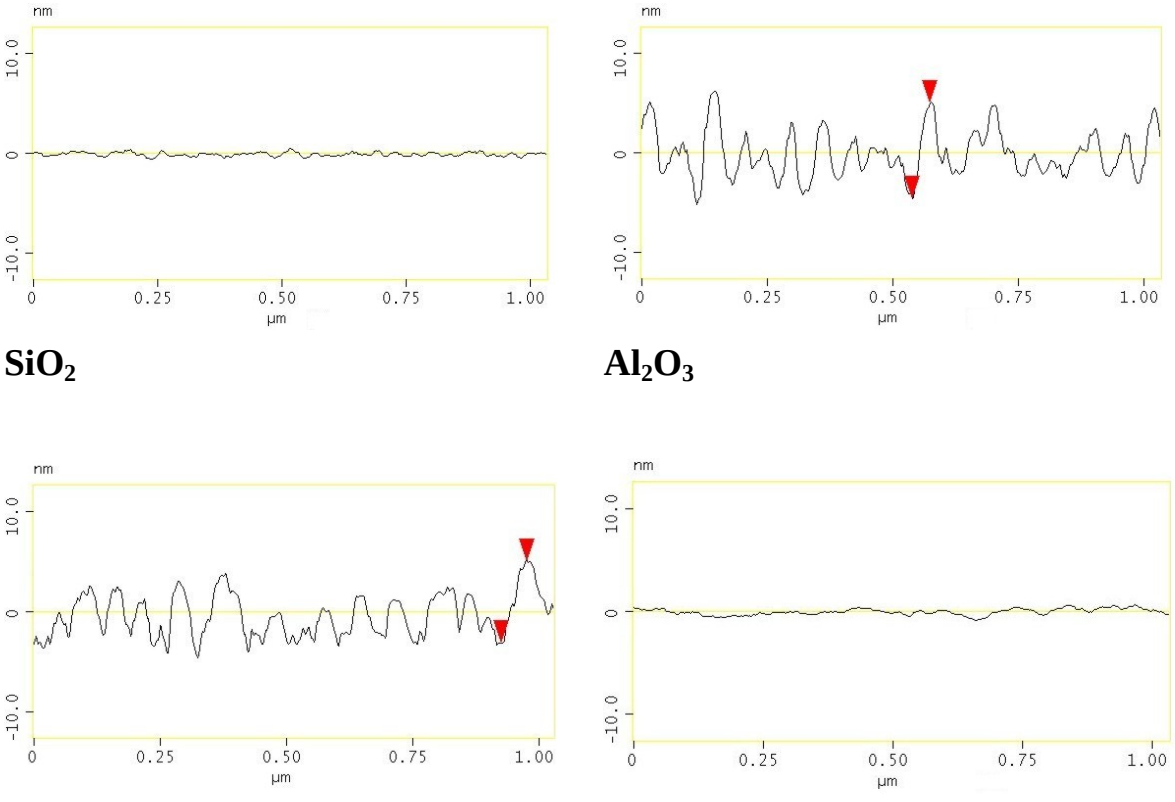
Since SEM imaging of SiO_2 and $DyScO_3$ films did not reveal any inhomogeneities, the corresponding images are not shown. By contrast, the imaging of both Al_2O_3 and YSZ films visualised structures on the order of 10 – 40 nm in lateral dimension (see figure 4.3) indicating a non-uniform film thickness. These results were confirmed by AFM measurements depicted in figure 4.4b: While SiO_2 and $DyScO_3$ film surfaces appear atomically flat (RMS roughness = 0.2 nm and 0.5 nm, respectively), Al_2O_3 and YSZ

surfaces show considerable roughness (RMS roughness = 2.2 nm and 2.1 nm, respectively).



Al_2O_3 **YSZ**

Figure 4.3: SEM images of Al_2O_3 (d = 13 nm) and YSZ (d = 12 nm) films, which were deposited by PLD onto thermally oxidised silicon (820 °C for 2 min). Both scale bars represent 200 nm.

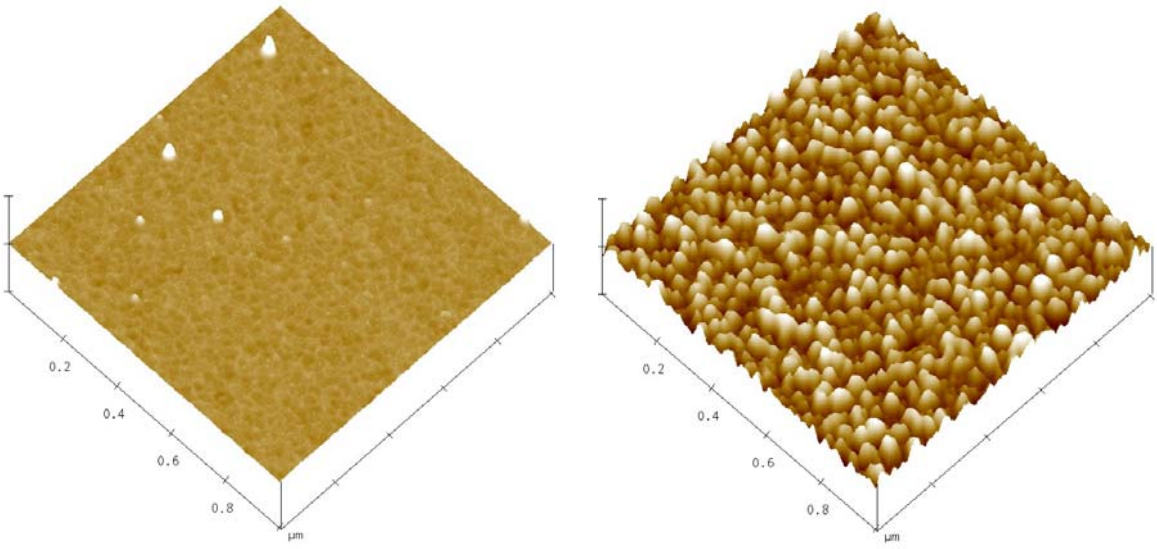


SiO_2 **Al_2O_3**

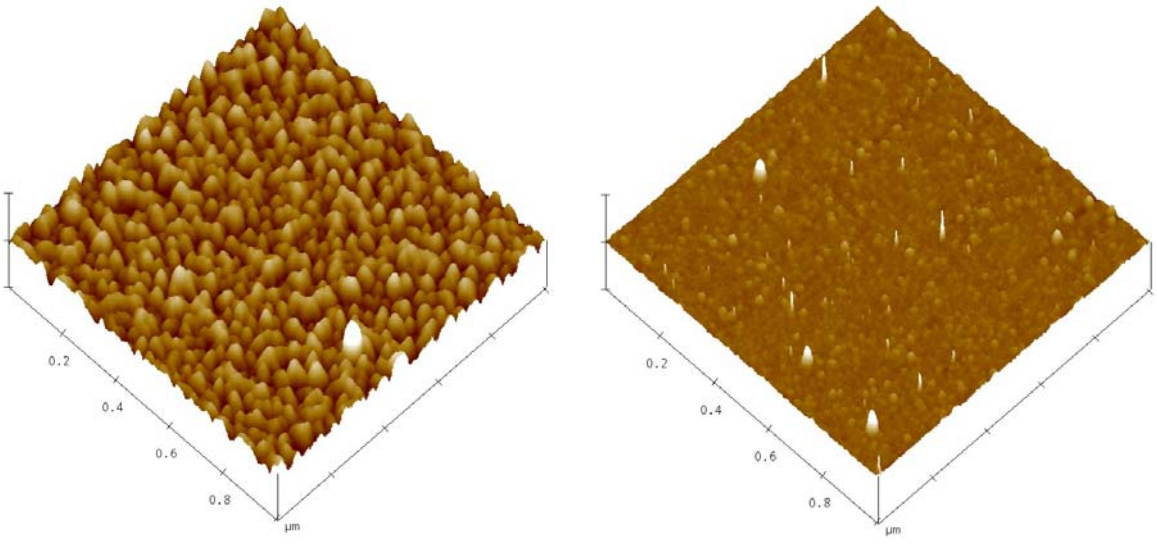
YSZ **$DyScO_3$**

Figure 4.4a: AFM section graphs of an ultrathin SiO_2 film (d = 3.4 nm, dry furnace oxidation at 820 °C for 2 min) and of Al_2O_3 (d = 13 nm), YSZ (d = 12 nm) and $DyScO_3$ (d = 14 nm) films, which were deposited by PLD onto the ultrathin SiO_2 film. The vertical distance between the red markers in the graphs of Al_2O_3 and YSZ represents the maximum hole deepness: 9.7 nm for Al_2O_3 and 8.0 nm for YSZ.

As mentioned earlier in chapter 4.1.2, the surface morphology of silicon wafers is generally preserved during thermal oxidation of ultrathin SiO_2 films explaining the atomic flatness of the SiO_2 film surface. The surface roughness of deposited films is a strong function of the deposition method and the process parameters during the deposition process. For the employed PLD system, the vacuum background gas and pressure and the substrate temperature are the most important parameters for the film quality optimisation. This optimisation has been performed with the $DyScO_3$ deposition process and resulted in the atomically flat $DyScO_3$ films. Analogous optimisation for the Al_2O_3 and YSZ films should result in a comparably small surface roughness.



SiO_2 [RMS roughness = 0.19 nm] **Al_2O_3** [RMS roughness = 2.2 nm]



YSZ [RMS roughness = 2.1 nm] **$DyScO_3$** [RMS roughness = 0.53 nm]

Figure 4.4b: 3-dimensional representation of AFM surface scans of an ultrathin SiO_2 film (d = 3.4 nm, dry furnace oxidation at 820 °C for 2 min) and of Al_2O_3 (d = 13 nm), YSZ (d = 12 nm) and $DyScO_3$ (d = 14 nm) films, which were deposited by PLD onto thermally oxidised silicon (820 °C for 2 min). For all graphs, the tic mark spacing is 25 nm on the z-axis and 0.2 µm on x- and y-axis.

The maximum vertical dimension of the observed inhomogenities in Al_2O_3 and YSZ films was 8 – 10 nm as seen in the AFM section graphs displayed in figure 4.4a. Hence it was concluded that dense surface coverage requires Al_2O_3 and YSZ average film thicknesses as measured by ellipsometry of more than 5 nm. Since the SiO_2 and $DyScO_3$ films were atomically flat (see figure 4.4a), already very thin layers were sufficient for dense surface coverage.

4.2 Dielectric properties of high capacitance films

4.2.1 Dielectric breakdown in thin SiO_2 films

Since the work presented in this thesis aims to replace parts of a thick SiO_2 dielectric film (~ 10 nm) by a high-k dielectric, first the dielectric breakdown in ever thinner SiO_2 films was studied. Figure 4.5 shows the electrochemical I-V characteristics of thermally grown SiO_2 films (dry furnace oxidation at 820 °C) with thicknesses ranging from 2.7 to 6.8 nm. The thickness values were calculated from electrochemical capacitance measurements by applying the plate capacitor formula (equation (3.7)) with the literature value of $\varepsilon_{SiO2} = 3.9$ for the dielectric constant of SiO_2. Hence, these thickness values constitute the electrochemically active dielectric thickness.

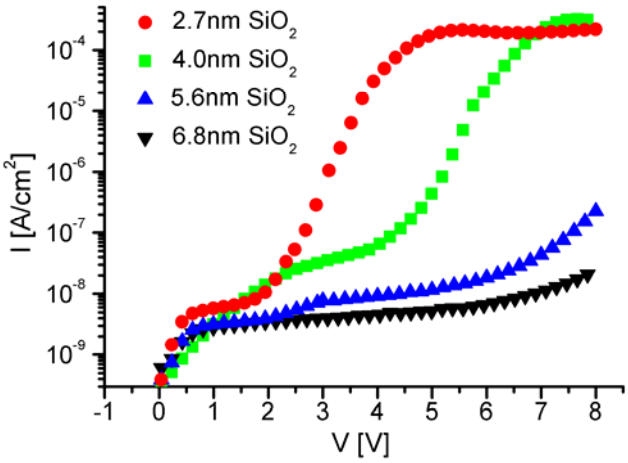


Figure 4.5: Electrochemical I-V characteristics of thermally grown SiO_2 films (dry furnace oxidation at 820 °C between 2 and 45 min) with varying thickness: 2.7 nm (red circles), 4.0 nm (green squares), 5.6 nm (blue triangles pointing upwards) and 6.8 nm (black triangles pointing downwards). The breakdown voltage, which is indicated by a dramatic rise in the current density, is lower for thinner films keeping the breakdown field approximately constant.

The semi-logarithmic plots of figure 4.5 follow theoretical predictions [Green, 2001 and Chou, 1997]: The slow increase in current density at low voltages is attributed to direct

tunnelling and trap-assisted tunnelling. At higher voltages, the slope starts to increase moderately at the onset of Fowler-Nordheim tunnelling and dramatically during the actual breakdown. The current saturation at $(2 – 5) \cdot 10^{-4}$ A/cm^2 is due to limited diffusion of the reacting ion species from the bulk electrolyte to the electrode surfaces during electrolysis.

The rise in current density is relatively sharp for the 2.7 and 4.0 nm thick SiO_2 films and less sharp for the 5.6 and 6.8 nm films leading to the question of defining objectively the breakdown voltage. Throughout this thesis, the voltage, at which the current density exceeds $1 \cdot 10^{-7}$ A/cm^2, is defined as breakdown voltage of the dielectric. This value was suggested by repeated C-V measurements, which were performed by default during I-V recordings: The I-V characteristics were measured in a series of consecutive measurements, each driven to higher voltages than the preceding one. The C-V curves were measured between the single I-V characteristics and compared with each other. When the current density in the I-V measurement reached values on the order of $1 \cdot 10^{-7}$ A/cm^2, the C-V curve was always distorted in comparison with the curve from unstressed films: The curve shoulder was stretched out along the voltage axis and the height of the hump at the shoulder bottom was increased, both indicative of interface state generation. Furthermore, particularly in high-k dielectric films, the flat-band voltage was shifted by several 100 mV suggesting the generation and charging of oxide traps. Both the generation of interface states and of oxide trapped charge are associated with dielectric breakdown.

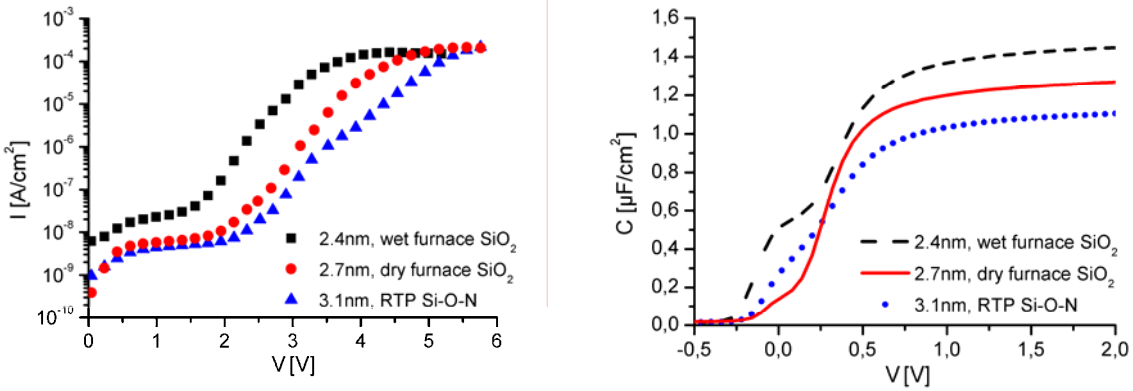
Table 4.2 lists the approximate breakdown voltages and the corresponding electric fields. The breakdown fields, which lie between 10 and 14 MV/cm, are in good agreement with the literature for SiO_2 MOS structures: Dielectric breakdown has been reported in the range from 9 to 30 MV/cm [Sze, 1981] and the onset of Fowler-Nordheim tunnelling has been reported at approximately 6 MV/cm [Chou, 1997].

SiO_2 film thickness [nm]	Breakdown voltage [V]	Breakdown field [MV/cm]
2.7	2.7	10.0
4.0	4.3	10.8
5.6	7.6	13.6
6.8	> 8.0	> 11.8

Table 4.2: Dielectric breakdown voltages (defined as the voltage corresponding to a current density of $1 \cdot 10^{-7}$ A/cm^2) and fields of SiO_2 films with varying thicknesses determined from the electrochemical I-V characteristics of figure 4.5.

4.2.2 Ultrahin SiO_2 and Si-O-N films

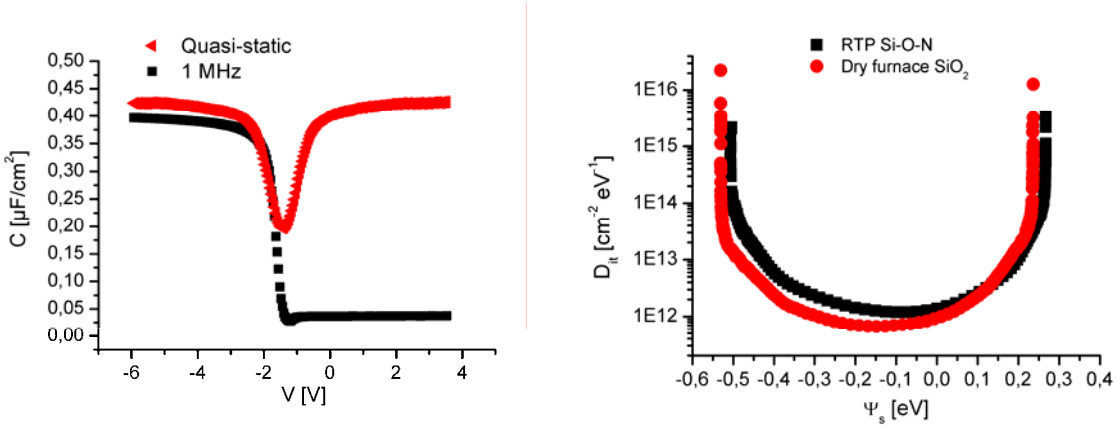
Figure 4.6 shows the electrochemical I-V and C-V characteristics of three differently prepared ultrathin SiO_2 and silicon oxynitride (Si-O-N) films of comparable thickness. All films were grown thermally, but in varying conditions: The 2.4 nm SiO_2 was grown in H_2O atmosphere at 600 °C for 60 minutes in a furnace. The 2.7 nm SiO_2 was also grown in a furnace, but in pure O_2 atmosphere at 820 °C for 2 minutes. The 3.1 nm Si-O-N was grown during a rapid thermal process (RTP) in a mixed atmosphere of O_2 and N_2O (1:1) at 950 °C for 30 seconds. The thickness values were calculated from the electrochemical capacitance measurements of figure 4.6b by applying the plate capacitor formula (equation (3.7)). Since the dielectric constant of SiO_2 was also used for the Si-O-N, these film thicknesses constitute the respective electrochemically active equivalent oxide thickness (EOT), which is defined by the thickness of an SiO_2 film of the same capacitance.



a **b**

Figure 4.6a: Electrochemical I-V characteristics of three differently prepared ultrathin SiO_2 and Si-O-N films of comparable equivalent oxide thickness: 2.4 nm wet furnace SiO_2 (black squares), 2.7 nm dry furnace SiO_2 (red circles) and 3.1 nm RTP Si-O-N (blue triangles).
b: Electrochemical C-V characteristics of the same ultrathin SiO_2 and Si-O-N films: 2.4 nm wet furnace SiO_2 (dashed black line), 2.7 nm dry furnace SiO_2 (red solid line) and 3.1 nm RTP Si-O-N (blue dotted line). All C-V curves were recorded at 1000 Hz.

Figure 4.7a shows typical low-frequency (quasi-static) and high frequency (1 MHz) C-V curves as measured on MOS structures for the calculation of the interface state density D_{it}. Since leakage currents prohibit the determination of D_{it} from ultrathin films, thicker oxides (8 to 9 nm) were used than for the electrochemical characterisation, but with identical preparation except for a prolonged oxidation time and in the case of the Si-O-N a higher oxidation temperature. Figure 4.7b depicts the extracted D_{it} over the silicon band gap for the furnace SiO_2 grown in pure O_2 atmosphere at 820 °C for 60 minutes and the RTP Si-O-N grown in a mixed atmosphere of O_2 and N_2O (1:1) at 1050 °C for 3 minutes.



a **b**

Figure 4.7a: The low-frequency (quasi-static, red triangles) and high frequency (1 MHz, black squares) C-V curves of an 8.1 nm thick SiO_2 (dry furnace oxidation at 820 °C for 60 minutes) MOS structure (squared pad with 200 µm in length), which were used for the calculation of the interface state density. Note: Opposite to the conventions in electrochemistry, the MOS community defines the bias voltage with respect to the grounded silicon and not to the electrolyte. Therefore the voltage values are inverted with respect to the electrochemical measurements.
b: Interface state density D_{it} over the silicon band gap as a function of surface potential Ψ_s for the dry furnace SiO_2 (red circles) and the RTP Si-O-N (black squares). The D_{it} values were calculated from high and low frequency C-V curves measured on respective MOS structures.

Oxidation method	Breakdown field [MV/cm]	D_{it} [10^{11} cm^{-2} eV^{-1}]	C-V curve hysteresis [mV]	Flat-band voltage [V]
Dry furnace SiO_2	9.9	6-10	20	- 0.11
RTP oxynitride	9.5	10-20	20	- 0.15
Wet furnace SiO_2	7.6	> 20	40	- 0.25

Table 4.3: Dielectric properties of three differently prepared ultrathin SiO_2 films: Dry furnace oxide grown at 820 °C for 2 minutes, RTP Si-O-N grown at 950 °C for 30 seconds in a mixture of O_2 and N_2O (1:1) and wet furnace oxide grown at 600 °C for 60 minutes.

The results of the electrochemical and electrical measurements on the three ultrathin SiO_2 and Si-O-N films are summarised in table 4.3. For the comparison of the D_{it} values, it is assumed that the thicker oxides used in the D_{it} measurements, which were prepared with prolonged oxidation times, exhibit the same D_{it} as the respective ultrathin counterparts.

The two most important properties for the evaluation of oxide quality are the breakdown field and the interface state density D_{it}. The breakdown fields of the dry furnace SiO_2 and the RTP Si-O-N are almost identical, whereas the wet furnace SiO_2 breakdown occurs at a more than 20 % lower field (see table 4.3). Furthermore, the lower quality of

the wet furnace SiO_2 is also indicated by the nearly one order of magnitude higher leakage current in the subbreakdown regime (see figure 4.6a), presumably due to higher oxide trap densities.

The quantitative measurements of the interface state density on the MOS structures agree very well with the qualitative results from the electrochemical C-V curves: The higher D_{it} values in the Si-O-N in comparison with the dry furnace SiO_2 (see figure 4.7b) causes the C-V curve of the Si-O-N to be more stretched out along the voltage axis and to exhibit a larger hump at the bottom of the curve shoulder than the SiO_2 curve (see figure 4.6b). An even higher D_{it} value in the wet furnace SiO_2 is concluded qualitatively from the very high hump at the bottom of its C-V curve shoulder (see figure 4.6b).

The flat-band voltage values extracted from the C-V curves and the exhibited C-V curve hysteresis are small for all three oxides (see table 4.3). However, the larger values for the wet furnace SiO_2, which presumably indicate more oxide fixed charge and more charging of oxide traps upon voltage application, respectively, further affirm its lower quality.

Regarding dielectric reliability (evaluated from the breakdown field), oxide fixed charge (evalutated from the flat-band voltage) and the charging behaviour of oxide traps (evaluated from the exhibited hysteresis), the dry furnace SiO_2 and the RTP Si-O-N are of comparable quality (see table 4.3). However, since the interface state density is by a factor of two lower for the dry furnace SiO_2 (see the typical density distributions of figure 4.7b), the dry furnace SiO_2 was employed as interlayer in all SiO_2 – high-k material dielectric stacks presented in this thesis.

In general, the resulting interface state density D_{it} not only depends on the actual oxidation process but likewise on the preoxidation cleaning treatment [Burkman et al., 1993]. During the work of this thesis, variations in the cleaning procedure have been tested such as cancelling the last preoxidation HF dip in the RCA clean, which avoids possible contamination from the HF solution, or performing the last HF dip at lower acid concentrations (0.5 to 1 % HF instead of 10 %), which possibly reduces the silicon surface roughness. However, the measured D_{it} values appeared to be independent from the tested preoxidation treatments.

Keeping in mind the strong dependence of D_{it} values on the entire cleaning and oxidation process, it is evident, that the values presented in this thesis, which were produced in a clean room of class 100, cannot compete with industrially produced SiO_2 and Si-O-N films, which exhibit D_{it} values on the order of only several $10^{10}\,cm^{-2}\,eV^{-1}$ [Green et al., 2001]. Deviation in the processing details is most probably also the reason for the higher D_{it} value of the produced wet furnace SiO_2 in comparison with the reported value of $8\cdot10^{10}\,cm^{-2}\,eV^{-1}$ [Appenzeller et al., 2000].

4.2.3 High-k dielectric thin films

Figure 4.8 shows the equivalent oxide thicknesses d_{EOT} of Al_2O_3, YSZ and $DyScO_3$ films with a dry furnace SiO_2 interlayer as a function of the actual thickness of the high-k films $d_{high\text{-}k}$. The $d_{high\text{-}k}$ values were determined from ellipsometric measurements and range from approximately 7 to 100 nm. The d_{EOT} values of the SiO_2 – high-k dielectric stacks were calculated from electrochemical measurements of their capacitances through the EOT plate capacitor formula (equation (3.8)), which uses the dielectric constant of SiO_2. The dielectric constant ε of the high-k materials and the thicknesses of the SiO_2 interlayers were extracted from the respective linear fits according to equation (3.10) and are summarised in table 4.4. Finally, table 4.4 lists the literature values for the respective dielectric constants. The lowest dielectric constant with 10 ± 1 exhibits Al_2O_3, which is illustrated by the significantly steeper slope of the Al_2O_3 fit in figure 4.8 in comparison with the fits for YSZ and $DyScO_3$. Their respective fit slopes and accordingly their dielectric constants are almost equal (31 ± 2 for YSZ and 29 ± 2 for $DyScO_3$).

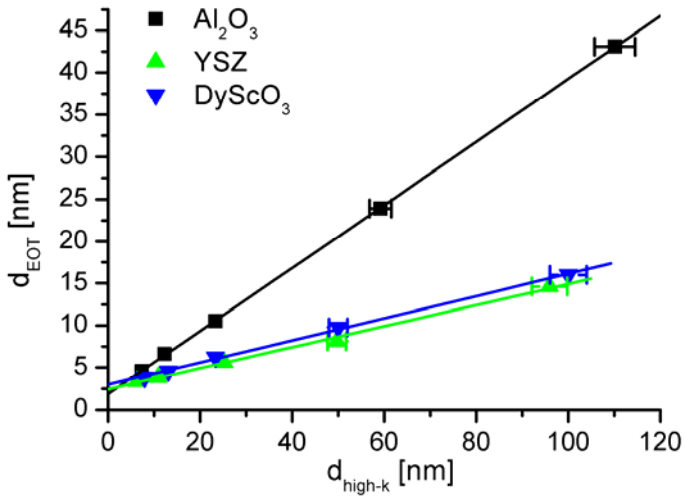


Figure 4.8: Equivalent oxide thickness d_{EOT} of PLD deposited Al_2O_3 (black squares), YSZ (green triangles pointing upwards) and $DyScO_3$ (blue triangles pointing downwards) films with an SiO_2 interlayer (dry furnace oxidation at 820 °C for 2 minutes) as a function of the actual thickness of the high-k films $d_{high\text{-}k}$. d_{EOT} was determined from electrochemical C-V measurements and $d_{high\text{-}k}$ from ellipsometry. The linear fits were used to extract the dielectric constants and the thicknesses of the SiO_2 interlayer. The error bars originate from the ellipsometric thickness measurement.

The measured dielectric constant for Al_2O_3 agrees well with the literature value, whereas both the YSZ and $DyScO_3$ dielectric constants exceed the highest reported values by approximately 20 % (see table 4.4). Since the production of high capacitance films was one essential aim in the work of this thesis, the observed deviation is welcome but rises the question for the underlying reason. The deviation of the YSZ dielectric constant cannot be

attributed to the added 10 mol % Y_2O_3 in comparison with the pure ZrO_2 from the literature value: The reported dielectric constant of Y_2O_3 is with values ranging from 11 to 15 [Young et al., 2003 and Wilk et al., 2001] lower than the ZrO_2 value suggesting an even lower dielectric constant for YSZ than for ZrO_2.

Material	ε (experiment)	ε (literature value)	d_{SiO_2} [nm]
Al_2O_3	10 ± 1	9-11.5 [Young et al., 2003]	1.9
YSZ	31 ± 2 (90 mol % ZrO_2)	22-25 [Young et al., 2003] (pure ZrO_2)	2.4
$DyScO_3$	29 ± 2	22 ± 3 [Zhao et al., 2005]	3.0

Table 4.4: Dielectric constants ε and SiO_2 interlayer thicknesses d_{SiO_2} of the PLD deposited high-k materials, which were determined from the linear fits of the equivalent oxide thickness d_{EOT} as a function of high-k film thickness $d_{high\text{-}k}$. The SiO_2 interlayers were grown thermally (dry furnace oxidation at 820 °C for 2 minutes) prior to the deposition. The third column lists the respective literature value for the dielectric constants.

The equivalent oxide thicknesses d_{EOT}, which originate from electrochemical C-V curves, are undoubted, because the same set-up and analysis was employed for the numerous d_{EOT} measurements on simple SiO_2 films, which agreed perfectly with their independently determined ellipsometric thicknesses. From this it follows, that in case the determined YSZ and $DyScO_3$ dielectric constants are higher than the true values, an error source is present, which shifts the true $d_{high\text{-}k}$ values in figure 4.8 towards higher values resulting in a less steep slope. Furthermore, the absolute magnitude of this error is required to be proportional to the high-k film thickness so that the obtained $d_{high\text{-}k}$ values match a linear fit. The only source, which could produce such a systematic error, is a falsely assumed refractive index. However, since the agreement between the measured and fitted Δ and Ψ values in both the initial ellipsometric refractive index and the successive standard thickness measurements was extremely well (deviation ≤ 1° for Δ and Ψ), it is strongly believed, that the determined dielectric constants are the true values.

In general the dielectric constant of a material is a function of its crystallinity: The higher the crystallinity the higher is the expected dielectric constant [Young et al., 2003]. Therefore, differences in the crystallinity are assumed to account for the observed deviations between the obtained dielectric constants and the literature values.

The SiO_2 interlayer thicknesses, which were extracted from the d_{EOT} fits, range from 1.9 to 3.0 nm (see table 4.4). The electrochemically active thickness of the dry furnace SiO_2 grown at 820 °C for 2 minutes was always in the range between 2.7 and 3.2 nm. This minor deviation in the thickness range can probably be attributed to the experimental errors of the respective ellipsometric and C-V measurements. The fact that

the SiO_2 thickness after the pulsed laser deposition remains on the same order of magnitude as before, may indicate that the high quality of the SiO_2 film survives the temperatures of up to 550 °C and the collisions with the ions and electrons of the plasma during the deposition.

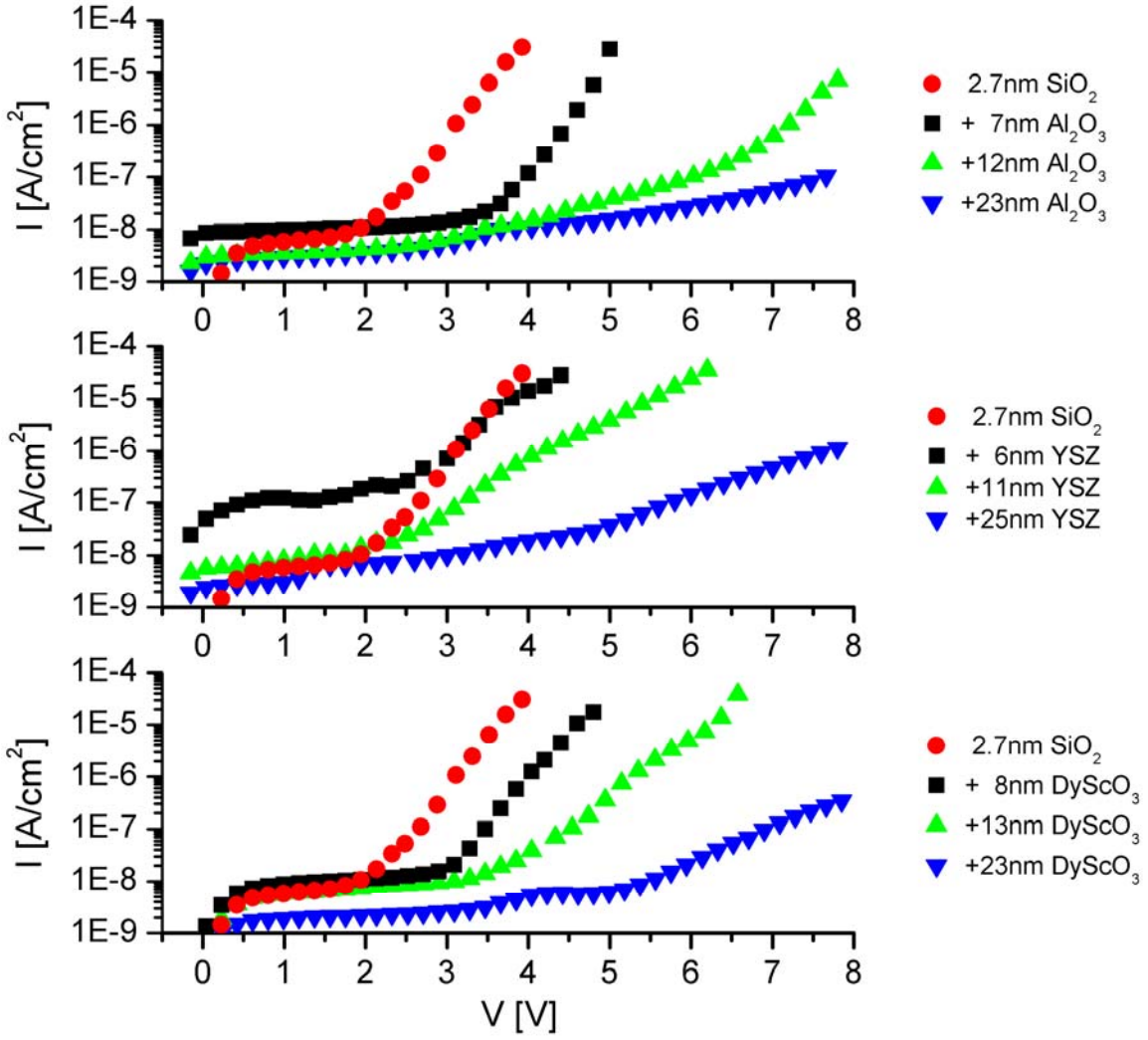


Figure 4.9: Electrochemical I-V characteristics of PLD deposited Al_2O_3 (top), YSZ (centre) and $DyScO_3$ (bottom) films with an SiO_2 interlayer (dry furnace oxidation at 820 °C for 2 minutes). The SiO_2 interlayer has an electrochemically active dielectric thickness of 2.7 nm and its characteristic is shown in each graph as reference (red circles). The high-k material top layers have ellipsometric thicknesses of approximately 7 nm (black squares), 12 nm (green triangles pointing upwards) and 24 nm (blue triangles pointing downwards).

Figure 4.9 shows the I-V characteristics of Al_2O_3, YSZ and $DyScO_3$ films of thicknesses ranging from 6 to 25 nm, which were deposited onto a 2.7 nm thick SiO_2 interlayer. To illustrate the genuine effect of the high-k dielectric films, the characteristic of the interlayer SiO_2 without top layer is added to each graph. It is clearly seen that for all

three materials the dielectric breakdown voltage is shifted to higher values as the film thickness increases.

In the SiO_2 – high-k material stacks of comparable thickness, the dielectric breakdown occurs at the lowest voltages in the YSZ stacks, followed by the $DyScO_3$ stacks, while the Al_2O_3 film stacks exhibit the highest breakdown voltages. However, the respective breakdown fields cannot be concluded from this observation, because the different dielectric constants of the high-k materials lead to a different distribution of the applied voltage between the SiO_2 interlayer and the respective material. Instead the respective high-k dielectric breakdown field has to be calculated from the breakdown voltage of the SiO_2 – high-k material stack by applying the formula for capacitors in series. The results are listed in table 4.5. However, only minimum values are obtained, because it is not possible to distinguish whether the overall dielectric breakdown in the stack was caused by initial SiO_2 or high-k material breakdown. Moreover, since the electric field in the SiO_2 at breakdown was for all stacks on the order of the SiO_2 breakdown field (7 to 12 MV/cm), it is rather likely, that the produced high-k films have breakdown fields on the order of the literature values of 5 MV/cm for Al_2O_3 [Groner et al., 2002] and 3 to 5 MV/cm for ZrO_2 [Wang et al., 2005], which are considerably larger than the obtained minimum values.

Striking is the characteristic of the SiO_2 – 6 nm YSZ stack in comparison with the SiO_2 interlayer film (see figure 4.9, centre): In the subbreakdown regime, the leakage current of the YSZ stack is by one order of magnitude higher and after the dielectric breakdown in both the YSZ stack and the SiO_2 film, their characteristics coincide. Since Zr is known to have a higher affinity to O than Si [Ingebrandt, 1998], the high leakage current may be explained by a partial dissociation of the SiO_2 interlayer by Zr during the YSZ deposition: A reduced SiO_2 thickness constitutes a lower energy barrier for the leakage tunnelling currents.

Figure 4.10 shows the electrochemical C-V characteristics of Al_2O_3, YSZ, $DyScO_3$ and CeO_2 films of 10 to 13 nm thickness, which were deposited onto the 2.7 nm thick SiO_2 interlayer. For the evaluation of the genuine properties of the high-k dielectrics, the characteristic of the SiO_2 interlayer without top layer is added as reference. The quantitative properties of the high-k dielectric stacks, which were extracted from the I-V and C-V characteristics of figure 4.9 and 4.10, are summarised in table 4.5.

The equivalent oxide thicknesses achieved for film stacks with high-k material layers thicker than 10 nm on top of the 2.7 nm SiO_2 interlayer are below promising 5 nm for YSZ, $DyScO_3$ and CeO_2, and still below 7 nm for Al_2O_3 (see table 4.5). Therefore, from the capacitance point of view, all four materials are suited to replace SiO_2 as ISFET gate dielectric.

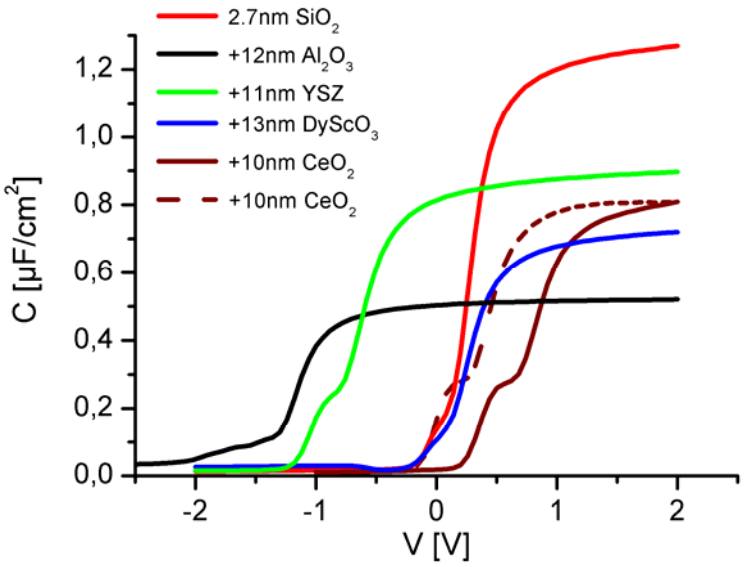


Figure 4.10: Electrochemical C-V characteristics of PLD deposited Al_2O_3 (solid black line), YSZ (solid green line), $DyScO_3$ (solid blue line) and CeO_2 (solid and dashed brown line) films with thicknesses ranging from 10 to 13 nm and a 2.7 nm SiO_2 interlayer (dry furnace oxidation at 820 °C for 2 minutes). The characteristic of the SiO_2 interlayer (red solid line) is shown as reference. All solid lines represent characteristics, which were recorded from accumulation to inversion, whereas the dashed second CeO_2 characteristic was recorded from inversion to accumulation and is shown to illustrate the large hysteresis exhibited by the CeO_2 films. All measurements were performed at 1000 Hz.

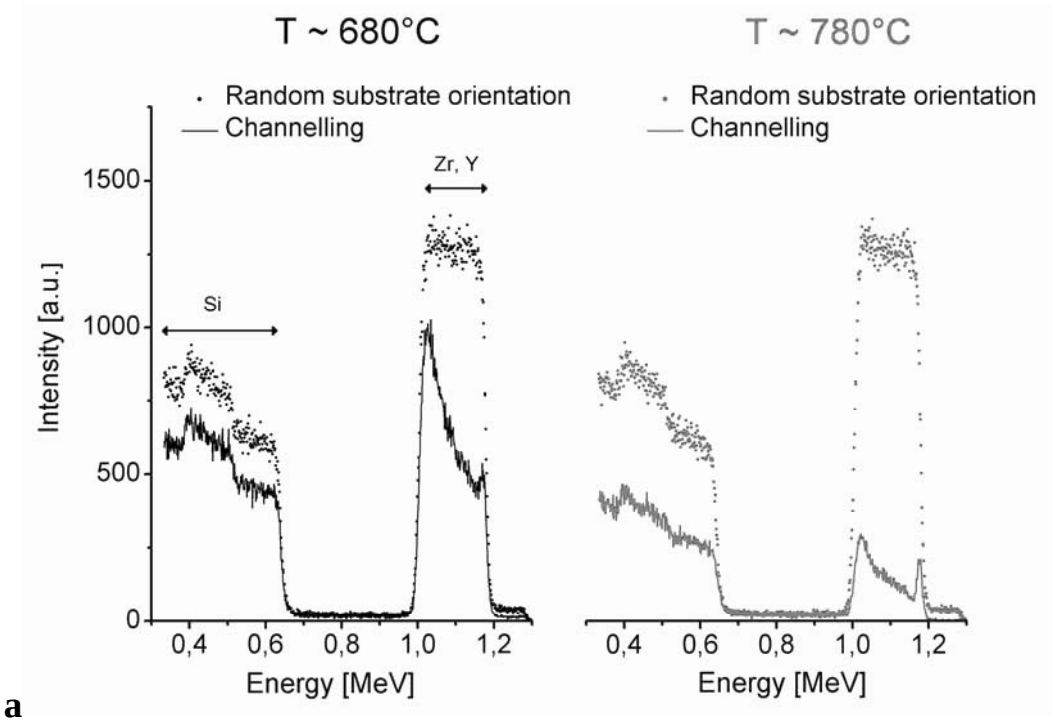
Material	$d_{high\text{-}k}$ on top of 2.7 nm SiO_2 [nm]	d_{EOT} [nm]	Breakdown field [MV/cm]	Hysteresis [mV]	Flat-band voltage shift [V]
SiO_2	-	2.7	-	20	0
Al_2O_3	12	6.6	≥ 3.2	20	- 1.67
YSZ	11	3.9	≥ 1.0	5	- 1.04
$DyScO_3$	13	4.8	≥ 1.4	70	- 0.05
CeO_2	10	4.3	-	400	+ 0.37

Table 4.5: Dielectric properties of PLD deposited Al_2O_3 (12 nm), YSZ (11 nm), $DyScO_3$ (13 nm) and CeO_2 (10 nm) films with a 2.7 nm SiO_2 interlayer and for reference of the SiO_2 interlayer film without top layer. All values were extracted from the I-V and C-V characteristics of figure 4.9 and 4.10. The minimum breakdown fields for the respective high-k materials were calculated from the breakdown voltage of the stack (defined as the voltage corresponding to a current density of $1 \cdot 10^{-7}$ A/cm^2). The flat-band voltage shifts were determined relative to the flat-band voltage of the SiO_2 film.

The CeO_2 films, however, exceed by far the other materials regarding the exhibited hysteresis (see table 4.5). Hysteresis values as high as 400 mV were measured (see figure 4.10), suggesting high oxide trap densities and large charge injection during voltage sweeping in CeO_2 films. Furthermore, the CeO_2 C-V characteristics show considerably higher humps at the bottom of the curve shoulder in comparison with the SiO_2 reference, indicating an increase of the interface state density during the CeO_2 deposition. In conclusion, these indicators of low CeO_2 film quality lead to the decision to exclude CeO_2 from the implementation as gate dielectric into ISFETs.

The possible increase in interface state density D_{it} during the stressing conditions of the pulsed laser deposition (temperatures up to 550 °C and collisions of the plasma constituents with the surface) is evaluated qualitatively by comparing the C-V curve shapes of the high-k material stacks and the original SiO_2 interlayer (see figure 4.10), the latter having a state density of $(6\text{-}10)\cdot 10^{11}\,cm^{-2}\,eV^{-1}$ as determined earlier. The hump at the bottom of the $DyScO_3$ C-V curve is slightly lower than in the SiO_2 reference indicating no degradation during the $DyScO_3$ deposition. By contrast, the YSZ characteristic exhibits a hump, which is considerably higher than the SiO_2 hump, suggesting an increase in the D_{it} value during YSZ deposition. The same applies to the even higher hump in the CeO_2 characteristic. Finally, the Al_2O_3 characteristic shows an unusual hump, which is extremely stretched out. However, the hump height itself is comparable with the height in the SiO_2 reference, suggesting that the interface state density keeps to the order of magnitude as before the Al_2O_3 deposition. Different substrate temperatures during the deposition process of the respective high-k material and different target characteristics (for instance the used YSZ target releases during the evaporation process YSZ particles, which are up to 10 µm in diameter) are assumed to account for the different degrees in stressing.

The flat-band voltages of the Al_2O_3 and YSZ characteristics shift by more than 1 V towards negative voltages with respect to the flat-band voltage of the original SiO_2 interlayer (see figure 4.10). This large shift is probably due to extensive incorporation of positive charges into the Al_2O_3 and YSZ films. However, since the hysteresis exhibited by both curves is very small (20 mV for Al_2O_3 and only 5 mV for YSZ), almost exclusively oxide fixed charge seems to be responsible for the flat-band voltage shift. The implementation of a dielectric with high oxide fixed charge into FETs changes indeed the gate-source voltage working point, but has no detrimental effects on the performance itself. In particular, the signal-to-noise ratio of the device remains unchanged.



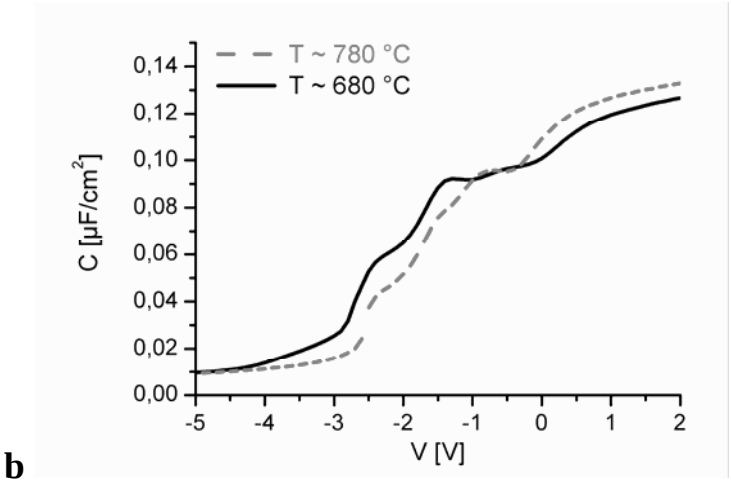


Figure 11a: RBS spectra of two PLD deposited YSZ films, which were grown at substrate temperatures of approximately 680 °C (black curves in the left graph) and 780 °C (red curves in the right graph). The elements responsible for the respective signal regions indicated by the double arrows are given by their symbols in the left graph. The higher reduction of the RBS channelling signal (solid lines) with respect to the signal at random substrate orientation (dotted lines) in the 780 °C YSZ film indicates a considerably higher degree of cristallinity in comparison with the 680 °C film. Crystallinity may result in an increase of the dielectric constant.

b: C-V characteristics of the same two YSZ films, which have identical thicknesses of approximately 200 nm. Since the exhibited capacitances are nearly equal, the expectation of a considerably higher dielectric constant for the 780 °C film was not fulfilled.

The RBS spectra of figure 4.11a illustrate, that epitaxial growth of YSZ on silicon is a strong function of the substrate temperature during the pulsed laser deposition as described in [Ingebrandt, 1998]: The film deposited at approximately 780 °C clearly exhibits higher channelling than the 680 °C film, which indicates better expitaxial growth and a higher degree of crystallinity in 780 °C films. It is known that in general crystalline oxides are more depolarisable in electric fields than amorphous oxides, wherefore crystalline oxides often exhibit higher dielectric constants [Young et al., 2003]. Therefore, a higher dielectric constant was expected for the 780 °C film. However, the capacitance of equally thick YSZ films deposited at 680 °C and 780 °C, respectively, differed in magnitude by less than 5 % (see figure 4.11b). In conclusion, the dielectric constant of YSZ was not significantly increased in epitaxial films in comparison with amorphous films indicating equal depolarisation in electric fields.

4.2.4 Organic monolayers

Figure 4.12 shows the electrochemical I-V and C-V characteristics of dodecene monolayers, which were bound covalently onto silicon. The exhibited capacitance corresponds to an equivalent oxide thickness on the order of only 2.1 nm. The underlying capacitance value had to be extrapolated from the curve shape in figure 4.12b, because the dielectric was broken before the silicon surface had reached complete accumulation, where the true capacitance could have been measured. As seen in figure 4.12a, the dielectric breakdown occurred at voltages of less than 0.5 V. These low values are in agreement with the reported breakdown voltages of identical organic monolayer – silicon structures, where the organic layer was contacted by a mercury probe in place of the electrolyte [Faber, 2005]. It is concluded that due to their very low breakdown voltage, organic monolayers are not suited as gate dielectric for enhancement mode ISFETs as used in the work of this thesis: The layers would not withstand the required application of several volts in gate-source voltage during operation.

The large height of the hump at the bottom of the C-V characteristics indicates a very high interface state density in the organic films, which needs to be lowered for an implementation into depletion mode devices. Moreover, the hump height and accordingly the state density increase further upon the application of moderate voltages of only several 100 mV, as seen in the series of C-V characteristics in figure 4.12b, which were performed at ever higher voltages. The observed simultaneous increase in interface state density and occurrence of dielectric breakdown agree well with the theoretical expectation.

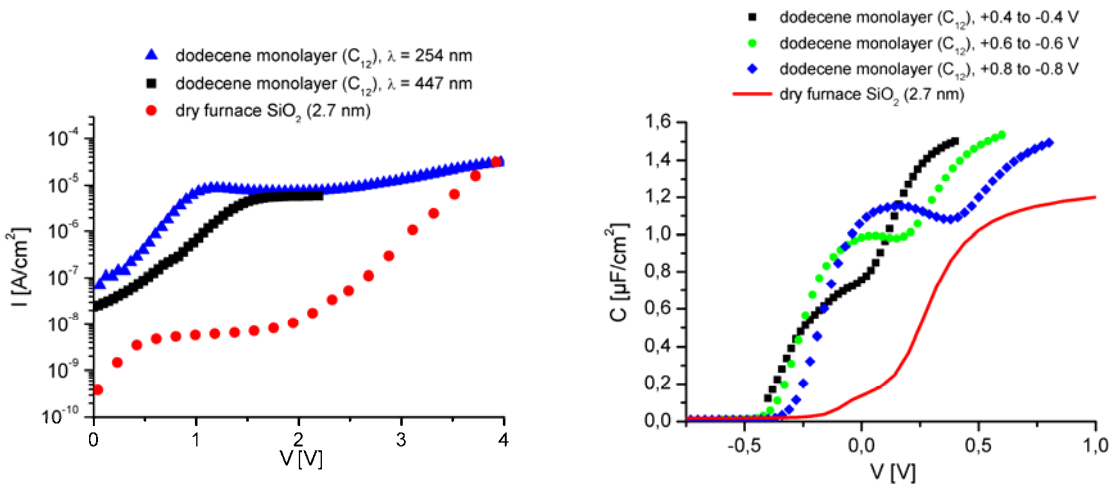


Figure 4.12a: Electrochemical I-V characteristics of covalently bound dodecene (a C_{12} alkane derivative) monolayers on silicon. The layers were formed in a chain reaction mechanism, which was initiated by light of either 447 nm (black squares) or 254 nm (blue triangles) in wavelength. Both layers exhibit breakdown voltages (defined as the voltage corresponding to a current density of $1 \cdot 10^7$ A/cm^2) of less than 0.5 V. For comparison, the characteristic of the 2.7 nm thick dry furnace SiO_2 (oxidation at 820 °C for 2 min, red circles) is added. The current saturation is due to limited diffusion of the reacting ion species from the bulk electrolyte to the dielectric surface.
b: Series of electrochemical C-V characteristics of a covalently bound dodecene monolayer on silicon (initiation of the chain reaction by 447 nm light), which were driven to ever higher voltages: First from +0.4 to -0.4 V (black squares), subsequently from +0.6 to -0.6 V (green circles) and finally from +0.8 to -0.8 V (blue diamonds). For comparison, the C-V curve of the 2.7 nm thick dry furnace SiO_2 (oxidation at 820 °C for 2 min, red solid line) is added. All curves were recorded at 1000 Hz.

4.3 High-k dielectric ISFET characterisation

4.3.1 Transconductance and noise power density

Figure 4.13 shows transconductance curves of high-k dielectric ISFETs and of the standard SiO_2 ISFET, which were obtained by differentiation of typical transfer characteristics recorded at V_{DS} = 3V. The gate width of all ISFETs was 25 µm. The high-k material gate stacks consisted of an approximately 3 nm thick SiO_2 interlayer (820 °C for 2 min) and top layers of approximately 5 nm Al_2O_3, 20 nm YSZ and 15 nm $DyScO_3$, respectively. The corresponding gate capacitances per unit area of the high-k material stacks and of the approximately 9 nm thick standard SiO_2 (820 °C for 60 min) were calculated from the earlier determined dielectric constants (see table 4.4) by using the plate capacitor formula (equation (3.7)) and are given in table 4.6. Furthermore, table 4.6 lists the respective maximum value in transconductance g_m and the threshold voltage shifts with respect to the

standard SiO_2 ISFET, which both were extracted from the graphs of figure 4.13. For the determination of the threshold voltage shifts, the transconductance maximum was used as reference point. The maximum g_m^{eff} values given in table 4.6 were calculated by equation (4.1), which eliminates the influence of the source resistance R_s in a simple approximation as explained shortly.

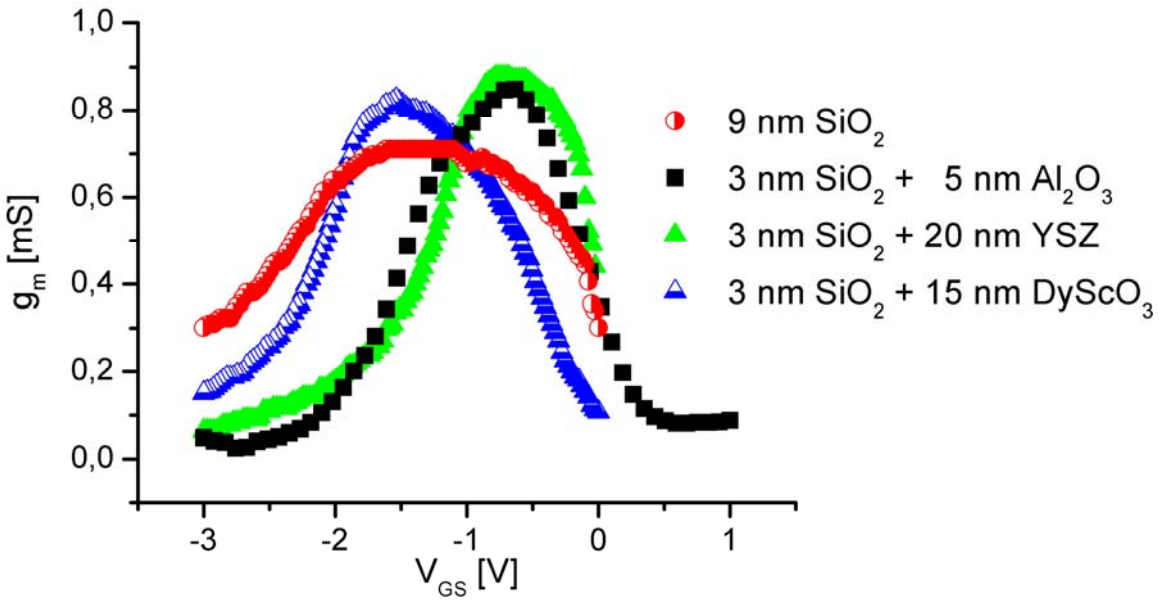


Figure 4.13: Transconductance g_m as a function of the gate-source voltage V_{GS} of Al_2O_3 (5 nm), YSZ (20 nm) and $DyScO_3$ (15 nm) ISFETs with a respectively 3 nm SiO_2 interlayer as gate dielectric. For reference, also the curve of a standard 9 nm SiO_2 ISFET is added. The underlying transfer characteristics were recorded at V_{DS} = -3V. All ISFETs had gate widths of 25 µm.

Gate dielectric	C_{ox} [µF/cm^2]	Maximum g_m [mS]	Maximum g_m^{eff} [mS]	Threshold voltage shift [V]
9 nm SiO_2	0.38	0.71	0.90	0
3 nm SiO_2 + 5 nm Al_2O_3	0.70	0.85	1.14	+ 0.73
3 nm SiO_2 + 20 nm YSZ	0.63	0.88	1.19	+ 0.63
3 nm SiO_2 + 15 nm $DyScO_3$	0.69	0.83	1.10	- 0.18

Table 4.6: Characteristic properties of the high-k dielectric and for reference of the standard SiO_2 ISFETs. The film thicknesses were measured ellipsometrically and used to calculate the gate capacitances per unit area. The maximum g_m values and the threshold voltage shifts with respect to the SiO_2 ISFET were determined from the transconductance curves of figure 4.13. The maximum g_m^{eff} values were calculated by equation (4.1).

The results of the gate capacitances and of the maximum transconductances (see table 4.6) do not show good agreement with the theoretical predictions of the long-channel FET equation (equation (2.12)): According to the derivative of equation (2.12) for V_{GS}, the transconductance is expected to be proportional to the gate capacitance. However, the capacitances of the high-k dielectric stacks exceed the capacitance of the standard SiO_2 by 66 to 84 %, whereas the maximum transconductance values of the high-k dielectrics exceed the SiO_2 value by only 17 to 24 %.

Two reasons may be responsible for the disagreement. Firstly, the channel length of the ISFETs used in the work of this thesis was aimed for 2 µm. The long-channel FET equation however, is only valid for channel lengths above 10 µm [Muller and Kamins, 2002]. Hence, the observed deviation of the experimental data may be due to the shorter channel length. Secondly, it is known that high series resistances of the source and drain feed lines cause lower drain-source currents and consequently lower transconductance values [Paul, 1994]. Accordingly, the source and drain feed line resistances of the used ISFETs may be sufficiently high to give rise to the observed deviation. The following simple approximation was used to study the effect of the feed line resistances: To eliminate the influence of the source resistance R_s, which was on the order of 200 Ω for the employed ISFETs, the actual gate-source voltage V_{GS} was replaced by an effective gate-source voltage $V_{GS}^{eff} = V_{GS} - I_{DS} \cdot R_s$. The effective transconductance g_m^{eff}, which would have been exhibited if $R_s = 0$, was then calculated by

$$g_m^{eff} = \frac{\partial I_{DS}}{\partial (V_{GS} - I_{DS} \cdot R_s)} \tag{4.1}$$

As seen in table 4.6, all maximum g_m^{eff} exceed their corresponding g_m value by 27 to 35 %. Although the maximum g_m^{eff} do not scale significantly better with C_{ox} than the g_m values, the increase of the transconductance by this approximation indicates that the source and drain feed line resistances probably limit the performance of the used ISFETs.

The threshold voltage shifts of the Al_2O_3 and YSZ ISFETs by more than + 0.6 V with respect to the standard SiO_2 ISFET (see table 4.6) are in agreement with the earlier described flat-band voltage shifts in the C-V characteristics of the corresponding EOS diodes (see table 4.5). As mentioned earlier, these large voltage shifts are most probably due to extensive incorporation of positive charges into the Al_2O_3 and YSZ films during the PLD process. The difference in shift direction between the ISFET threshold voltage and the EOS diode flat-band voltage originates from the different choice in the ground electrode (voltage reference point): In the ISFET graphs, the source is grounded, while in EOS graphs, the electrolyte is grounded.

Figure 4.14 shows the noise power density spectra in the gate-source voltage regime of YSZ, $DyScO_3$ and standard SiO_2 ISFETs. The explicit composition of the respective gate dielectrics and the corresponding gate capacitances C_{ox} are given in table 4.7. As seen by the graphs and by the extracted average noise power densities

between 998 and 1003 Hz (see table 4.7), the recorded noise levels do not differ significantly and are not proportional to C_{ox}^{-2} as predicted by equation (2.19). In conclusion, like the maximum transconductance, the noise level does not scale with the gate capacitance as expected. Again the invalidity of the long-channel FET equation and high source and drain feed line resistances are assumed to be the underlying reasons.

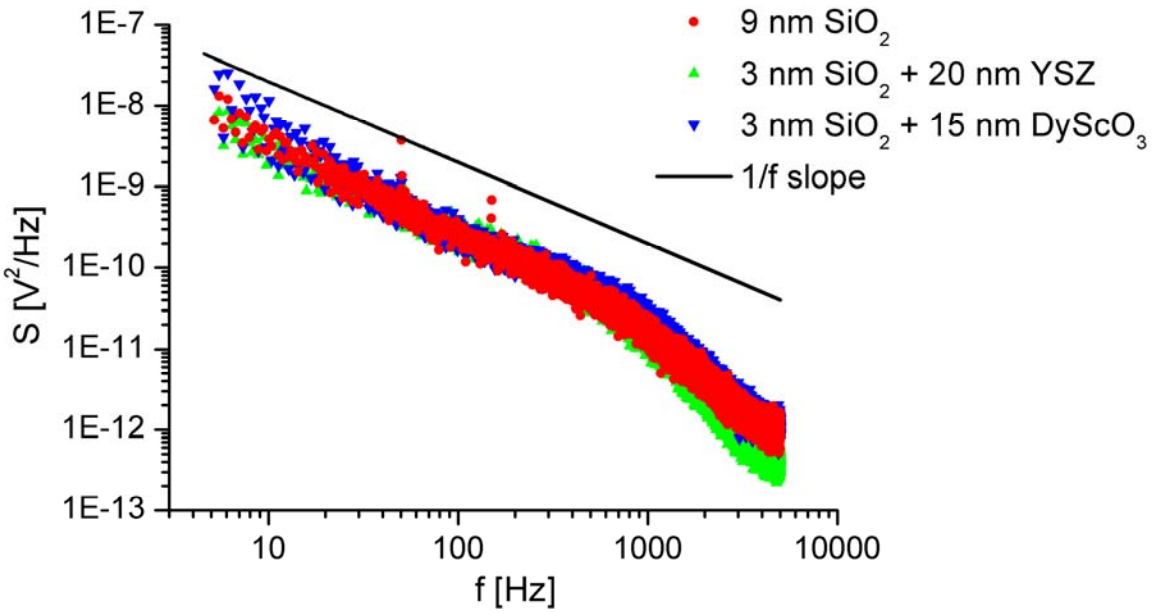


Figure 4.14: Noise power density spectra of YSZ (20 nm) and $DyScO_3$ (15 nm) ISFETs with a respectively 3 nm SiO_2 interlayer as gate dielectric. The spectrum of the standard 9 nm SiO_2 ISFET is added for reference. All ISFETs had gate widths of 25 µm. The underlying noise recordings were performed in the working point of the transconductance maximum for V_{DS} = -3V. The 1/f slope (black line) is given by $y(f) = f^{-1} + \text{const.}$

Gate dielectric	Gate capacitance [µF/cm²]	Average noise power density at 1000 Hz [10^{-12} V²/Hz]
9 nm SiO_2	0.38	17 ± 2
3 nm SiO_2 + 20 nm YSZ	0.63	14 ± 3
3 nm SiO_2 + 15 nm $DyScO_3$	0.69	22 ± 4

Table 4.7: The average noise power densities of the high-k dielectric ISFETs and the standard SiO_2 ISFET, which were extracted from the graphs in figure 4.14, do not scale with one over gate capacitance squared (C_{ox}^{-2}) as predicted by equation (2.19).

The black solid line in figure 4.14 corresponds to a 1/f slope. The approximate 1/f slopes of the spectra confirm the low frequency noise of the ISFETs to be the expected

1/f noise, which is caused by the statistical capture and emission of single inversion carriers in and from individual traps in the gate oxide. The strong decrease in noise beyond approximately 1000 Hz is due to the electronic amplifier set-up, which was optimised for low frequencies and acts as a low pass filter.

Figure 4.15 shows the transconductance curves of $DyScO_3$ ISFETs with identical gate dielectrics (15 nm $DyScO_3$ on top of a 3 nm SiO_2 interlayer), but varying gate widths W of 100, 50, 25 and 12 µm. The noise power density spectra of the same ISFETs are depicted in figure 4.16. The respective maximum transconductance (g_m) values, maximum g_m^{eff} values according to equation (4.1) and average noise power densities at 1000 Hz are listed in table 4.8.

The maximum g_m values do not precisely obey the proportionality between W and g_m, which is predicted by the long-channel FET equation (equation (2.12)). The g_m values only follow the trend of equation (2.12): Reducing the gate width by 50 % results in g_m reductions by 30 to 42 % (see table 4.8). Once more invalidity of the long-channel FET equation and high source and drain feed line resistances are assumed to account for the non-scaling between g_m and W. The g_m^{eff} values, which approximately would have been exhibited if the source feed line resistance was zero, exceed their corresponding g_m values and in addition improve the scaling with W: Reducing the gate width by 50 % results in g_m^{eff} reductions by 40 to 46 %. The better scaling of the larger g_m^{eff} values affirms the assumption that high feed line resistances cause the used ISFET devices to deviate from the theoretically expected behaviour.

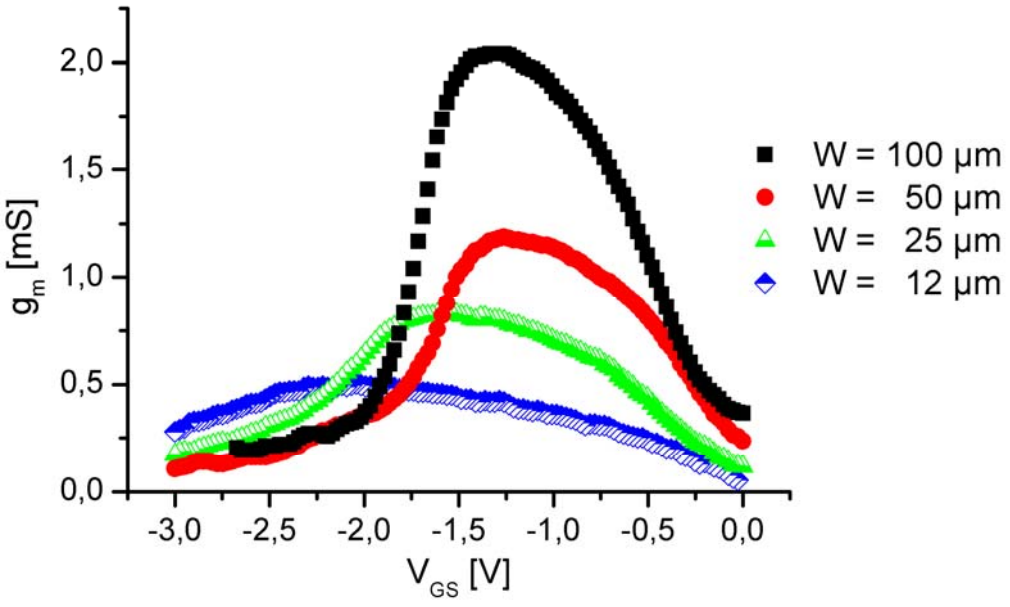


Figure 4.15: Transconductance curves of $DyScO_3$ ISFETs (15 nm on top of a 3 nm SiO_2 interlayer) with gate widths W of 100, 50, 25 and 12 µm. The underlying transfer characteristics were recorded at V_{DS} = -3V.

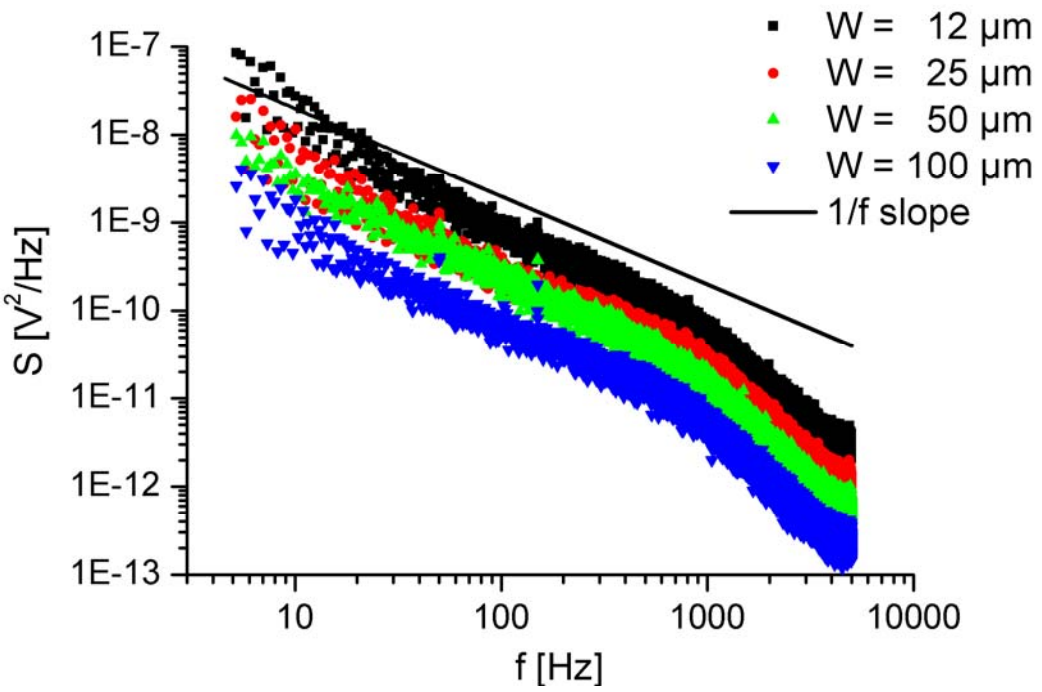


Figure 4.16: Noise power density spectra of $DyScO_3$ ISFETs (15 nm on top of a 3 nm SiO_2 interlayer) with gate widths W of 100, 50, 25 and 12 µm. The underlying noise recordings were performed in the working point of the transconductance maximum for V_{DS} = -3V. The 1/f slope (black line) is given by y (f) = f^{-1} + const.

Gate width [µm]	Maximum g_m [mS]	Maximum g_m^{eff} [mS]	Average noise power density at 1000 Hz [10^{-12} V^2/Hz]
100	2.04	3.44	5 ± 1
50	1.19	1.85	13 ± 3
25	0.83	1.11	22 ± 4
12	0.50	0.59	50 ± 11

Table 4.8: Characteristic properties of the $DyScO_3$ ISFETs (15 nm on top of a 3 nm SiO_2 interlayer) with gate widths W of 100, 50, 25 and 12 µm. The maximum g_m values were determined from the transconductance curves of figure 4.15. The average noise power densities were extracted from the graphs of figure 4.16. The g_m^{eff} values were calculated by equation (4.1).

The average noise power densities S_V at 1000 Hz obey the proportionality between W^{-1} and S_V (see table 4.8) predicted by equation (2.19): Doubling the gate width W yields within the RMS error halved noise levels. However, the noise level reduction with increasing gate width only leads to corresponding signal-to-noise ratio increases for signals, which are applied to the entire gate width. This is the case in biomolecule detection experiments. In cell-transistor coupling experiments, however, the recorded cell

controls only the gate region underneath its body. Therefore, the optimum gate width for cell-transistor coupling is not as large as possible as for biomolecule detection experiments, but defined by the dimension of the individual recorded cell.

4.3.2 Ion sensitivity

Figure 4.17 shows typical pH, pK and pNa sensitivity measurements of Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs. The pH, pK and pNa ranges covered by the measurement solutions were chosen in such a way that the physiological ion concentrations were contained therein (for details see chapter 2.3.2): The pH sensitivity was determined between 5 and 9, while the pK and pNa sensitivities were determined between 4 and 0. The pH, pK and pNa step between the respective measurement solutions was 1. First the measurements were performed from one extreme value of the ion concentration range to the other extreme value. Subsequently, the solutions were applied backwards to study the stability (hysteresis) of the ISFETs.

As seen in figure 4.17, the Al_2O_3, SiO_2 and $DyScO_3$ ISFETs exhibit very good stability in all ion sensitivity measurements. In general the same surface potential Ψ_s is reached as before, when a measurement solution is applied for the second time (minimum hysteresis).

By contrast, the YSZ ISFETs exhibit extraordinarily high drift in all measurements. Even if the first solution was applied until the signal had stabilised (see the YSZ pK and pNa sensitivity measurements), each solution change was followed by large drifts. As seen in the pK and pNa recordings, the respective drift rate is correlated to the ion sensitivity: The larger the preceding change in surface potential the faster is the subsequent drift. A specific characteristic of the drift after K^+ concentration changes is that the drift always occurs against the direction of the K^+ sensitivity signal. Since ISFET drift is generally assumed to result from the formation of a gel surface layer by the penetration of ions into the gate oxide (for details see chapter 2.2.4), the most probable reason for the higher drift rate and lower stability of the YSZ signals is a higher porosity of the YSZ films: Higher porosity would lead to faster and deeper ion penetration and accordingly faster and longer lasting drift.

Figure 4.18 shows the average surface potential changes of Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs upon pH, pK and pNa changes. Each data point constitutes the average of four independent measurements. The surface potential changes were extracted from measurements such as shown in figure 4.17 by subtracting the potential immediately after the solution exchange from the potential immediately before the exchange. This procedure was especially required for the YSZ ISFETs because of their large drift following solution exchanges.

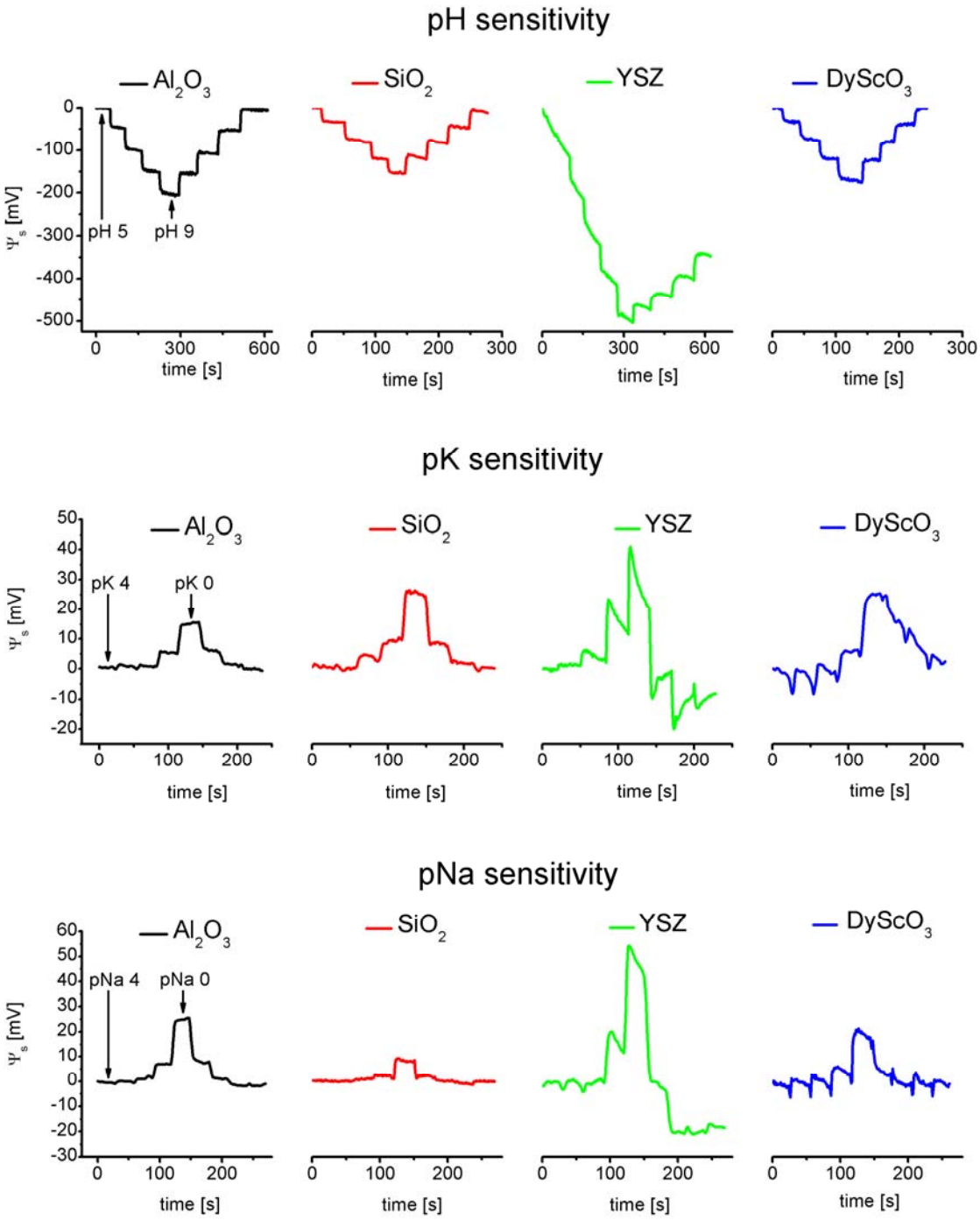


Figure 4.17: pH, pK and pNa sensitivity measurements of Al_2O_3 (black lines), SiO_2 (red lines), YSZ (green lines) and $DyScO_3$ (blue lines) ISFETs. The ion sensitivities were measured for the pH range between 5 and 9 and for the pK and the pNa ranges between 4 and 0. The pH, pK and pNa step between the successive measurement solutions was respectively 1. During all measurements of the same ion sensitivity, the solutions were applied in the same order. The arrows in the leftmost Al_2O_3 graphs indicate the signal of the maximum and minimum pH, pK and pNa solutions. The time intervals between the solution exchanges were kept constant during each measurement and vary between 30 and 60 seconds. The respective Ψ_s-axis of the Al_2O_3 graphs applies to all graphs in the same row.

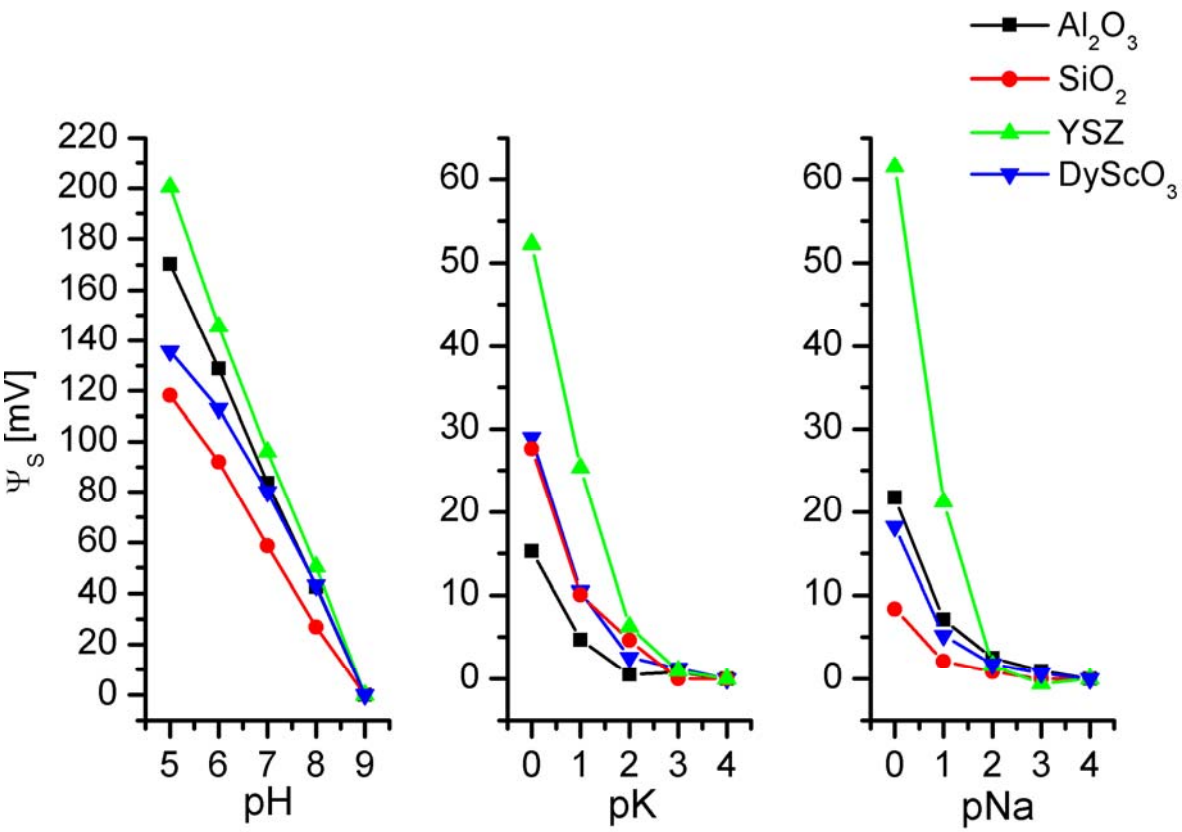


Figure 4.18: The pH, pK and pNa sensitivity of Al_2O_3 (black squares), SiO_2 (red circles), YSZ (green triangles pointing upwards) and $DyScO_3$ (blue triangles pointing downwards) ISFETs. All data points are average values of four independent measurements and were extracted from measurements such as shown in figure 4.17. The RMS errors of the data points in the pH sensitivity graph are smaller than 4 mV and in the pK and pNa sensitivity graphs smaller than 1.7 mV, i.e. smaller than the respective symbol. The legend to the top right applies to all three graphs.

The graphs in figure 4.18 show that the surface potential rises for all four ISFETs with increasing H_3O^+, K^+ and Na^+ concentrations as expected by the respective positive ion charge. The pH sensitivity of all ISFETs was independent from the electrolyte pH as seen by the basically constant slopes in the corresponding graph. The relatively moderate deviations in the pH sensitivity between ISFETs with different gate dielectric are caused by differences in the properties, which determine the intrinsic pH sensitivity of oxides (for details see chapter 2.2.3): Either Al_2O_3, SiO_2, YSZ and $DyScO_3$ have different reaction site densities on their surfaces (terminating oxygen atoms) or the dissociation constants of the base and acid reaction of their reaction sites differ or both.

In contrast to the pH sensitivtiy, the pK and pNa sensitivities of all ISFETs greatly increase with increasing K^+ and Na^+ concentrations (see the corresponding graphs in figure 4.18). This behaviour is well known from the literature [Abe et al., 1979; Bergveld, 1996; Schöning et al., 1996]. However, to my knowledge, no theory explaining this particular behaviour has been published.

The YSZ ISFETs exhibit by far the highest pK and pNa sensitivity, while the lower pK and pNa sensitivities of the Al_2O_3, SiO_2, and $DyScO_3$ ISFETs differ rather moderately from each other. As described in chapter 2.2.3, the K^+ and Na^+ sensitivity of oxides is a secondary counter ion effect, which is based on the pH sensitivity: K^+ and Na^+ ions bind to negatively charged O^- surface groups, whose density is determined by the pH sensitivity of the respective oxide. Therefore, the observed differences in the pK and pNa sensitivity between the Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs are caused firstly by the same oxide properties, which determine the pH sensitivity: the density of oxygen surface atoms and the dissociation constants of the pH sensitivity reactions. Furthermore, the adsorption affinity of K^+ and Na^+ ions to the respective oxide may account for the pK and pNa sensitivity differences.

Table 4.9 compares the measured pH sensitivities with the literature values for the Al_2O_3, SiO_2 and YSZ ISFETs. While the SiO_2 and YSZ ISFET results show good agreement with the literature, the measured Al_2O_3 pH sensitivity deviates with 43 mV/pH significantly from the widely reported Nernstian behaviour of 54 to 56 mV/pH. The gate dielectric of the Al_2O_3 ISFETs used for the ion sensitivity measurements consisted of an only 5 nm thick Al_2O_3 film on top of a 3 nm SiO_2 interlayer. However, as shown in chapter 4.1.3, 10 nm thick films are required for dense PLD deposited Al_2O_3 films. It is therefore assumed, that the lower pH sensitivity is caused by incomplete Al_2O_3 coverage and contributions of SiO_2 surface parts of generally lower pH sensitivity.

Gate material	pH sensitivity (experiment) [mV/pH]	pH sensitivity (literature value) [mV/pH]
Al_2O_3	43	54 – 56 [Schöning et al., 1996] [Vlasov et al., 2003]
SiO_2	30	30 – 40 [Bergveld, 1996] [Fung et al., 1986] [Vlasov et al., 2003]
YSZ	50	55 [Vlasov et al., 2003]
$DyScO_3$	34	-

Table 4.9: Comparison of experimental and literature pH sensitivities of Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs. The experimental sensitivities are taken from figure 4.18. The YSZ literature value originates from a pure ZrO_2 ISFET.

Table 4.10 and 4.11 compare the experimental and literature pK and pNa sensitivities of Al_2O_3 and SiO_2 ISFETs (no literature values are available for YSZ and $DyScO_3$ ISFETs). Quite remarkable is the large range of the sensitivities reported in the

literature. The maximum range constitutes the Al_2O_3 pNa sensitivity from pNa 1 to pNa 0, which varies from 4 mV to 18 mV. Similarly large deviations occur between the experimental and literature sensitivities in parts of the SiO_2 data. These sensitivity ranges probably originate from one of the following three reasons: (i) Different techniques in oxide preparation may result in different degrees of impurities, which change the number of surface reaction sites and accordingly the ion sensitivity. (ii) Variations in the number of reaction sites (negatively charged O^- groups) may also be caused by different background pH values of the measurement solutions. (iii) Finally, as described in chapter 3.5.3, the ionic strength of all solutions used in the pK and pNa sensitivity measurement of this thesis was kept constant. Since the cited literature does not comment on this topic, it is likely that constant ionic strength was not taken care for. Differences in the ionic strength between the measurement solutions lead to changes in the Helmholtz capacitance, which may change the ion sensitivities (for details see chapter 2.2.3).

	pK sensitivity of Al_2O_3 [mV/pK]		pK sensitivity of SiO_2 [mV/pK]	
pK step	experiment	literature value	experiment	literature value
pK 4 → pK 3	0	0	0	-
pK 3 → pK 2	0	0	4	4
pK 2 → pK 1	4	0	6	19
pK 1 → pK 0	10.5	4 – 12	18	21

Table 4.10: Comparison of experimental and literature pK sensitivities of Al_2O_3 and SiO_2 ISFETs. The experimental sensitivities are taken from figure 4.18. The literature values were reported by [Abe et al., 1979] and [Schöning et al., 1996].

	pNa sensitivity of Al_2O_3 [mV/pNa]		pNa sensitivity of SiO_2 [mV/pNa]	
pNa step	experiment	literature value	experiment	literature value
pNa 4 → pNa 3	0	0	0	0 – 2
pNa 3 → pNa 2	0	0	0	0 – 2
pNa 2 → pNa 1	5	0	2	8
pNa 1 → pNa 0	15	4 – 18	6	17 – 22

Table 4.11: Comparison of experimental and literature pNa sensitivities of Al_2O_3 and SiO_2 ISFETs. The experimental sensitivities are taken from figure 4.18. The literature values were reported by [Abe et al., 1979], [Bergveld et al., 1996] and [Schöning et al., 1996].

4.3.3 Drift

Figure 4.19 depicts the long-term drift of the Al_2O_3, SiO_2, YSZ and $DyScO_3$ ISFETs. All measurements were started immediately after the exposure of the respective gate dielectric to the electrolyte. All curves are fitted very well by first order exponential decays of the form

$$V_T = \Delta V_T \cdot e^{\frac{-t}{\tau}} + const\,, \tag{4.2}$$

where V_T is the ISFET threshold voltage, τ is the characteristic time of the decay and ΔV_T is the total drift in the threshold voltage until saturation is reached. To keep figure 4.19 concise, only the YSZ and $DyScO_3$ fits are included. The fit parameters τ and ΔV_T of all four measurements are listed in table 4.12.

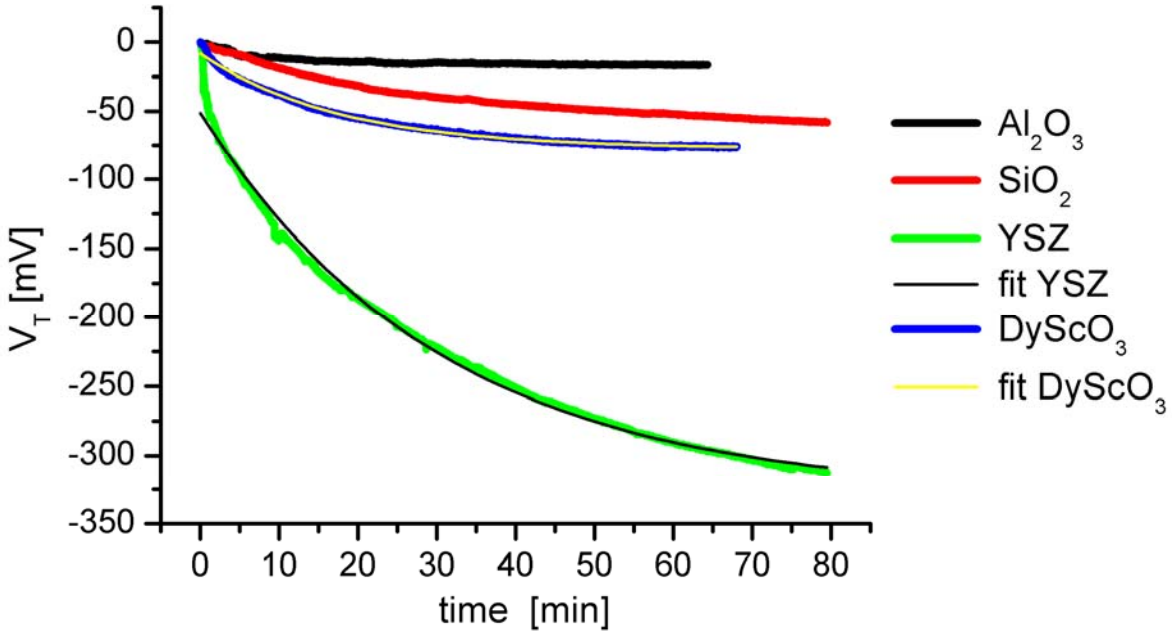


Figure 4.19: Long-term drift measurements of Al_2O_3 (thick black line), SiO_2 (thick red line), YSZ (thick green line) and $DyScO_3$ (thick blue line) ISFETs. The thin black and yellow line constitute the first order exponential decay fits to the YSZ and $DyScO_3$ data, respectively.

Gate material	τ [min]	ΔV_T [mV]
Al_2O_3	8	16
SiO_2	28	60
YSZ	30	329
$DyScO_3$	18	77

Table 4.12: The parameters of the first order exponential decay fits, which were performed on the drift measurements of figure 4.19: The characteristic time τ and the total drift ΔV_T.

As seen by the graphs in figure 4.19 and by the ΔV_T values of table 4.12, the YSZ dielectric exhibits by far the largest total drift with 329 mV. The SiO_2 and $DyScO_3$ total drifts of 60 and 77 mV, respectively, are on the same order of magnitude, while the Al_2O_3 ISFET drifts by only 16 mV. Although the total drift ΔV_T of the SiO_2 ISFET is much smaller than that of the YSZ ISFET, their τ values of 28 and 30 minutes, respectively, are on the same order of magnitude. The $DyScO_3$ ISFET exhibits a medium τ value of 18 minutes, while the τ value of the Al_2O_3 ISFET is only 8 minutes.

Generally the ISFET long-term drift is attributed to the penetration of electrolyte ions into the gate oxide (for details see chapter 2.2.4). The total number of penetrating ions and the duration of the penetration process, which define the drift parameters ΔV_T and τ, are determined by the porosity of the respective gate oxide. Therefore, it is assumed that the very large drift of the YSZ ISFETs is caused by high porosity of the YSZ gate dielectric, while the small drift of the Al_2O_3 ISFETs indicate considerably lower porosity for the Al_2O_3 dielectric films. The moderate drifts of the SiO_2 and $DyScO_3$ ISFETs are attributed to intermediate porosity of the SiO_2 and $DyScO_3$ films compared with the YSZ and Al_2O_3 films.

The characteristic time τ of the exponential decay constitutes a measure for the time until the respective ISFET reaches the saturation regime. Since the noise level during biomolecule detection experiments is determined by the ISFET drift, these experiments are not performed until the drift has saturated. Consequently, Al_2O_3 ISFETs offer in comparison with the YSZ, $DyScO_3$ and standard SiO_2 ISFETs the advantage of reducing the time to be waited before the biomolecule detection experiments can start from several hours to several tens of minutes.

4.4 Bioelectronic coupling

4.4.1 Oxide silanisation for biomolecule detection experiments

Table 4.13 lists the contact angles of SiO_2, Al_2O_3, YSZ and $DyScO_3$ films with deionised water after O_2 plasma treatment and after gas-phase silanisation with APTES. For all dielectrics, the contact angles after the plasma treatment are much lower than after the silanisation leading to the following conlusions: Firstly, the low contact angles after the plasma treatment (hydrophilicity) indicate that this treatment constitutes an excellent oxide cleaning method, which leaves behind hydrophilic surfaces terminating with OH and O^- groups. Since the oxygen surface atoms are responsible for the hydrophilicity, the significantly larger YSZ and $DyScO_3$ contact angles in comparison with SiO_2 may be due to an intrinsically lower density of oxygen atoms on the YSZ and $DyScO_3$ surfaces. Secondly, from the large contact angles after the silanisation (hydrophobicity), it is

concluded that the surface silanisation, which is a prerequisite for the polyelectrolyte and DNA detection experiments, was successfully performed on all oxides.

Gate dielectric	Contact angle after O_2 plasma treatment [°]	Contact angle after APTES silanisation [°]
SiO_2	4	59
Al_2O_3	12	58
YSZ	17	54
$DyScO_3$	18	53

Table 4.13: Contact angles of SiO_2, Al_2O_3, YSZ and $DyScO_3$ films with deionised water after O_2 plasma treatment and after gas-phase silanisation with APTES.

4.4.2 Polyeletrolyte detection

Figure 4.20 shows the recording of a polyelectrolye detection experiment with an Al_2O_3 ISFET. As indicated by the black and red bars, the ISFET was alternately exposed to PSS and PAH solution for 12 minutes. During the also 12 minutes long time intervals between the polyelectrolyte solution applications, buffer solution was applied in order to flush away all of the previously applied excess polyelectrolyte. The sharp, up to 30 mV high peaks, which occur all 6 minutes, are caused by the respective solution exchange.

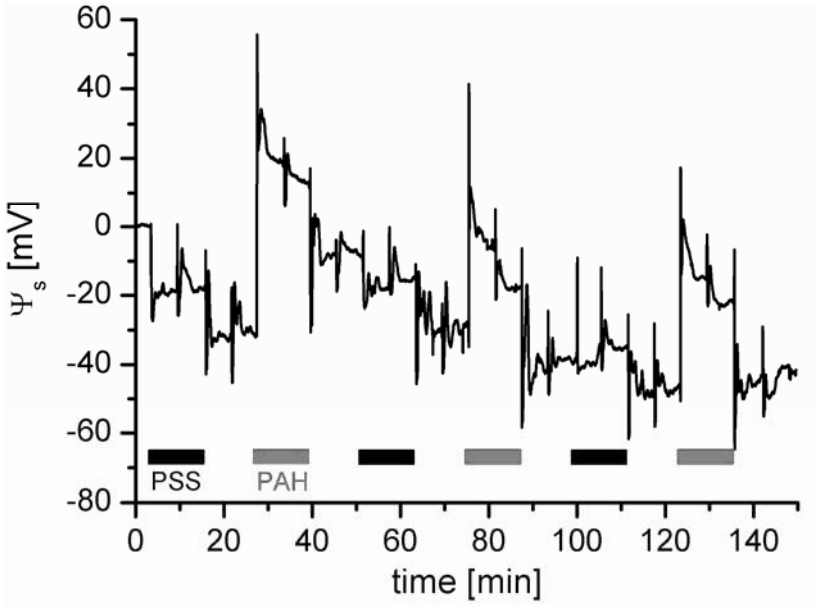


Figure 4.20: Polyelectrolyte detection experiment with an Al_2O_3 ISFET: The black and red bars indicate the time intervals, during which the ISFET was exposed to PSS and PAH solution, respectively. During the intermediate intervals, buffer solution was applied.

In the analysis, the equilibrium buffer signals were extracted as measurement signal for the previously applied polyelectrolyte. Although before the beginning of the actual experiment, the ISFET was exposed to buffer solution until the long-term drift had saturated, the polyelectrolyte measurement signals exhibited an exponentially decaying drift.

The bar diagrams of figure 4.21 show PSS and PAH measurement signals of Al_2O_3 and $DyScO_3$ ISFETs, which were extracted from alternate PSS and PAH layer deposition recordings such as depicted in figure 4.20. The exponentially decaying drifts observed in the original recordings were compensated by subtracting the according fits from the extracted measurement signals. The Al_2O_3 diagram contains the signals of 3 PSS and 3 PAH layers, the $DyScO_3$ diagram the signals of 3 PSS and 2 PAH layers.

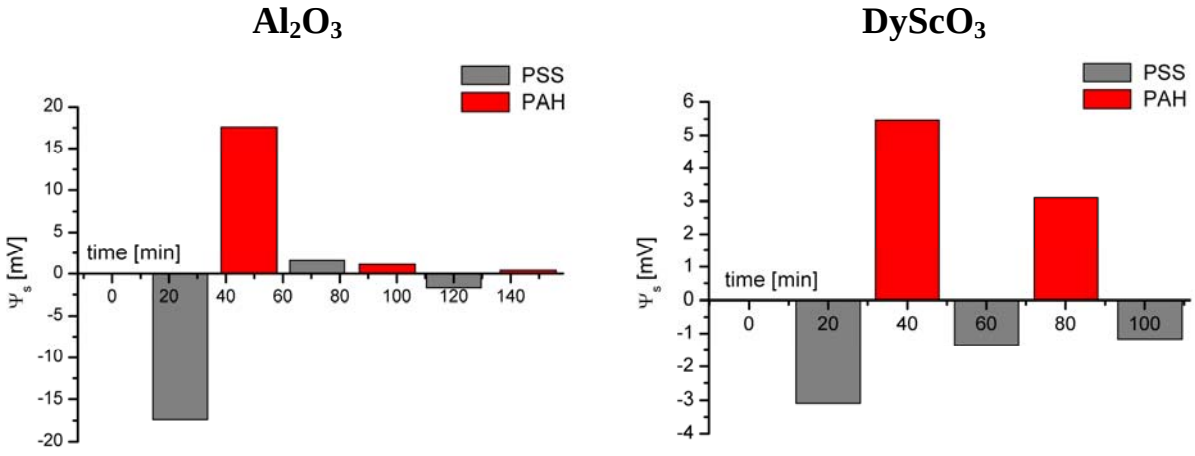


Figure 4.21: Bar diagrams of PSS (grey) and PAH (red) measurement signals of Al_2O_3 and $DyScO_3$ ISFETs, which were extracted from alternate PSS and PAH layer deposition experiments.

The PSS and PAH signals of both the Al_2O_3 and $DyScO_3$ ISFETs resemble the signals reported from SiO_2 ISFET measurements [Uslu et al., 2004]: According to their intrinsic charge, the negatively charged PSS layers exhibit negative signals, while the positively charged PAH layers exhibit positive signals. The peak to peak signal amplitudes of the first PSS and PAH layers are in both the Al_2O_3 and the $DyScO_3$ measurement within the 5 to 15 mV range reported for SiO_2 ISFETs. The signal amplitudes decline with increasing number of the deposited polyelectrolyte layers, i.e. with increasing distance of the adsorbed polyelectrolyte layers from the inversion channel of the ISFET. The only qualitative difference in comparison with the reported SiO_2 measurements is that in the Al_2O_3 measurement the polyelectrolyte layers following the first deposited layers do not decline gradually with increasing layer number, but yield no significant signal.

In conclusion, although only few polyelectroyte detection experiments with Al_2O_3 and $DyScO_3$ ISFETs have been performed, the obtained results reproduce the key features

reported in the literature for identical SiO_2 ISFET measurements. Therefore, both Al_2O_3 and $DyScO_3$ ISFETs seem to be well suited for biomolecule detection experiments.

4.4.3 DNA detection

Figure 4.22 shows the differential Al_2O_3 ISFET recording of a DNA detection experiment: First buffer solution was applied until the long-term drift had saturated. Subsequently, as indicated by the according arrow, the buffer solution was exchanged for the target DNA solution. The negative signal, which appears after the application of the target DNA solution, is attributed to the hybridisation reaction between the target DNA and the immobilised perfect match probe DNA. The hybridisation reaction was given 10 minutes to complete, after which the DNA solution was exchanged for buffer solution as indicated by the second arrow. Since the application of the buffer solution does not cancel the hybridisation, the DNA hybridisation signal remains after the solution exchange.

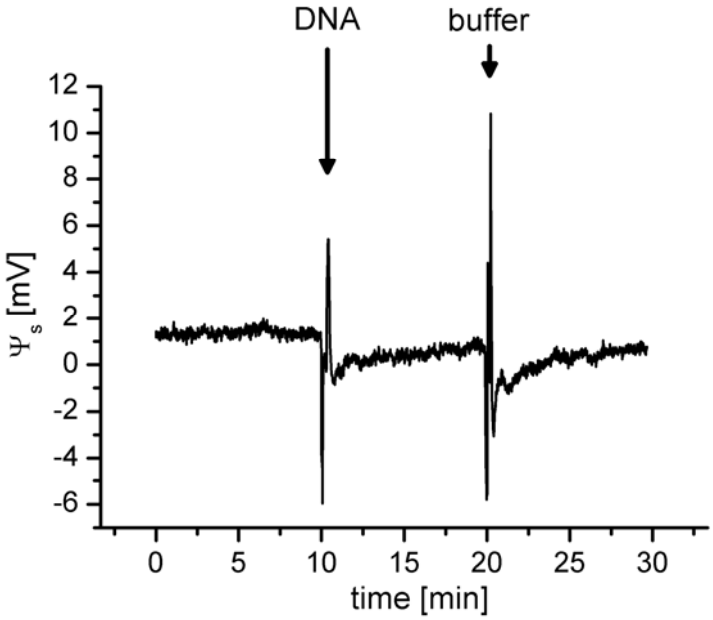


Figure 4.22: Differential Al_2O_3 ISFET recording of a DNA detection experiment: First buffer solution was applied until the long-term drift had saturated. Subsequently, as indicated by the arrows, DNA target solution was applied for 10 minutes, which then was exchanged for buffer solution.

Only few DNA detection experiments with high-k dielectric ISFETs have been performed and the Al_2O_3 ISFET recording shown in figure 4.22 has the character of preliminary results. However, since already the first experiments yielded small hybridisation signals, Al_2O_3 ISFETs seem to be well suited for DNA detection. Optimisation of the experimental protocol should facilitate hybridisation signals of several mV as achieved routinely in our group for experiments with SiO_2 ISFETs [Han et al., 2006b].

4.4.4 Biocompatibility

Figure 4.23 depicts differential interference contrast (DIC) (Axiotech 100 Vario with water immersion objective, Zeiss AG) micrographs of embryonic rat cortical neurons, which were cultured for 10 to 11 days on poly(L)lysine-coated SiO_2, Al_2O_3, YSZ, $DyScO_3$, $LaAlO_3$ and $GdScO_3$ surfaces. In all micrographs, the neurons do not form clusters, the cell morphology looks normal, neurites have grown and neurites of different cells join each other. Since primary mammalian neurons are generally known to be sensitive to minute changes in the culture conditions, it is concluded that all dielectrics are biocompatible and may be used as interface in the cell-transistor coupling. Furthermore, in identically performed neuron culture experiments (images not shown), also CeO_2 and $LaScO_3$ have proven biocompatibility.

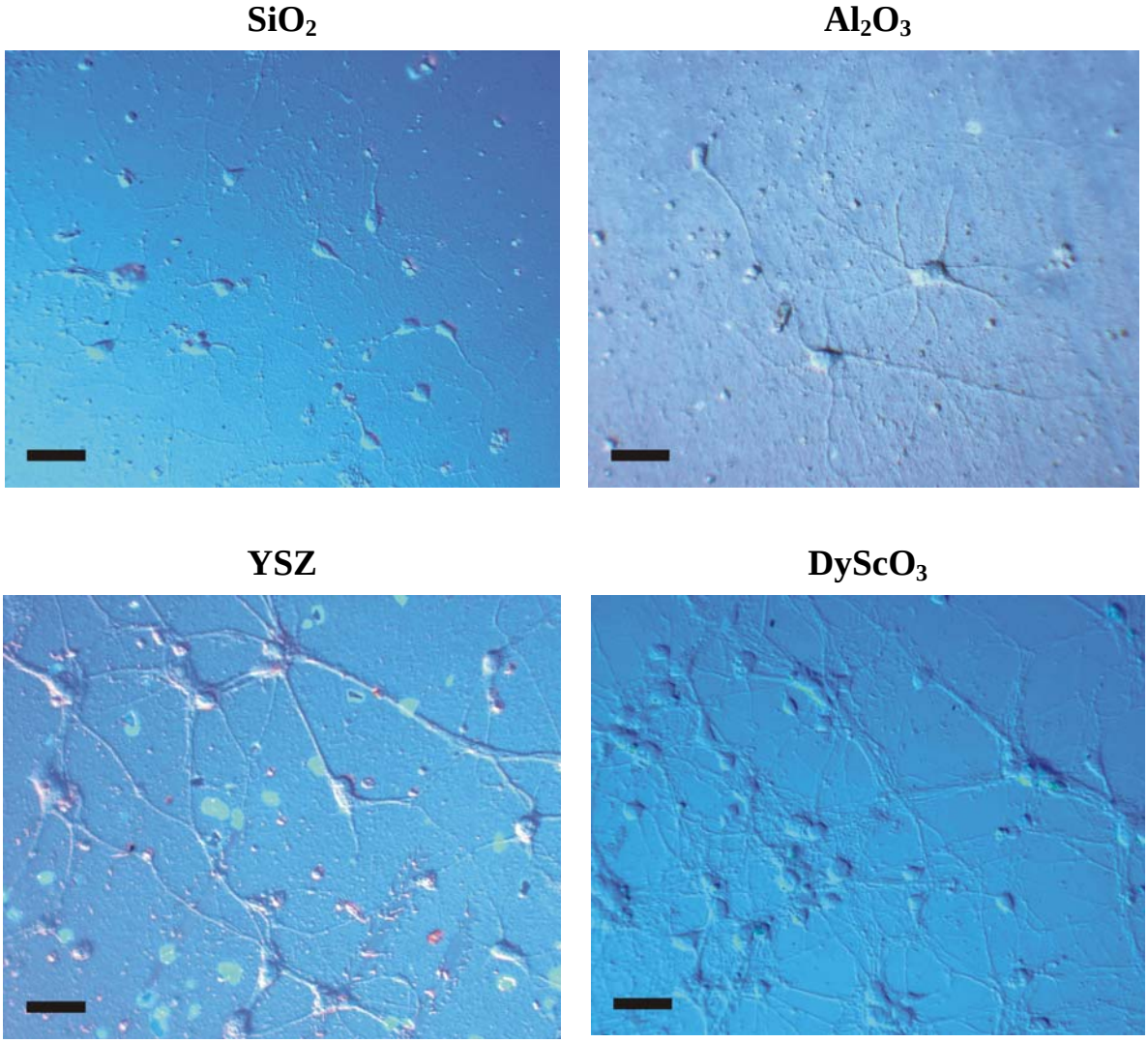
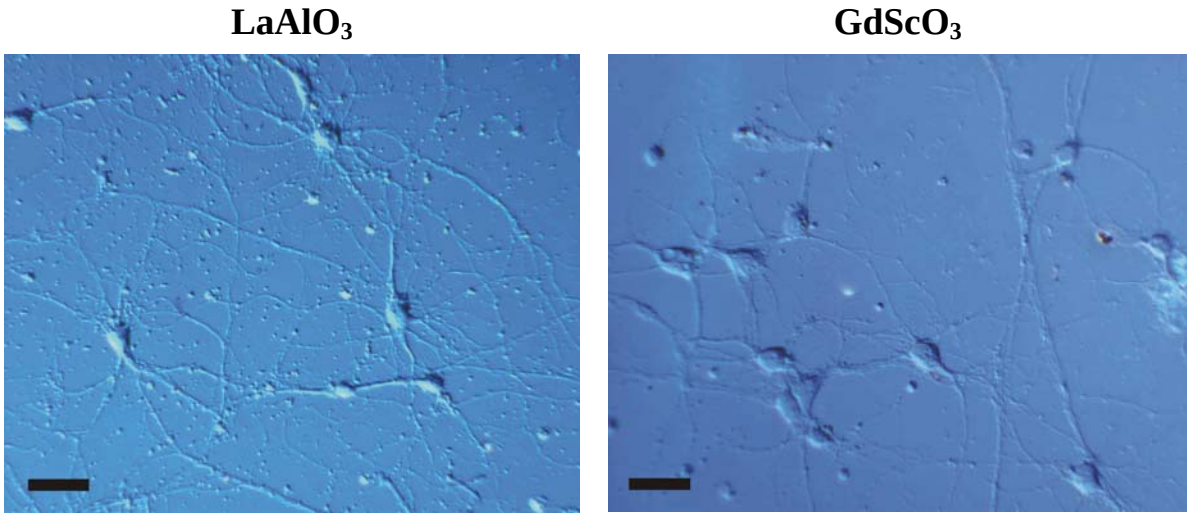


Figure 4.23: DIC micrographs of embryonic rat cortical neurons, which were cultured for 10 to 11 days on poly(L)lysine-coated SiO_2, Al_2O_3, YSZ, $DyScO_3$, $LaAlO_3$ and $GdScO_3$ surfaces (see also the top of next page). All dielectric films were 70 to 100 nm thick and produced on silicon substrates. All scale bars correspond to 40 µm.



4.4.5 Cell-transistor coupling with the cardiomyocyte cell line HL-1

Figure 4.24 shows recordings of cell-transistor coupling between the cardiomyocyte cell line HL-1 and YSZ and $DyScO_3$ high-k material and standard SiO_2 ISFETs. All signals were recorded from dense layers of HL-1 cells covering the chip surface. The cell layers optimally sealed the gates from the bath electrolyte providing a low junction conductance G_J and accordingly strong coupling between cell and ISFET (see equation (2.42)). The APs were exhibited spontaneously at an approximately constant frequency. The AP frequency in the depicted recordings ranged from 0.4 to 1.4 Hz.

Figure 4.25 depicts recordings of SiO_2, YSZ and $DyScO_3$ ISFETs from HL-1 APs, which were averaged to reveal all their details. The number of averaged APs is 17 for the SiO_2, 28 for the YSZ and 15 for the $DyScO_3$ recording. In each graph, all underlying APs were recorded from the same cell. At approximately 150 ms, the SiO_2 and the YSZ AP show a large maximum in the junction voltage V_J, which originates from the depolarisation of the recorded cell by the slightly earlier AP in neighbouring cells (for details see chapter 3.7.2). By contrast, the $DyScO_3$ AP exhibits only a very weak depolarisation signal at approximately 140 ms. The probable reason for this small depolarisation signal, which is only visible in the averaged AP and hidden in the noise of the original recording (compare the $DyScO_3$ recordings of Figure 4.24 and Figure 4.25), is a relatively slow depolarisation of the recorded cell: Since not until after the depolarisation ion channels open and ions flow through the cell membrane, the depolarisation itself couples to the ISFET purely capacitively via the attached membrane. Capacitive signal transduction, however, requires fast signals, because the absolute impedance value of a capacitance C is given by $(\omega C)^{-1}$, where ω is the signal frequency and proportional to the signal velocity. Varying depolarisation velocities between different cell samples are variations typical to all complex biological systems.

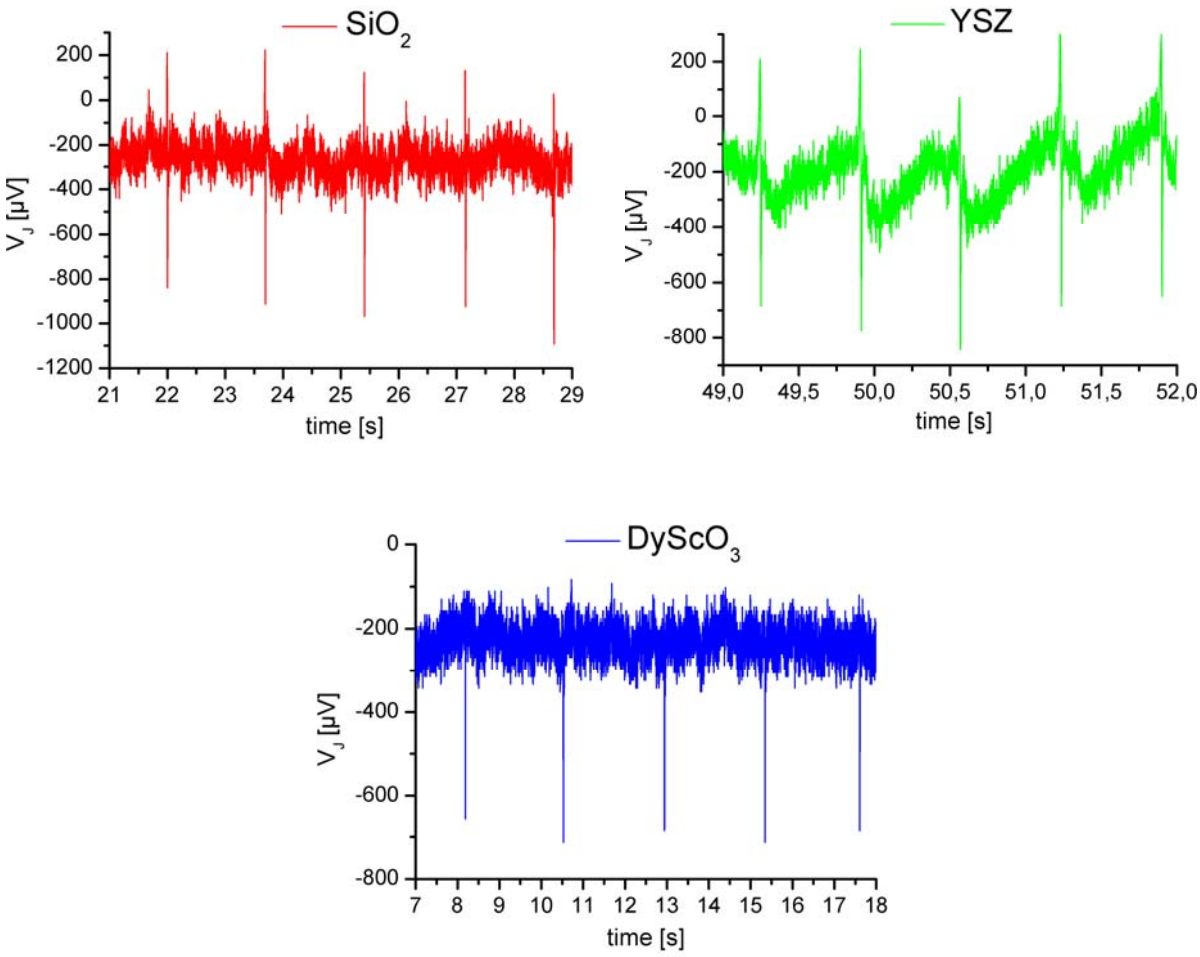


Figure 4.24: Recordings of cell-transistor coupling between the cardiomyocyte cell line HL-1 and YSZ and $DyScO_3$ high-k material and standard SiO_2 ISFETs.

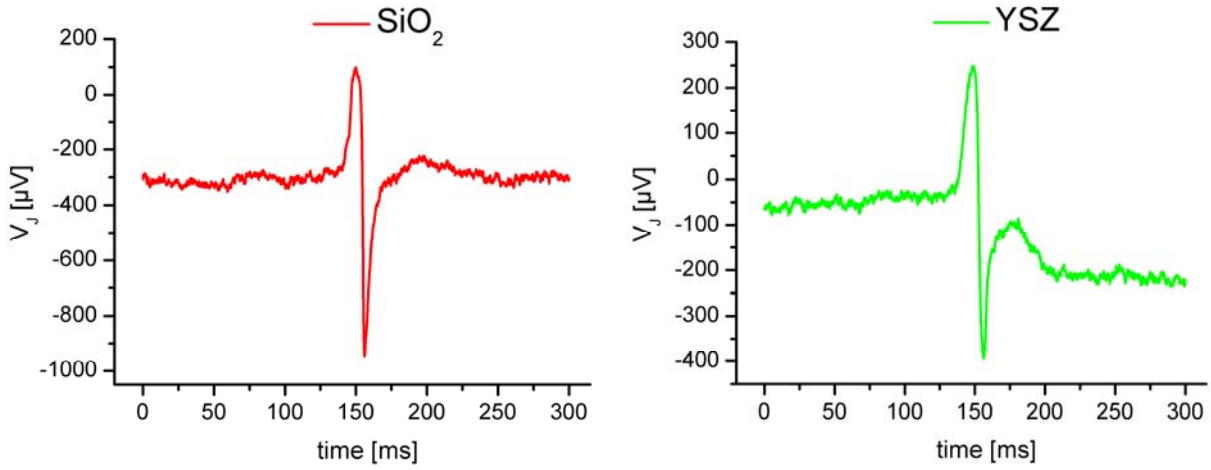
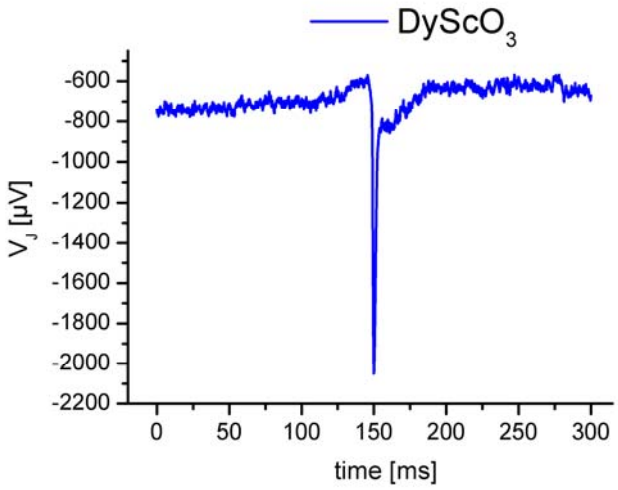


Figure 4.25: Averaged HL-1 APs recorded by SiO_2 (n = 17), YSZ (n = 28) and $DyScO_3$ (n = 15) ISFETs (see also the top of next page). In each graph, all averaged APs were recorded from the same cell. In the YSZ recording, the steady-state signal after the AP is different than before the AP, because the complete drift after the AP (see Figure 4.24) is much slower than the AP itself.



The large minimum in V_J in all recordings of Figure 4.25 directly following the depolarisation is caused by opening of voltage-gated Na^+ channels and subsequent drain of Na^+ ions from the cleft between cell and gate into the cytosol. The Na^+ V_J minimum constitutes a very sharp peak, because the time of the involved Na^+ channels in the open state is on the order of only few milliseconds. The subsequent slow further rise in V_J (in the SiO_2 and $DyScO_3$ recording back to the resting potential) is caused by the influx of K^+ ions through the gradually and late opening voltage-gated K^+ channels. The in chapter 3.7.2 described Ca^{2+} current, which keeps typical human cardiomyocytes depolarised for approximately 200 ms [Schrader, 2001], is not visible in any of the recordings. This may be caused by a lack of Ca^{2+} current or equal K^+ and Ca^{2+} currents with similar kinetic, which compensate each other.

While the shape of the HL-1 APs recorded by the SiO_2 and $DyscO_3$ ISFETs are basically the same, the YSZ signal shape deviates significantly: The K^+ current does not bring V_J straight back to the steady-state signal of before the depolarisation, but a strong drift against the direction of the K^+ current signal occurs. This behaviour resembles the large drift against the direction of K^+ signals observed in the YSZ K^+ sensitivity measurements (see figure 4.17). Furthermore, as described in chapter 2.3.3, the current model of cell-transistor coupling believes the ion sensitivity of the gate oxides to account for the slow signal components. It is therefore assumed, that the drift in the YSZ AP originates from the intrinsic property of the YSZ gate dielectric to exhibit a strong drift against the direction of signals caused by K^+ concentrations changes.

Alternatively, a much higher ion sensitivity of the YSZ ISFETs to Ca^{2+} in comparison with the SiO_2 and $DyScO_3$ ISFETs could explain the shape of the YSZ recording. However, this assumption is rather unlikely: The site-binding theory, which is the accepted theory for the description of the ISFET ion sensitivity (see chapter 2.2.3), states that cation sensitivities are based on the adsorption of the respective cation onto monovalent, negatively charged O^- sites of the oxide surface. Since monovalent charges

are not neutralised by divalent cations such as Ca^{2+}, ISFETs without the implementation of an ion-selective membrane as top gate layer, are basically insensitive to divalent cations [Bergveld and Sibbald, 1988]. Hence, a high Ca^{2+} sensitivity of the YSZ ISFET would be very surprising. However, the corresponding sensitivity measurements have not been performed.

4.4.6 Cell-transistor coupling with the HEK 293 cell line

Figure 4.26 shows the DIC micrograph of a YSZ ISFET chip surface during a typical cell-transistor coupling experiments with HEK 293 cells: The entire surface is covered by a dense layer of spherical HEK 293 cell bodies. The cell layer strongly seals the gates from the bath electrolyte, which is a prerequisite of strong coupling between cell and ISFET (see equation (2.42)). The arrows indicate the blurry image of the unfocussed patch pipet and the 25 µm wide gate used for the recording. Since the HEK 293 cells exhibit no spontaneous electrical activity, the patch pipet is attached to the cell on top of the gate in order to stimulate intracellularly (voltage clamp whole-cell mode) K^+ channel opening and closing by voltage pulses.

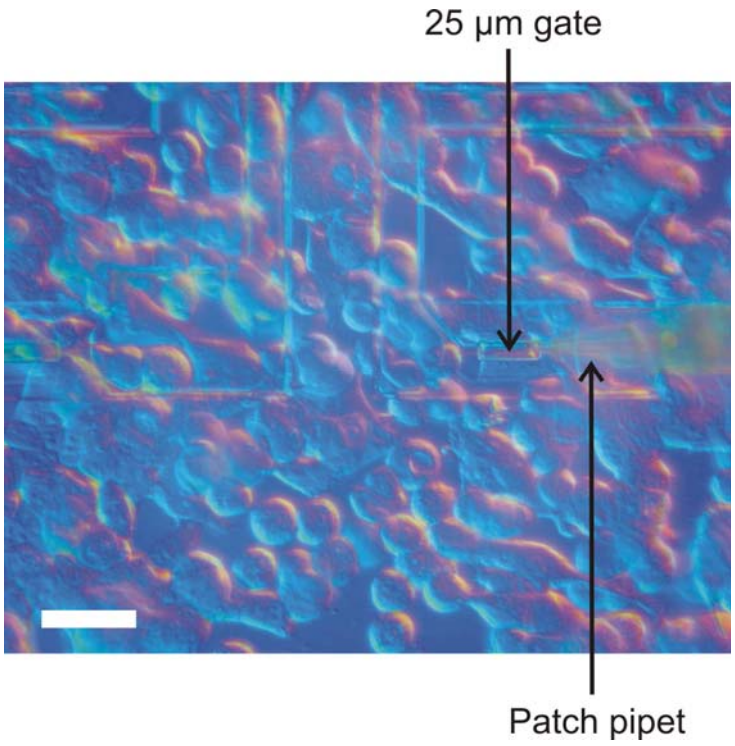


Figure 4.26: DIC micrograph of a YSZ ISFET chip surface during cell-transistor coupling with HEK 293 cells. The entire surface is covered by a dense layer of spherical HEK 293 cell bodies, which have diameters on the order of 15 to 30 µm. The arrows indicate the blurry image of the unfocussed patch pipet and the 25 µm wide gate used for the recording. The white scale bar corresponds to 40 µm.

Figure 4.27 shows averaged recordings of stimulated cell-transistor coupling between HEK 293 cells and high-k dielectric YSZ and standard SiO_2 ISFETs. Furthermore, also the averaged corresponding K^+ membrane currents I_{mem} (black traces), which were measured simultaneously by the voltage clamp pipet, are inserted into the graphs.

The time course of both I_{mem} signals is very similar and meets the expectations from the literature [Wrobel et al., 2005]: Upon the onset of the stimulation pulse, a sharp, approximately 0.3 ms lasting capacitive peak occurs because of charging and discharging of the membrane capacitance. Subsequently, I_{mem} rises due to gradual opening of the voltage-gated K^+ channel until the saturation current is reached after several 100 ms (note that the SiO_2 stimulation pulse is almost twice as long as the YSZ pulse for these selected recordings). After termination of the stimulation pulse, I_{mem} exhibits another capacitive peak and returns instantaneously to zero due to K^+ channel closing.

In further agreement with [Wrobel et al., 2005], the time course of the junction potential V_J measured by the SiO_2 ISFET follows closely the course of the corresponding I_{mem}: Upon the onset of the stimulation pulse, V_J also exhibits a capacitive peak, which is caused by charging and discharging of the membrane and the gate capacitance. During the pulse, V_J increases with the same kinetics as I_{mem}, because the K^+ influx into the cleft between cell and gate builds up a potential. After termination of the K^+ influx, i.e. after the return of I_{mem} to zero, the corresponding potential breaks down and V_J drops sharply. The only minor qualitative deviation of V_J from I_{mem} in the SiO_2 ISFET recording is an additional slow signal component during the return to the resting steady-state signal of before the stimulation. This deviation is attributed to the ion-sensitivity of the SiO_2 gate, which is assumed to generate a slow signal component on the order of tens of milliseconds [Brittinger and Fromherz, 2005; Wrobel et al., 2005].

By contrast, the course of the YSZ ISFET recording deviates strongly from the course of the corresponding membrane current: After a capacitive stimulation peak and strong rise in V_J due to the influx of K^+ ion into the cleft, V_J exhibits a strong drift against the direction of the K^+ signal. This behaviour resembles the drifts against the direction of K^+ signals observed in the YSZ ISFET recordings of HL-1 cell APs (see Figure 4.25) and in the YSZ K^+ sensitivity measurements (see figure 4.17). As described in chapter 2.3.3, the ion sensitivity of the gate oxides is believed to account for the slow signal components in cell-transistor coupling. Hence, it is assumed, that the drift in the YSZ ISFET recording originates from the intrinsic property of the YSZ gate dielectric to exhibit a strong drift against the direction of signals caused by K^+ concentrations changes.

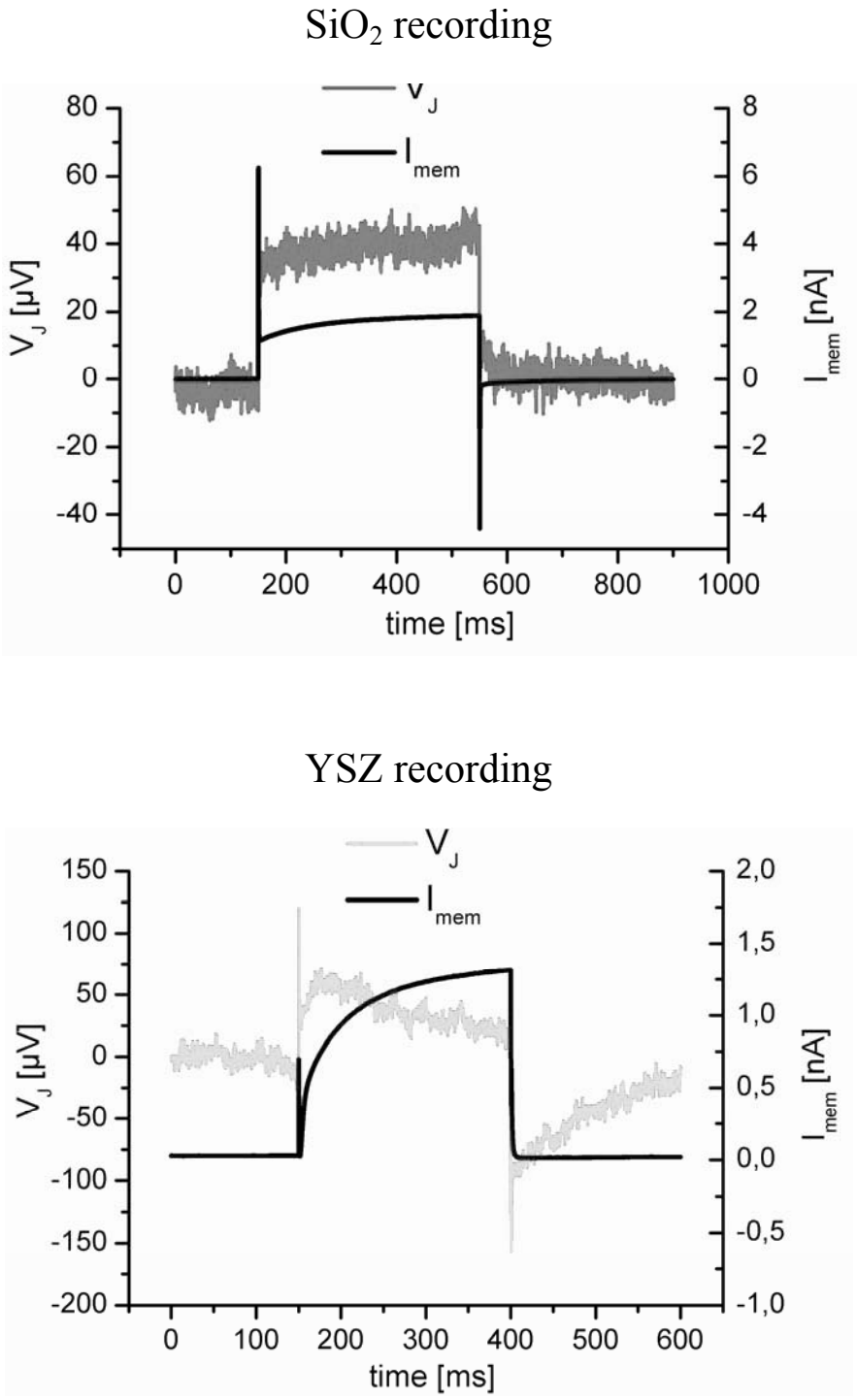


Figure 4.27: Averaged recordings of stimulated cell-transistor coupling between HEK 293 cells, which contained a voltage-gated K^+ channel due to stable transfection, and standard SiO_2 (red trace in the upper graph, n = 50) and YSZ (green trace in the lower graph, n = 150) ISFETs. The voltage-clamp stimulation pulse in the YSZ recording raised the membrane voltage from -60 to +80 mV and lasted 250 ms, while the SiO_2 stimulation pulse raised the membrane voltage from -20 to +100 mV and lasted 400 ms. The black traces in both graphs constitute the respective averaged membrane currents, which were simultaneously recorded by the voltage-clamp pipet.

5 Conclusions and Outlook

In the first part of this thesis, all properties of selected high-k dielectric and ultrathin SiO_2 and Si-O-N films, which are relevant for the employment as bioelectronic interface in ISFETs, were studied:

(i) By culturing primary embryonic rat neurons on the dielectrics, the materials SiO_2, Al_2O_3, YSZ, $DyScO_3$, CeO_2, $LaAlO_3$, $GdScO_3$ and $LaScO_3$ have proven to be biocompatible substrates even for sensitive cell systems.

(ii) The dielectric properties of three different ultrathin (≤ 3 nm) SiO_2 and Si-O-N films, which were produced by dry or wet furnace oxidation and an RTP process, were characterised by electrical and electrochemical I-V and C-V measurements. The dry furnace SiO_2 films showed the best suitability as interlayer for an ultrathin SiO_2 – high-k dielectric stack structure: It exhibited the highest breakdown field, the lowest interface state density, small flat-band voltage and low hysteresis in electrochemical C-V characteristics indicating low oxide charge densities.

(iii) The measurement of the dielectric properties of the high-k dielectric films, themselves, yielded the following results: With values of 31 and 29, very high dielectric constants and capacitances were achieved for YSZ and $DyScO_3$ films in electrochemical measurements. As expected, the dielectric constant and capacitances of the Al_2O_3 films was with a value of 10 considerably smaller, but yet 2.5 fold the SiO_2 value. Accordingly, the implementation of YSZ and $DyScO_3$ and to a minor degree of Al_2O_3 as gate dielectric allows the fabrication of ISFETs with much higher input capacitance than the standard SiO_2 (dielectric constant of 3.9) ISFETs used in cell-transistor coupling.

(iv) Due to a hysteresis of 400 mV in the electrochemical C-V characteristics, which indicate high oxide trap densities, the produced CeO_2 films were not suited as ISFET gate dielectric.

(v) Calculations of the voltage distribution between the SiO_2 interlayer and the high-k material stacks indicated that most probably the SiO_2 dielectric breakdown was responsible for the overall breakdown of the SiO_2 – high-k material stacks. Therefore, only minimum breakdown fields of at least 1 MV/cm could be determined for the Al_2O_3, YSZ and $DyScO_3$ films. The actual breakdown fields are assumed to be on the order of the literature values of 3 to 5 MV/cm. Since 3 MV/cm correspond to 0.3 V/nm, the assumed breakdown fields would allow reliable operation of enhancement mode ISFETs with a minimum high-k gate dielectric thickness on the order of 20 nm, which corresponded to a breakdown voltage of 6 V. However, this approximation of a lower thickness threshold is only valid for pure high-k gate dielectrics. Since due to minimisation of the interface state density SiO_2 – high-k dielectric stacks were used as gate dielectric, considerably thinner top high-k dielectric films could be employed.

(vi) The low hysteresis values of 20 and 5 mV for the Al_2O_3 and YSZ films and the moderate value of 70 mV for the $DyScO_3$ film indicate low trap densities and good stability against electrostatic charging. In conclusion, the PLD deposited Al_2O_3, YSZ and $DyScO_3$ films and the corresponding SiO_2 – high-k dielectric stacks exhibit very good electrochemical dielectric properties and are well suited for the implementation as gate dielectric into high capacitance input ISFETs.

(vii) The electrochemical characterisation of an organic dielectric consisting of dodecene (C_{12}) monolayers, which were covalently bound to the silicon via Si – C bonds, yielded breakdown voltages on the order of only several 100 mV. Therefore, the produced layers are not suited as gate dielectric for enhancement mode ISFETs as used in the work of this thesis. Moreover, electrochemical C-V characteristics indicated very high interface state densities, which need to be lowered for a potential implementation into depletion mode devices.

The second part of this thesis dealt with the comprehensive characterisation and comparison of Al_2O_3, YSZ and $DyScO_3$ high-k dielectric ISFETs with an ultrathin SiO_2 interlayer and of the standard SiO_2 ISFETs with lower input capacitance, which are routinely used in our group:

(i) The measured transfer characteristics showed that the high input capacitances of the SiO_2 – high-k material gate stacks did not lead to the expected likewise increase in the drain-source current and transconductance, respectively. In line with the transconductance results, also the signal-to-noise ratios were independent from the ISFET input capacitance. It is assumed that high source and drain feed line resistances and invalidity of the long-channel FET equation for the employed ISFET devices are the underlying reasons. Transconductance values, which were calculated by eliminating the source resistance from the gate-source voltage, were considerably larger than the measured values. This result further affirmed that high feed line resistances limited the performance of the employed ISFETs.

(ii) The assumption that the used ISFET design was responsible for the non-scaling of transconductance and signal-to-noise ratio with the input capacitance was further indicated by the corresponding measurements with ISFETs of different gate widths but equal gate length and gate dielectric: The obtained transconductance values did not follow exactly the relations, which were expected from the simple geometric variation of the gate width, but followed only their trend. The transconductance values, which were calculated by eliminating the source resistance from the gate-source voltage, yielded improved scaling with the gate width. This result further affirmed that high feed line resistances caused the used ISFET devices to deviate from the theoretically expected behaviour. As expected, the noise levels decreased significantly with increasing gate width. Therefore, the signal-to-noise ratio of biomolecule detection experiments can be improved by using ISFETs with large gate widths. For cell-transistor coupling, however, the optimum gate

width is defined by the dimension of the cell to be recorded because the signal is only applied to the gate area covered by the cell body.

(iii) The ion sensitivity measurements showed that the YSZ ISFETs were considerably more sensitive to K^+ and Na^+ ions, in particular around the respective physiological concentrations, than the SiO_2, Al_2O_3 and $DyScO_3$ ISFETs. The underlying reasons are the following intrinsic YSZ properties, which in general determine the ion sensitivity of oxides: A higher density in surface reaction sites (terminating oxygen atoms); considerably different dissociation constants for the acid and base pH sensitivity reactions because pK and pNa sensitivity are secondary effects following from pH sensitivity; or a higher adsorption affinity to K^+ and Na^+ ions. Furthermore, after exchanging the electrolyte for a solution of different pK or pNa value, the YSZ ISFETs exhibited strong characteristic drifts, while the SiO_2, Al_2O_3 and $DyScO_3$ ISFETs exhibited stable signals with small drifts only. Since in general the porosity of the gate oxide accounts for the rate and duration of ion penetration into the oxide and accordingly for the drift behaviour, it is assumed that the YSZ films are considerably more porous than the SiO_2, Al_2O_3 and $DyScO_3$ films. The pH, pK and pNa sensitivity of the SiO_2, Al_2O_3 and $DyScO_3$ ISFETs differed moderately from each other indicating only moderate differences between the SiO_2, Al_2O_3 and $DyScO_3$ films in the intrinsic properties, which determine the respective ion sensitivities.

(iv) The long-term drift measurements of the high-k dielectric and the standard SiO_2 ISFETs revealed the times until the respective ISFETs reach their equilibrium surface potential: While the YSZ ISFETs exhibited over hours very large total drifts of more than 300 mV, the Al_2O_3 ISFETs reached saturation within half an hour and a total drift of less than 20 mV. In comparison with the Al_2O_3 and YSZ ISFETs, the SiO_2 and $DyScO_3$ ISFETs exhibited medium total drifts of 60 to 80 mV with drift durations similar to the YSZ ISFETs of hours. The large long-term drift of the YSZ ISFETs is in line with the observed drift and signal instability during the ion sensitivity measurements. Again higher porosity of the YSZ films, which leads to more and longer lasting ion penetration into the YSZ dielectric than into the other dielectrics, is assumed to be the underlying reason. Accordingly, the small drift of the Al_2O_3 ISFETs indicates the lowest porosity for the Al_2O_3 films. The moderate drifts of the SiO_2 and $DyScO_3$ ISFETs are attributed to intermediate porosity of the SiO_2 and $DyScO_3$ films.

The third part of this thesis covered the bioelectronic coupling experiments with the Al_2O_3, YSZ and $DyScO_3$ high-k dielectric ISFETs:

(i) Surface silanisation of the gate oxide, which allows the assembly of well-defined organic surface architectures, is a prerequisite for charged biomolecule detection experiments. Contact angle measurements indicated that the surface silanisation was performed successfully on Al_2O_3, YSZ and $DyScO_3$ surfaces.

(ii) Because of their large drift following solution exchanges, YSZ ISFETs are not suited for biomolecule detection experiments. However, successful detection of alternately

charged polyelectrolyte layers, which represent a model system for DNA, has been performed with Al_2O_3 and $DyScO_3$ ISFETs. Therefore, both Al_2O_3 and $DyScO_3$ ISFETs seem to be suited for DNA detection. First DNA test experiments with Al_2O_3 ISFETs yielded low hybridisation signals further affirming their suitability.

(iii) Coupling between YSZ and $DyScO_3$ ISFETs (and not with Al_2O_3 ISFETs due to their similarity in ion sensitivity with the SiO_2 ISFETs) and the HL-1 cardiomyocyte cell line has been achieved in first proof of principle experiments and demonstrated the biocompatibility of the YSZ and $DyScO_3$ films.

(iv) The measured HL-1 APs of all ISFETs (including the SiO_2 ISFETs) lacked the expected Ca^{2+} current. As underlying reason, it is assumed that the Ca^{2+} current is either lacking in this cell type or K^+ and Ca^{2+} current have similar kinetics, which compensate each other. Furthermore, the signal shapes measured from HL-1 cells with YSZ ISFETs deviated considerably from SiO_2 and $DyScO_3$ recordings: Following the K^+ current, the APs recorded with YSZ ISFETs exhibited a strong drift against the direction of the K^+ current signal. In the YSZ ion sensitivity measurements, it has been shown that this drift is an intrinsic property of the YSZ gate dielectric. Hence, in a general conclusion, it is assumed that the signal shape in cell-transistor coupling is influenced by the chemical properties of the gate oxide surface such as the drift behaviour.

(v) First coupling experiments between HEK 293 cells transfected with a K^+ channel and YSZ ISFETs further affirmed the assumption from the HL-1 experiments that the characteristic drift behaviour of the YSZ ISFETs influences the recorded signal shape: Although the simultaneously measured K^+ membrane increased during the entire duration of the stimulation pulse, the YSZ ISFET recording exhibited a strong drift against the direction of the K^+ signal.

Concerning the outlook of DNA detection with high-k dielectric ISFETs, the next logic steps will be the performance of more experiments with Al_2O_3 and $DyScO_3$ ISFETs to enhance the understanding of the detection mechanism: Currently, the pH sensitivity of the gate oxide is discussed as a potentially crucial component of the detection mechanism. Although the measured pH sensitivities of the SiO_2, Al_2O_3 and $DyScO_3$ ISFETs showed only moderate differences, the differences were still significant. Hence, it is assumed that DNA detection experiments with Al_2O_3 and $DyScO_3$ ISFETs would allow to clarify the influence of the pH sensitivity on the detection mechanism. The optimum experimental design to meet this question would combine ISFETs with different gate dielectrics and accordingly different pH sensitivities on one chip: This would allow the comparison of DNA signals, which were obtained in identical electrochemical conditions but with ISFETs of different pH sensitivity.

In particular $DyScO_3$ has proven to be an excellent bioelectronic interface for field-effect transistors with high input capacitance: The $DyScO_3$ films exhibited a high dielectric constant of 29 and good chemical stability in the ion sensitivity and long-term drift measurements. Furthermore, the biocompatibility of the $DyScO_3$ films was

demonstrated in successful coupling experiments with electrogenic cells. Therefore, $DyScO_3$ will be implemented as gate dielectric into the next ISFET generations of our institute, which have floating gate architecture [Meyburg, 2005].

In the floating gate architecture, the transistor gate is physically separated from the sensing gate by a feed line, which leads to several advantages compared to the single gate design used in the work of this thesis: Firstly, the physical separation allows to optimise both gates individually for their purposes: the sensing gate for the dimension of the spatially extended membrane and the transistor gate for high transconductance. Secondly, since the transistor gate oxide is located inside the chip, it is well protected from the electrolyte resulting in robust devices. Thirdly, the floating gate has no interface with the silicon channel. Hence, the SiO_2 interlayer, which was used in the work of this thesis to keep the interface state density of high capacitance gate structures low, can be omitted. The employment of pure $DyScO_3$ films as sensing gate dielectric would allow the fabrication of floating gate ISFETs with very high input capacitance without increasing the noise.

The very next transistor generation of our group will be a CMOS floating gate ISFET array with pitch 12.5 µm, similar to the array with pitch 7.8 µm of [Eversmann et al., 2003], which used a 40 nm stack of TiO_2 and ZrO_2 as high-k dielectric sensing gate. Implementation of the studied $DyScO_3$ films as gate dielectric into the prospected CMOS floating gate ISFET arrays is expected to provide robust devices with very high signal-to-noise ratios, which enable to study the dynamics of neuronal nets by recording the activity of all neurons simultaneously similar to the work of [Lambacher et al., 2004].

YSZ has shown to be different from the other studied gate dielectrics: Its characteristics are an ion sensitivity, which is considerably higher than the sensitivity of the SiO_2, Al_2O_3 and $DyScO_3$ films, and a strong, specific drift behaviour. Therefore, the comparison of YSZ with SiO_2, Al_2O_3 or $DyScO_3$ ISFET recordings from electrogenic cells are well suited to study further the assumption that intrinsic surface properties of the respective gate dielectric have an impact on the recorded signals. The optimum experimental design to meet this issue would situate two ISFET gates, of which one is comprised of YSZ and the other of SiO_2, Al_2O_3 or $DyScO_3$, directly next to each other. This would allow to record the activity of a single cell simultaneously with both gate dielectrics and accordingly to compare signal shapes recorded from the identical cell input signal. Such a close distance has been achieved for p- and n-channel ISFETs, which have recently been used to simultaneously record from one single cell [Meyburg et al., 2006].

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Appendix: List of abbreviations and variables

AC	alternating current
AFM	atomic force microscopy
AP	action potential
APTES	3-aminopropyltriethoxysilane
C	capacitance
c_0	ion concentration in the bulk electrolyte
c_J	ion concentration in the cleft
C_{JM}	capacitance of the junction membrane
C_{ox}	(gate) oxide capacitance per unit area
DC	direct current
d	film thickness
d_{EOT}	equivalent oxide thickness
DNA	deoxyribonucleic acid
D_{it}	interface state density
E	electrochemical potential
E_F	Fermi energy
E_i	intrinsic Fermi energy
EOS	electrolyte – oxide – semiconductor
EOT	equivalent oxide thickness
ε	dielectric constant
E_V	valence band energy
FET	field-effect transistor
FMM	fully mismatch
G_J	junction conductance
G_{JM}	conductance of the junction membrane
g_m	transconductance
HEK	human embryonic kidney
I	current
i	index for ion species
IC	integrated circuit
I_{DS}	drain-source current
ISFET	ion-sensitive field-effect transistor
L	channel length
MOS	metal – oxide – semiconductor
MOSFET	metal – oxide – semiconductor field-effect transistor
MW	molecular weight

n	refractive index
PAH	polyallyamine hydrochloride
PC	personal computer
PLD	pulsed laser deposition
PM	perfect match
PMMA	polymethylmethacrylate
Ψ_0, Ψ_s	surface potential
PSS	polystyrenesulfonate
PVD	physical vapour deposition
Pt	platinum
q	elementary charge
RBS	Rutherford backscattering spectroscopy
RMS	root mean square
R^p	Fresnel coefficient parallel to the plane of incidence
R^s	Fresnel coefficient perpendicular to the plane of incidence
R_s	source resistance
RTP	rapid thermal process
S	noise power density per unit frequency band (1 Hz)
SEM	scanning electron microscopy
σ_0	surface charge density
ssDNA	single-stranded deoxyribonucleic acid
TRIS	(tris(hydroxymethyl)aminomethan
V	voltage
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage
V_J	junction potential
V_M	membrane potential
V_S	source voltage
V_T	threshold voltage for charge carrier inversion
W	channel width
YSZ	yttria stabilised zirconia

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