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Influence of low temperature thermal annealing on the performance of microcrystalline silicon thin-film transistors

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Top-gate staggered microcrystalline silicon thin-film transistors (μc-Si:H TFTs) were prepared by plasma enhanced chemical vapor deposition at temperatures below 200 °C. The μc-Si:H TFTs exhibit high effective electron mobilities (device mobilities) of up to 35 $cm^2/V\,s$ for long channel devices. Due to the high carrier mobility μc-Si:H TFTs are promising devices for large area electronics such as organic light-emitting diode displays or radio frequency identification devices. The fabrication process of the μc-Si:H TFTs is similar to the fabrication process of amorphous silicon thin-film transistors, which facilitates an easy transfer of the technology to industry. In this paper, the influence of postfabrication low temperature thermal annealing (150 °C) on the device properties of top-gate staggered μc-Si:H TFTs is investigated. Low temperature thermal annealing reduces the device threshold voltage and subthreshold slope. Furthermore, the annealing step results in an increase of the effective mobility for long channel transistors, whereas the effective mobility for short channel transistors is reduced. The influence of the postfabrication low temperature thermal annealing on the device performances will be discussed in detail. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2710762]

I. INTRODUCTION

With the advance of flat panel display technologies thin-film transistors (TFTs) based on amorphous silicon (*a*-Si:H) have established themselves as an inexpensive and reliable technology for display backpanels. The electron mobility of *a*-Si:H TFTs is sufficiently high to enable operation of liquid crystal flat panel displays at video rate. However, the performance of *a*-Si:H TFTs does not allow for the operation of organic light-emitting diode (OLED) displays. In order to provide stable operation of large area OLED displays at video rate the carrier mobility has to be in the range of 5 $cm^2/V\,s$ or higher.[1] Furthermore, the threshold voltage of the TFTs has to be stable during device operation. Such behavior cannot be provided by *a*-Si:H technology. So far only polycrystalline silicon TFTs provide sufficiently high carrier mobilities and stable threshold voltages.

A promising material for applications in OLED displays is hydrogenated microcrystalline silicon (μc-Si:H). The material mainly comprises of an amorphous and a crystalline silicon phase. μc-Si:H TFTs combine the two worlds of amorphous and polycrystalline silicon. Transistors with high charge carrier mobility can be realized at low temperatures on large areas. Transistors with high carrier mobility have been realized by Mulato *et al.*,[2] Lee *et al.*,[3] and Saboundji *et al.*[4]

In this paper the fabrication and characterization of top-gate staggered μc-Si:H TFTs is described. The TFTs were prepared by plasma enhanced chemical vapor deposition (PECVD) at substrate temperatures below 200 °C. The microcrystalline material was grown in the high pressure and high power regime, which facilitates the deposition of microcrystalline films at high deposition rates.[5,6] The fabrication of μc-Si:H by PECVD is characterized by the formation of a nucleation layer on the substrate. The electronic properties in this region of the film are inferior in comparison to the bulk properties of the μc-Si:H and depend on the deposition conditions used.[7] Therefore, top-gate TFTs were investigated in this study. However, the realization of top-gate staggered TFTs leads to a process flow, in which the dielectric has to be prepared after depositing the channel material. In order to avoid the degradation of the underlying microcrystalline film, the subsequent process temperature is limited by the deposition temperature of the microcrystalline material. Such requirements complicate the fabrication of top-gate μc-Si:H TFTs.[8] However, the performance of the TFTs can be improved by postfabrication thermal annealing at low temperatures.

In the following the influence of postfabrication low temperature thermal annealing (150 °C) on the top-gate

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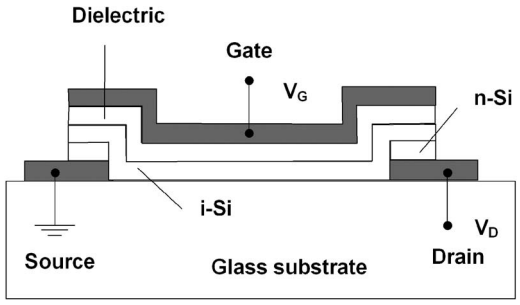

FIG. 1. Schematic cross section of a top-gate staggered microcrystalline silicon thin-film transistor (μc-Si:H TFT). The transistor was fabricated by using a two-mask photolithographic process.

μc-Si:H TFT parameters including the effective mobility (device mobility), device threshold voltage, and device subthreshold slope will be discussed.

II. EXPERIMENT

Top-gate staggered TFT structures were used in this study to take full advantage of the high crystalline volume fraction of bulk μc-Si:H.[7,9] A schematic cross section of a top-gate staggered μc-Si:H TFT is shown in Fig. 1. To allow for the fast evaluation of the materials and the device properties a simple two-mask photolithographic process was developed. The fabrication process starts with the electron beam deposition of a 30 nm thick chromium layer on a glass substrate. Afterwards, a highly doped *n*-type μc-Si:H film was deposited by PECVD at an excitation frequency of 13.56 MHz to form Ohmic contacts between the drain and source electrodes and the channel material. The *n*-type μc-Si:H film was deposited at a substrate temperature of 190 °C by using a gas mixture of silane (SiH_4), phosphine (PH_3), and hydrogen (H_2) at a deposition power of 0.3 W/cm^2 and a deposition pressure of 330 Pa. In the next step, the films were patterned by photolithography to define the drain and source contacts of the transistor. Subsequently a 100 nm thick intrinsic μc-Si:H layer was deposited at a substrate temperature of 160 °C and an excitation frequency of 13.56 MHz using a gas mixture of SiH_4 and H_2. The film was prepared by using a silane concentration (SiH_4/H_2) of 0.75%, a deposition power of 0.3 W/cm^2, and a deposition pressure of 1330 Pa resulting in a deposition rate of 0.3 nm/s. Raman measurements of the intrinsic microcrystalline film were performed to determine the crystalline volume fraction of the material. A crystalline volume fraction of 55% was deconvoluted for the intrinsic μc-Si:H film.

In the next step, a 300 nm thick silicon oxide (SiO_2) gate dielectric was deposited at a substrate temperature of 150 °C. SiO_2 was used as gate dielectric instead of silicon nitride to minimize the defect density at the channel/dielectric interface.[10,11] As the intrinsic microcrystalline layer and the SiO_2 layer were deposited in different PECVD systems the samples were subjected to a hydrofluoric acid dip prior to the deposition of the gate dielectric. By using such a treatment a clean and hydrogenated microcrystalline silicon surface was formed. For the SiO_2 gate dielectric deposition, the source gases silane, nitrous oxide, and helium were used. Finally, the gate electrode was formed by a 100 nm thick aluminum (Al) film.

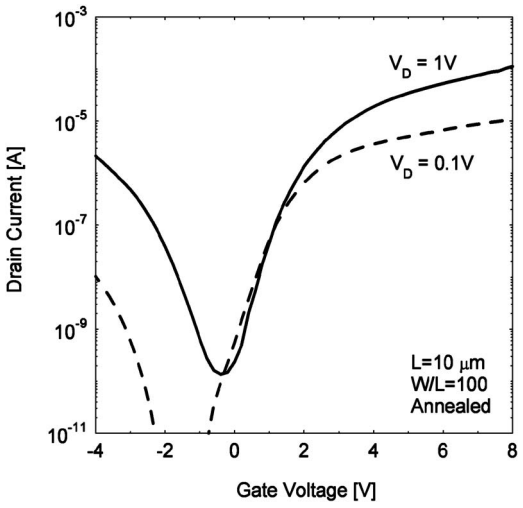

FIG. 2. Transfer characteristics of μc-Si:H TFT (annealed at 150 °C for 30 min) with a channel length of 10 μm and W/L of 100. The transfer curves were measured for V_D=0.1 and 1 V.

μc-Si:H TFTs with a channel length ranging from 2 to 200 μm and a channel width of 200 and 1000 μm were realized. The devices were characterized at room temperature under dark conditions. A standard measurement procedure was established to allow for a comparison of the devices and to exclude the influence of different measurement conditions on the device characteristic. The first measurement of the device characteristic deviates from the subsequent measurements. Therefore, the first measurement of device structures is not presented in the paper. The subsequent measurements exhibit a variation of the device parameters such as the effective mobility, the threshold voltage, and the subthreshold slope by less than 5%. For example, subsequent measurements of μc-Si:H TFTs lead to a shift of the device threshold voltage by less than 0.15 V.

III. RESULTS AND DISCUSSION

A. TFT properties

In the following the device behavior of the μc-Si:H TFTs will be discussed. Figure 2 shows the transfer characteristics of a μc-Si:H TFT with a channel length of 10 μm and a channel width to channel length ratio of 100. The sample was annealed at 150 °C for 30 min in ambient air prior to the measurement. The transfer curves were measured for drain voltages, V_D, of 0.1 and 1 V. The applied gate voltage, V_G, leads to an exponential increase of the drain current in the below threshold region followed by a linear increase of the drain current at higher gate voltages. The exponential increase of the drain current in the below threshold region, I_{Dsub}, can be described by[12]

$$I_{\mathrm{Dsub}} \propto \frac{W}{L}\mu_{\mathrm{eff}} \exp\left(\frac{C_G V_G}{qN_T d_S k_B T}\right), \tag{1}$$

where W and L are the channel width and channel length, respectively. μ_{eff} is the effective mobility, C_G is the gate

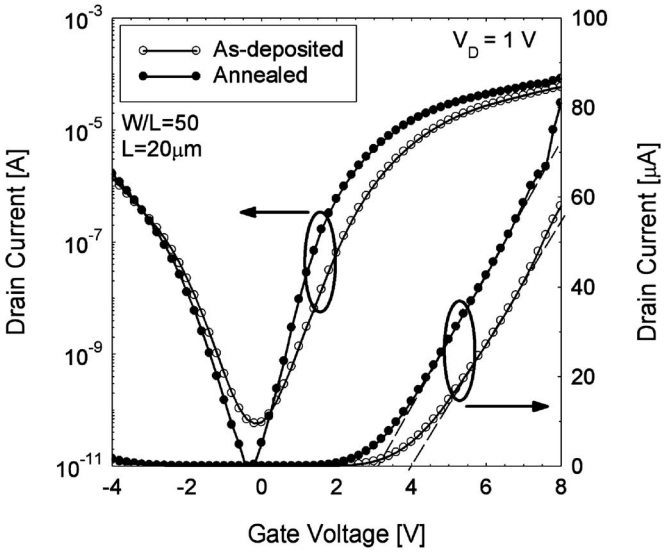

FIG. 3. Transfer characteristics for μc-Si:H TFT with a channel length of 20 μm and $W/L=50$ before and after thermal annealing (150 °C, 30 min).

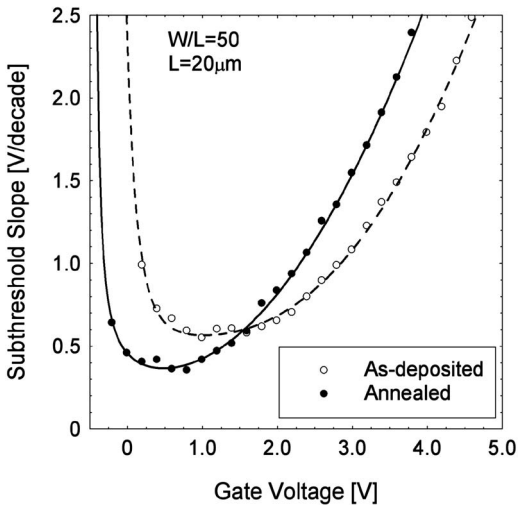

FIG. 4. Device subthreshold slope of the as-deposited and thermal annealed (150 °C, 30 min) μc-Si:H TFT.

capacitance, and q, N_T, d_S, k_B, and T is the electron charge, the defect density in the μc-Si:H, the μc-Si:H channel layer thickness, the Boltzmann constant, and the absolute temperature, respectively. The drain current in the above threshold region, I_D, is described by

$$I_D = \mu_{\text{eff}} C_G \frac{W}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \tag{2}$$

where V_T is the device threshold voltage. An effective mobility of 13 $\text{cm}^2/\text{V s}$ and a device threshold voltage of 1.6 V were extracted from the transfer characteristic measured for $V_D=0.1$ V. The on/off ratio of the TFT for low drain voltages is larger than 10^6. The determined effective mobility is significantly higher than the mobility of conventional a-Si:H TFTs ($\leqslant 1$ $\text{cm}^2/\text{V s}$) prepared by PECVD.

The measured output characteristics (not shown) for the μc-Si:H TFTs demonstrate a linear behavior of the drain current for low drain voltages. However, for high drain voltages, the drain current behavior significantly deviates from the well known a-Si:H TFT behavior, which shows that the drain current saturates at high drain voltages. For our devices, the drain current does not saturate and increases nonlinearly with higher drain voltages ($V_D > V_G - V_T$).

B. Influence of thermal annealing

In order to study the influence of postfabrication temperature treatment on the μc-Si:H TFT properties, the devices were characterized before and after thermal annealing at an elevated temperature of 150 °C for 30 min under ambient air. The annealing temperature was selected to be close to the deposition temperature of the intrinsic microcrystalline layer to avoid the degradation of the device and the effusion of hydrogen out of the microcrystalline film.[13] Figure 3 shows the transfer characteristics of a μc-Si:H TFT with a channel length of 20 μm and a $W/L=50$ for $V_D=1$ V. The effective mobility is slightly increased due to thermal annealing. Furthermore, a device threshold voltage of 3.2 V and a device subthreshold slope of 0.58 V/decade were extracted for the as-deposited transistor, whereas a lower device threshold voltage of 2.3 V and a device subthreshold slope of 0.4 V/decade were determined for the annealed transistor.

Figure 4 shows the device subthreshold slope for the same transistor (before and after annealing) plotted as a function of the gate voltage. A rather broad minimum of the device subthreshold slope for the as-deposited transistor and the annealed transistor is observed. The device subthreshold slope of the transistors, S, can be described by the following equation:[12]

$$S = \frac{\partial V_G}{\partial[\log(I_{\text{Dsub}})]} = \frac{q k_B T N_T d_S}{C_G \log_{10}(e)}, \tag{3}$$

which directly correlates the slope with the material parameters.

The enhanced device performances after thermal annealing can be explained by an improvement (i) of the electronic transport properties of the channel material caused by a reduced density of states (N_T), and/or (ii) a change of the Al gate metal/SiO_2 interface configuration. In the first case, the defect density, N_T, calculated according to Eq. (3) is 4.8×10^{16} $\text{cm}^{-3}\,\text{eV}^{-1}$ for the annealed device and $N_T=7 \times 10^{16}$ $\text{cm}^{-3}\,\text{eV}^{-1}$ for the as-deposited device. The defect densities determined here are comparable to the value reported by Lee *et al.*[14] for microcrystalline silicon. Furthermore, the defect densities are similar to values estimated by electron spin resonance and detailed numerical analysis of microcrystalline silicon solar cells.[15,16] In the second case, the shift of the device threshold voltage is caused by a change in work function difference as a result of the change of energy diagram of the metal-oxide-semiconductor (MOS) structure formed by Al, SiO_2, and μc-Si:H. The thermal treatment leads to a modification of the Al/SiO_2 interface, which affects the energy diagram of the MOS structure.

We suggest the second case is the main reason for the enhanced device performances of the top-gate μc-Si:H TFT. Since the annealing temperature (150 °C) does not exceed the deposition temperature of the intrinsic microcrystalline

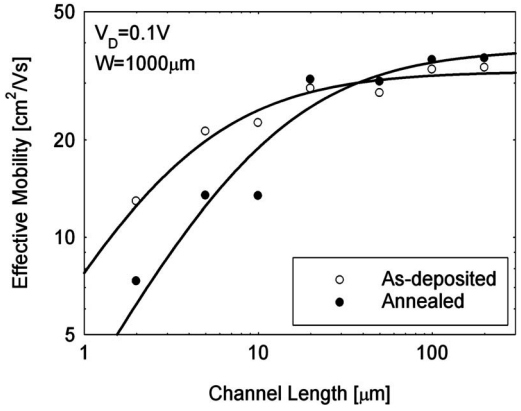

FIG. 5. Effective mobility of as-deposited and thermal annealed (150 °C, 30 min) μc-Si:H TFTs as a function of channel length.

layer (160 °C) and the subsequent SiO_2 layer (150 °C), the properties of the μc-Si:H/SiO_2 interface and the employed bulk materials should not be altered. This implies the reduction of the density of states is not the reason for the enhanced device performances by thermal annealing. The Al gate electrode was thermally evaporated at room temperature, so that the layer was not exposed to higher temperatures. A subsequent thermal annealing might modify the Al/SiO_2 interface and change the energy diagram of the μc-Si:H MOS structure. As a result of the variation of the energy diagram of the MOS structure, the device threshold voltage of the annealed μc-Si:H TFT is shifted to a lower value. Consequently, the device subthreshold slope is reduced.[17]

In order to obtain deeper insights into the influence of thermal annealing on the device properties, the annealing experiment was repeated for μc-Si:H TFTs with various channel lengths. Figure 5 shows the effective mobility of the TFTs as a function of the channel length. The effective mobilities were extracted from the transfer curves measured at V_D of 0.1 V. The effective mobility apparently decreases with decreasing channel length both for as-deposited and annealed transistors. For long channel transistors ($L > 100$ μm), we obtained an effective mobility of 35 cm^2/V s, whereas the effective mobility for short channel transistors ($L=2$ μm) is reduced to below 13 cm^2/V s. The difference in the effective mobility originates from the influence of drain and source contacts on the device performance. Such effects are more pronounced for transistors with short channel lengths.[14,17] In addition to these, for TFTs with channel length shorter than 20 μm, the effective mobility reduces considerably with thermal annealing. A slight increase in the effective mobility for the annealed transistors compared to the as-deposited transistors is noticeable for TFTs with channel lengths of 20, 50, 100, and 200 μm.

The influence of the thermal annealing on the device threshold voltage and device subthreshold slope for the TFTs is demonstrated in Fig. 6. The device threshold voltage and device subthreshold slope reduce with thermal annealing for all TFTs. Furthermore the change in these TFT parameters with thermal annealing is more pronounced for long channel devices compared to the short channel devices.

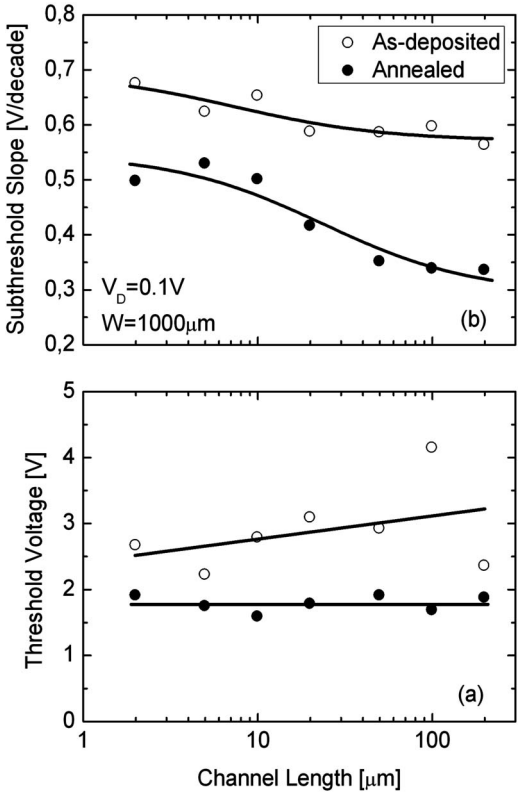

FIG. 6. Device threshold voltage and device subthreshold slope of as-deposited and thermal annealed (150 °C, 30 min) μc-Si:H TFTs as a function of channel length.

The annealing experiments carried out on the TFTs with different channel lengths reveal the distinct influence of thermal annealing on the device performances. To elucidate the different behavior for annealed devices with different geometry, we investigated the TFTs properties as a function of thermal annealing time. The annealing duration was varied from short annealing time of 15 min to long annealing time of 120 min. Figure 7 shows the effective mobility, device threshold voltage, and device subthreshold slope as a function of the annealing time for a TFT with a channel length of

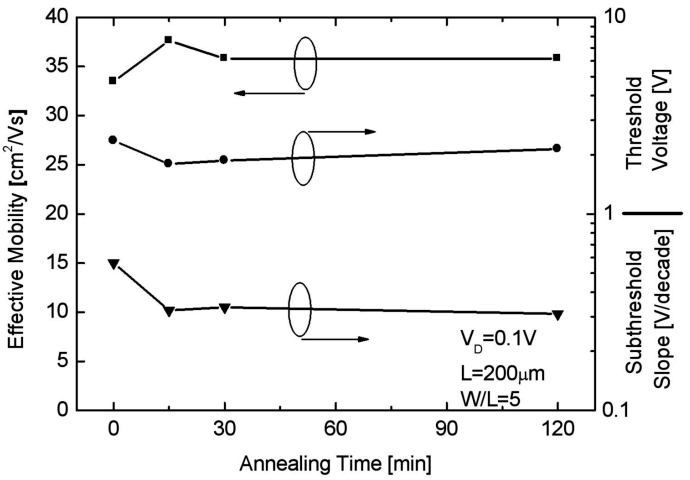

FIG. 7. Effective mobility, device threshold voltage, and device subthreshold slope of a μc-Si:H TFT with a channel length of 200 μm and $W/L=5$ as a function of thermal annealing time.

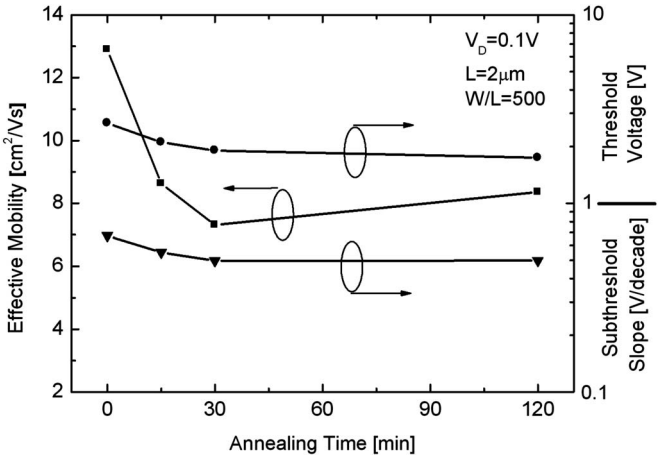

FIG. 8. Effective mobility, device threshold voltage, and device subthreshold slope of a μc-Si:H TFT with a channel length of 2 μm and $W/L=500$ as a function of thermal annealing time.

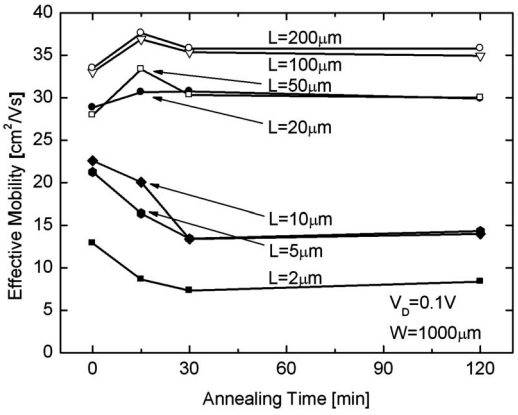

FIG. 9. Effective mobility of μc-Si:H TFTs with various channel lengths as a function of thermal annealing time.

$L=200$ μm and $W/L=5$. The data were extracted from the transfer curves measured at $V_D=0.1$ V. Annealing of the device for 15 min leads to an improvement of the effective mobility by 10%. However, the effective mobility reduces slightly for longer annealing times (15–30 min). Thereafter, the effective mobility remains constant. A shift of the device threshold voltage from 2.3 to 1.8 V and device subthreshold slope from 0.6 to 0.3 V/decade are observed after 15 min of thermal treatment. Afterwards the device threshold voltage and the device subthreshold slope remain nearly unaffected. Therefore, the device subthreshold slope and the device threshold voltage follow a similar trend. The change in the device subthreshold slope is correlated with the change of the device threshold voltage[17] and the shift of the device threshold voltage is associated with the improvement in the Al gate/SiO_2 interface.

To investigate the influence of the thermal annealing step on the short channel device behavior the experiments were repeated for a device with channel length of 2 μm. The extracted short channel device parameters are shown in Fig. 8 as a function of thermal annealing time. The device threshold voltage and device subthreshold slope for TFTs with a channel length of 2 μm follow the trend of long channel devices (200 μm). Both parameters decrease during the first 30 min of thermal annealing. Afterwards both parameters stay nearly constant. For the short channel device, however, we observed a monotonous decrease of the effective mobility within the first 30 min of the annealing time. Such behavior differs from the behavior of the long channel transistor, where the effective mobility slightly decreases after a first increase. The difference in the effective mobility behavior after thermal treatment for short and long channel transistors can be explained by the influence of thermal annealing on the drain and source contacts of the TFTs. The postfabrication thermal treatment causes a degradation of the drain and source contacts, which can likely be attributed to the change of the patterned drain and source contact configuration. It is worth mentioning that the annealing behavior is not reversible and that the as-deposited and annealed TFTs properties remain unaltered when the device is stored in ambient environment. The degradation effect entailed is more pronounced for short channel transistors as the effective mobility strongly depends on the contact properties.[17] Therefore, the improved Al gate/SiO_2 interface, which causes a reduction of the device threshold voltage and the device subthreshold slope is overcompensated by the degradation of the drain and source contacts. In the case of long channel devices, the electronic transport is dominated by the channel material and the drain and source contacts have only a minor influence on the device performances. Therefore, the effective mobility increases with thermal annealing for the 200 μm long device.

Figure 9 shows the effective mobility for transistors with various channel lengths plotted as a function of thermal annealing time. For transistors with channel length longer than 20 μm, an increase in the effective mobility within the first 15 min of thermal annealing can be observed. Thereafter the effective mobility decreases slightly from 15 to 30 min, before the value saturates for prolonged annealing duration. For transistors with a channel length shorter than 20 μm, the extracted effective mobility decreases monotonously within the first 30 min annealing before saturating for longer annealing times. For transistor with channel length of 20 μm, the effective mobility remains almost the same throughout the entire 120 min thermal annealing. In this case, the two effects of drain and source contact degradation and improvement of Al gate metal/SiO_2 interface balance the change of the effective mobility with annealing time.

In order to qualitatively determine the effect of thermal annealing on the drain and source contact degradation, contact resistances for the μc-Si:H TFTs before and after thermal annealing were analyzed. The following equation was employed to extract the contact resistances for the μc-Si:H TFTs from the measured device characteristics:[17]

$$\mu_{\text{eff}} \approx \mu_0 \frac{L}{L + W\mu_0 C_G R_C (V_G - V_T)}, \tag{4}$$

where R_C is the contact resistance for the drain and source contacts, μ_{eff} is the extracted effective mobility from the device characteristics which is subjected to the influence of the contacts, while μ_0 is the intrinsic mobility of the microcrystalline channel material which excludes the influence of the contacts. By fitting the experimental data in Fig. 5 we ob-

tained an increase of the contact resistance within the first 30 min annealing time. In the as-deposited state we extracted a contact resistance of 2 kΩ. After 15 min thermal annealing, the contact resistance was increased to 4 kΩ. For 30 and 120 min the contact resistance stays almost constant at 5.6 and 5.2 kΩ, respectively. The increase in the contact resistance with thermal annealing within the first 30 min causes a considerable reduction in the extracted effective mobility for the transistors with channel length shorter than 20 μm.

IV. CONCLUSIONS

Top-gate staggered μc-Si:H TFTs with an effective mobility of up to 35 $cm^2/V\,s$ and device threshold voltages in the range of 2 V were realized. The experimental results reveal that postfabrication low temperature thermal annealing reduces the device threshold voltage and device subthreshold slope of the transistors, which is attributed to the enhanced Al gate/SiO_2 interface properties. Furthermore, the thermal treatment affects the drain and source contacts of the transistor. For long channel transistors, the effective mobility (device mobility) is improved for annealing times shorter than 15 min, followed by a slight decrease, before saturating for longer annealing times. In the case of short channel transistors, the effective mobility decreases monotonously during the first 30 min annealing, before saturating for prolonged annealing time. The decrease of the effective mobility is caused by the degradation of the drain and source contacts by the thermal annealing, which is manifested by the increase of the contact resistance for the annealed transistors.

Due to the high carrier mobilities μc-Si:H TFTs are promising devices for OLED displays and radio frequency identification devices. The fabrication process of μc-Si:H TFTs is compatible to the fabrication process of *a*-Si:H TFTs, which facilitates an easy transfer of the technology to the industry.

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