



Analysis of the Cathode Electrical Contact in SOFC Stacks

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The cathode contact layer is a critical component in solid oxide fuel cell stacks and one possible cause of degradation. Even though this layer and its interfaces are responsible for a large proportion of the ohmic resistance, it is generally difficult to identify the degradation without carrying out an autopsy of the stack. As a non-destructive method, electrochemical impedance spectroscopy is used in this work to investigate in-depth the cathode contact and its evolution with the support of distribution of relaxation time and differences in impedance spectra analyses between 650°C and 800°C. By purposefully building a stack with a reduced cathode contact area, the electrochemical resistance of the contact is evaluated and its frequency response identified. Through measurements at various operating conditions the different peaks of the distribution of relaxation time analysis are identified and related to physical phenomena within the cell. These findings are then applied to a stack with a standard contact area in order to explain the degradation behavior observed upon dismantling from the test bench.

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Solid oxide cells (SOCs) have long been studied for their efficient and clean electrical generation,^{1,2} renewable fuel production^{3,4} and application in electricity storage.^{5,6} To achieve the power output needed for commercialization, SOC stacks must be built. These are made of a number of cells and interconnectors, assembled in series. The performance of a stack depends on the performance of the individual cells themselves, the conductivity or resistance of the different other materials used⁷ and on design issues like contact area or contact pressure. Peak power performances observed in stacks are generally lower than those obtained in single cells.⁸ Multiple groups have come to the conclusion that this is mostly caused by the cathode/interconnect interface.⁹⁻¹³

Therefore, maintaining decent electrical contact throughout the stack is necessary in order to achieve good overall stack performance. On the anode side, the nickel mesh that serves as a contact layer provides excellent contact with the interconnector and the anode / anode substrate. In most cases, it is spot welded to the interconnector. On the cathode side, an additional ceramic layer needs to be deposited to ensure satisfactory electrical contact. This layer not only assures electrical contact between the interconnector and cathode, but also serves as compensation for the dimensional tolerances of the various parts.^{14,15} Different materials have been investigated in order to fulfill this layer's requirements.¹⁶ Here, a proprietary perovskite compound in the La-Mn-Co-Cu-O system, LCC10, is used.¹⁷ This compound should show good electronic conductivity, an acceptable thermal expansion coefficient and no reaction with the chromium barrier layer on the interconnector.

Jin et al.¹⁸ investigated the effect of the cathode contact area with respect to peak power densities and degradation rate. They found that both increased with contact area up to a certain point. They established the optimal contact area to be around 45% of the cathode area. Similar work on the contact area was conducted by Jiang et al.⁹ Using IV curves, they revealed that the contact area affects both the cell resistance and polarization losses.

When a stack, or more commonly one layer thereof, starts to fail, the test is often halted and the stack taken for post-test analysis. However, it would be of interest to be able to employ a non-destructive method to analyze the degradation of the stack and its causes in situ. In certain cases, the operating parameters could be adjusted. In this regard, electrochemical impedance spectroscopy (EIS), combined with a distribution of relaxation times (DRT) analysis is of great interest.

In particular, the voltage of the lowest cell systematically drops upon dismantling/remounting the stack in the test bench. According to our experience, we suspect this behavior to be related to an increased resistance at the cathode contact.¹⁹ In this work, we will explore this hypothesis. First, the ohmic resistance will be separated into its different components (electrolyte, contact, ...). Then, using a stack with a reduced contact area, EIS and DRT will be employed to investigate the effect of the contact area and define its electrochemical response. Finally, these results will be applied in a standard stack exposed to dismantling/remounting.

Experimental

Stack preparation.—Three 4-layer Jülich F10 design²⁰ stacks were built. A standard build consists of two Crofer 22 APU end plates, three Crofer 22 APU interconnectors and four anode-supported cells (ASC). The 4-layer F10 stack (F1004) is built similarly to the 2-layer model shown in Figure 1.

The ASCs have a Ni-8YSZ (8 mol% yttria-stabilized zirconia) anode, an 8YSZ electrolyte, a screen-printed GDC ($\text{Ce}_{0.8}\text{Gd}_{0.2}\text{O}_{1.9}$) diffusion barrier layer and an LSCF air electrode ($\text{La}_{0.58}\text{Sr}_{0.4}\text{Co}_{0.2}\text{Fe}_{0.8}\text{O}_{3-\delta}$). Cells are $10 \times 10 \text{ cm}^2$ with an active area of $9 \times 9 = 81 \text{ cm}^2$. A Ni mesh welded to the interconnector serves as the anode contact, creating at the same time the gas distributor. On the cathode side of the interconnector, a manganese-cobalt-iron (MCF) oxide protective layer is applied by atmospheric plasma spraying (APS). The stack is sealed inside and outside using a proprietary glass ceramic. More information about the stack design can be found elsewhere.^{12,20,21}

The difference between the various stacks used in this study resides in the geometry of the cathode contact layer and electrolyte thickness (see Table I). Stacks F1004-87 and F1004-79 have a standard LLC10 ($\sigma \approx 80 \text{ S.cm}^{-1}$)²² coating applied over the complete cathode (see Figure 2a). An interconnector consists of 30, 0.14 cm wide, contact ribs that are applied over the 9 cm of the active cathode area. The standard cathode contact surface area is therefore 37.8 cm^2 . In contrast, F1004-86 has only 10 screen-printed strips of LCC10 printed on the surface of the cathode to reduce the overall contact area. The screen-printing mask was designed for each strip to be 0.63 cm wide. The strips are positioned perpendicularly to the air channels of the interconnector (see Figure 2b). Therefore, the contact area of each cell in stack F1004-86 consists of 300 small rectangles, each with an area of $\sim 0.14 \times 0.63 \text{ cm}^2$. The theoretical overall cathode contact surface area is 26.5 cm^2 , which corresponds to 70% of the standard

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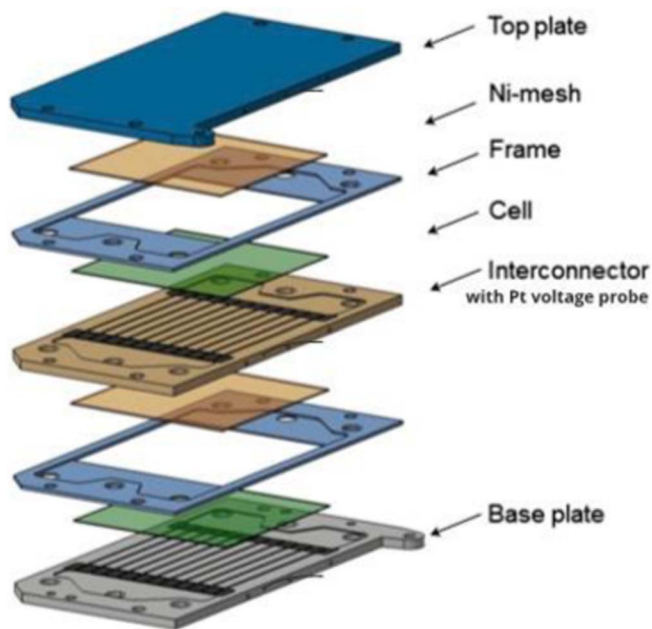


Figure 1. Jülich F10 Design.²⁰

contact area. Upon measurement of the contact area on the cells, it was established that the contact surface area was a bit smaller than planned, that is $\sim 65\%$ of the standard one. Finally, in stack F1004-79, layers 2 and 4 contain a standard $10\ \mu\text{m}$ electrolyte, whereas layers 1 and 3 contain a thinner $5\ \mu\text{m}$ electrolyte. The design was decided to allow for isolating the resistance difference due to a $5\ \mu\text{m}$ thicker electrolyte.

All stacks were tested with a 100 kg clamping weight. A thicker interconnector, with 40 mm-deep boreholes, was positioned between layers 2 and 3 to allow for temperature measurements to be made in the center of the stacks. The sealing process involved a 100 hour hold at 850°C . The reduction was carried out at 800°C by increasing the amount of H_2 stepwise. Thereafter, the stacks were characterized and followed their own testing protocol.

Electrochemical characterization.—EIS^{23,24} was carried out on a Zahner IM6 electrochemical workstation. Measurements were performed near OCV ($5\ \text{A DC} \pm 2\ \text{A AC}$) in the frequency range from 10/100 mHz to 100 kHz, in a wide range of operating conditions (gas composition and temperature). A 4-point probe method was used for the spectroscopy. Due to the gastight requirement of a complete stack, the probes can't be placed as close to the cell as for single button cell measurements. The Pt voltage probes were therefore located on the interconnector (see Figure 1) between each layer (i.e. 5 probes for a 4-layer stack). Therefore, in a stack, the impedance measured is the one of a repeating unit and not of a cell alone. The current leads were connected to the end plates. The geometry used was based on the findings of Mosbaek et al.²⁵ in order to minimize measurement errors, especially the inductance.

While 3-electrode impedance measurements have been reported to enable better separation of the various impedance components,^{26,27} the constraints of a stack did not allow its implementation here. Therefore,

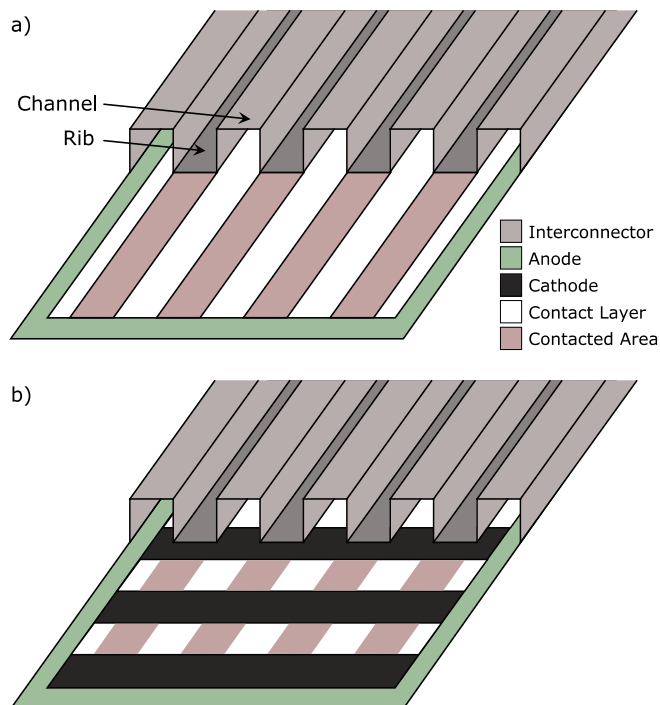


Figure 2. Schematic of the design differences between the standard (a) and reduced (b) contact areas.

impedance components were isolated by building stacks with different electrolyte thickness or smaller contact surface area, as described in the previous section.

The DRT²⁸ analysis of the EIS spectra was carried out with the Matlab toolbox DRTTools.²⁹ The inductive data was not fitted and a regularization parameter $\lambda = 10^{-4}$ was used for the Tikhonov regularization. Another exploration of the EIS data was conducted through the analysis of the difference in impedance spectra (ADIS) as described by Jensen et al.³⁰ The area-specific resistance (ASR) was evaluated either through the EIS measurements or the evaluation of the voltage drop with respect to Nernst potential during a current-voltage (IV) curve.

Results and Discussion

Resistance of the cathode contact.—From the EIS measurements carried out on stack F1004-79, the ohmic resistance was separated and is presented in Figure 3. Layers 1 and 3 exhibit a smaller ohmic resistance than layers 2 and 4, underlining the influence of the thinner electrolyte. The average ohmic resistance for layers with $5\ \mu\text{m}$ and $10\ \mu\text{m}$ -thick electrolytes, respectively, was calculated at each temperature. Given that the only difference in the cells is their electrolyte thickness, it was assumed that the ohmic resistance difference between the layers to be only due to the electrolyte thickness. By subtraction, a value corresponding to the resistance of a $5\ \mu\text{m}$ electrolyte was thus obtained. The results are presented in an Arrhenius-type plot in Figure 4. The activation energy of $0.91\ \text{eV}$ is on the low end of literature values for oxygen ion diffusion in YSZ.^{31–33}

Table I. Overview of the stacks used in this study.

	F1004-79	F1004-86	F1004-87
Electrolyte thickness	Layer 1,3: $5\ \mu\text{m}$ Layer 2,4: $10\ \mu\text{m}$	$10\ \mu\text{m}$	$10\ \mu\text{m}$
Cathode contact area	$37.8\ \text{cm}^2$ (100%)	$\sim 24.5\ \text{cm}^2$ ($\sim 65\%$)	$37.8\ \text{cm}^2$ (100%)

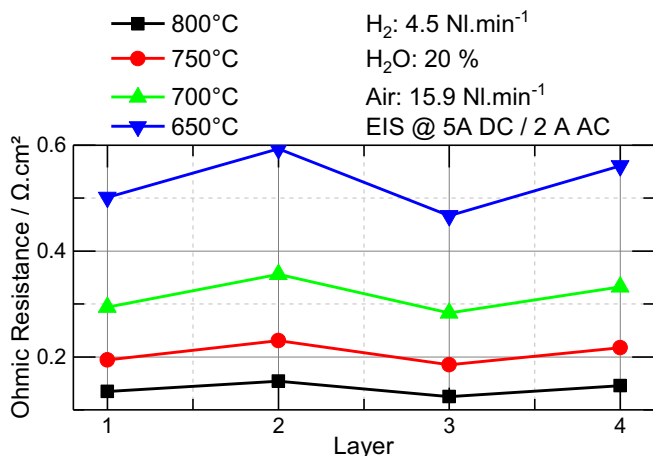


Figure 3. F1004-79 ohmic resistance in the different cells.

Knowing the bulk resistance value for a $5 \mu\text{m}$ YSZ electrolyte, we can also calculate the resistance for a $10 \mu\text{m}$ YSZ electrolyte. The part of the ohmic resistance due to the cathode contact resistance is then calculated using the following formula:

$$R_{\Omega} = R_{\text{Contact Cathode}} + R_{\text{Contact Anode}} + R_{\text{Electrolyte}} + R_{\text{Others}}$$

Given the excellent anode contact, we assume $R_{\text{Contact Anode}} \approx 0$. R_{Others} include other components of the ohmic resistance, such as the oxidation of the metallic interconnector, and are assumed to be minor with regard to the electrolyte and cathode contact shares.^{34,35} So the cathode contact resistance is being isolated by using multiple stacks (see Table I) with structural differences. The resistance of the cathode contact for different temperatures is presented in Figure 5. The good reproducibility, for instance between stacks F1004-79 and F1004-87, validates our method, based on multiple independent stacks. Stack F1004-86 with the reduced contact area shows on average a $\sim 57\%$ higher resistance, i.e., the cathode contact resistance of F1004-79 and F1004-87 is on average $\sim 36\%$ lower. This matches quite well with the reduction of the surface area built into stack F1004-86 (i.e. $\sim 35\%$). However, the difference is less pronounced at lower temperature; 39% at 800°C but only 29% at 650°C . At lower temperature the total ohmic resistance increases more than the contact resistance, due to the higher activation energy of the electrolyte resistance compared to that of the cathode contact (Figure 4). Therefore the relative effect of the same reduction of the contact area is smaller.

It is also to be noted that the resistance of the cathode/interconnect interface represents between 65% and 70% of the overall ohmic resistance. Therefore, its degradation also has a significant impact on the performance of the stack. This is highlighted by the performance of

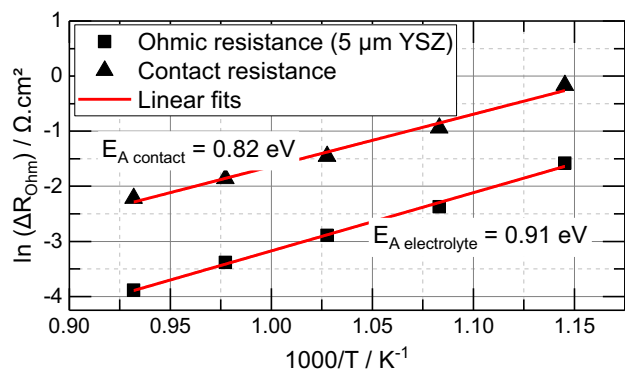


Figure 4. Arrhenius plot for the difference in the ohmic resistance between the cells with thin and thick electrolyte, as well as the contact resistance.

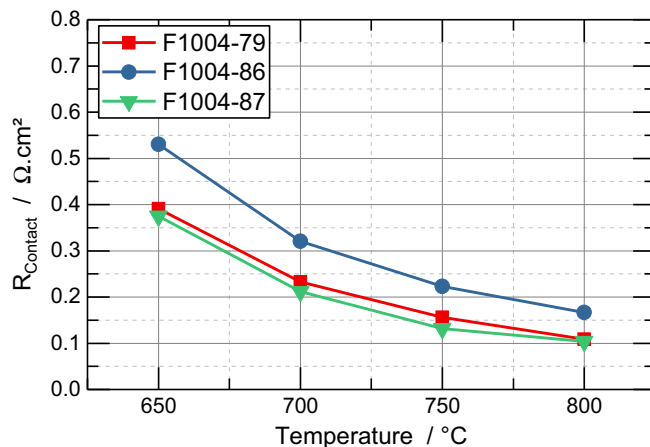


Figure 5. Resistance of the cathode contact for different temperatures.

stack F1004-86, which was purposefully built with a reduced contact layer. The ASR was computed for both stacks; F1004-86 and F1004-87 (see Figure 6). The performance of stack F1004-87 is significantly better. Given that the only alteration between the two stacks is the contact layer area, the change in performance can be attributed to the lesser contact on the cathode side. One can also note that the measurements made through the IV curves at 5A and the EIS data match reasonably well. The slightly higher ASR observed in cell 1 could be due to a temperature effect. Indeed, in the furnace, this bottom cell is often slightly colder than the rest of the stack.

The normalized resistance is a useful way to analyze the degradation. For different temperatures, Figure 7 presents the ohmic, electrode polarization and total resistance of the degraded F1004-86, normalized by the reference stack F1004-87. On average, the ohmic resistance of stack F1004-86 represents 73% of the ohmic resistance for stack F1004-87. For the polarization resistance the ratio is 88%. These results show that the reduction of the contact layer – by 35% – is partly compensated by in-plane electronic conduction, as all values are above 65%. Overall, the ratio of the total ASRs is 77%, such that the 35% decrease in the contact layer area only lead to a 23% performance decrease. This effect had been modeled by Gazzari et al.³⁶ and our experimental results are in accordance with their theoretical prediction. The detailed evolution of the ohmic and polarization resistance with respect to temperature is further commented in the following section.

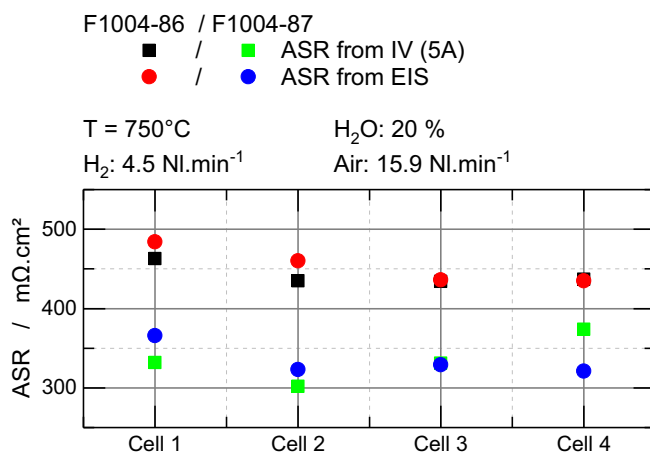


Figure 6. Comparison of ASR values for F1004-86 (with reduced cathode contact area) and F1004-87 calculated through IV curves and EIS.

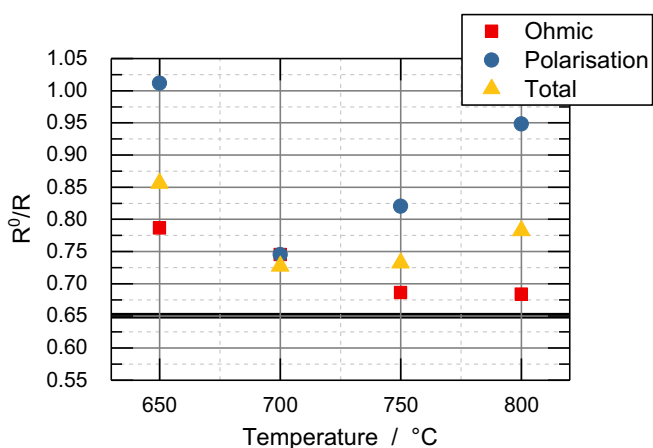


Figure 7. Ratio of the ohmic and polarization resistance between reference stack F1004-87 (R^0) and stack F1004-86 (R).

Influence of the contact area in EIS/DRT data.—Figure 8 presents the electrolyte, contact and polarization resistances obtained from EIS measurements. Stack F1004-86, with its reduced contact layer, not only shows a higher ohmic resistance as discussed in the previous section, but also exhibits an increase in the polarization resistance. With decreasing temperature, the ohmic resistance increases in absolute value due to poorer ionic and electronic transport. However, proportionally the effect of the contact area reduction becomes smaller (see also Figure 7). The assumption is that at lower temperature, the effect of the reduction of the contact area is dwarfed by the poorer ionic conductivity of the electrolyte. This can be explained by the higher activation energy of the electrolyte resistance. (see Figure 4). As expected, the polarization resistance also increases with decreased temperature. However, the polarization resistance ratio (see Figure 7) doesn't evolve evenly with temperature. It shows a minimum around 700°C. The hypothesis here is that the reduced contact area mostly has an effect on the polarization resistance due to poorer charge transfer reactions at the cathode. This mechanism is predominant in the polarization resistance at temperature between 800°C and 700°C, leading to a smaller R^0/R ratio. However, at 650°C, the diffusive transport of the gas species involved in the electrode reactions becomes the major component of the polarization resistance. This leads the absolute polarization resistance to being a factor of 2 higher at 650°C than at 700°C. Therefore, at 650°C, the effect of the smaller contact area in the charge transfer reaction is insignificant in regard of the resistance

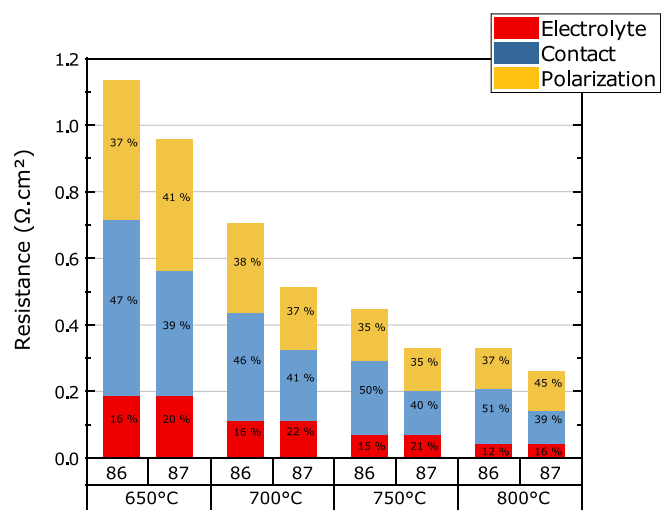


Figure 8. Detailed resistance of stacks F1004-86 and F1004-87.

due to diffusion of species. Therefore, the ratio of the polarization resistance in Figure 7 is close to 1 at 650°C.

The extent of the ohmic resistance increase is more stable with temperature than the one of the polarization resistance (see Figure 7). The hypothesis is that at 800°C the increase in polarization resistance is minimal because of the kinetics favored by high temperature. On the other hand, at 650°C, the electrochemical reaction processes in the cells are already responsible for higher losses and the effect of the cathode contact layer becomes negligible. Therefore, the polarization resistance is mostly impacted by the poor cathode contact layer at intermediate temperatures.

An ADIS analysis is presented in Figure 9. As it was formerly found that the polarization resistance is mostly impacted by the smaller cathode contact area at intermediate temperatures, it is coherent to see the major differences in the ADIS analysis at 700°C and 750°C. Indeed, the analysis in frequency shows that the main difference in the spectra lies in the 100 Hz - 1 kHz region, with a distinct peak around 1–3 kHz.

The perfect superposition of the four cells for measurements below ~0.5 Hz is statistically very unlikely. It is a measurement error that should be ignored in the analysis. This noise observed in the EIS measurements, mostly for stack F1004-87, is partly due to the data acquisition conditions. At low frequency, the acquisition times were not long enough to average data over sufficient periods. Moreover, EIS measurements of stacks are altogether more challenging than for single cells. For instance, the different metallic components of the stack can lead to frequency disturbance. Stronger temperature and compositional gradients also complicate data acquisition.^{25,37} To reduce these effects, the EIS measurements were set up so as to separate as much as possible the current and voltage probes.

While a response in the kHz frequency domain has been reported in the literature as being due to electrochemical processes (charge transfer reaction, ionic transport) in the fuel electrode,^{38–41} additional measurements were carried out here to confirm these results. Figures 10a–10d) presents the DRT analysis for stack F1004-86 operated under different conditions. Four major peaks can be observed, at 1–10 Hz, 10–100 Hz, 300–500 Hz and above 1 kHz. The highest peak is only significantly influenced by the temperature variation, which suggests this peak could correspond to a charge transfer process. The response at ~300–500 Hz is particularly sensitive to temperature and partial water pressure, indicating that it could also be associated with anodic electrochemical processes. The peak around 10–100 Hz could actually be two processes overlapping (see Figure 10c). Its sensibility is low, but it reacts to all changes of operating conditions, though mostly to water vapor. In literature, this peak is usually linked to oxygen surface exchange kinetics and O^{2-} diffusivity in the cathode, but because of the water sensitivity, this peak could also be a secondary peak of the anode gas diffusion. The response in the 1–10 Hz range is deeply influenced by the vapor content and to a lesser extent by the hydrogen amount. This peak can therefore be related to gas diffusion in the anode substrate. An overlap with a triple-phase boundary electrochemical process is possible. The literature reports another peak below 1 Hz, related to gas diffusion in the cathode structure, when oxygen partial pressure is too low.³⁹ However, given the amount of air used in this study, this response was, as expected, not observed here. Overall, this identification correlates well with previously reported results.^{38–41}

DRT spectra of F1004-86 and F1004-87 at 700°C are compared in Figure 11. A negative shift in frequency is observed, as well as an increase in the two responses at the highest frequencies. Therefore, the decrease of the contact area also seems to have an impact on the anode polarization. In any case, it corresponds well that they were found to be linked to charge transfer activity.

Application to a standard stack.—Stack F1004-84 is a standard stack with a 10 μm electrolyte and standard cathode contacting layer. This stack was built to be subjected to thermal cycles. Cycles are carried out between the operating temperature (700°C here) and either 200°C or room temperature. As is seen in Figure 12, the stack is little

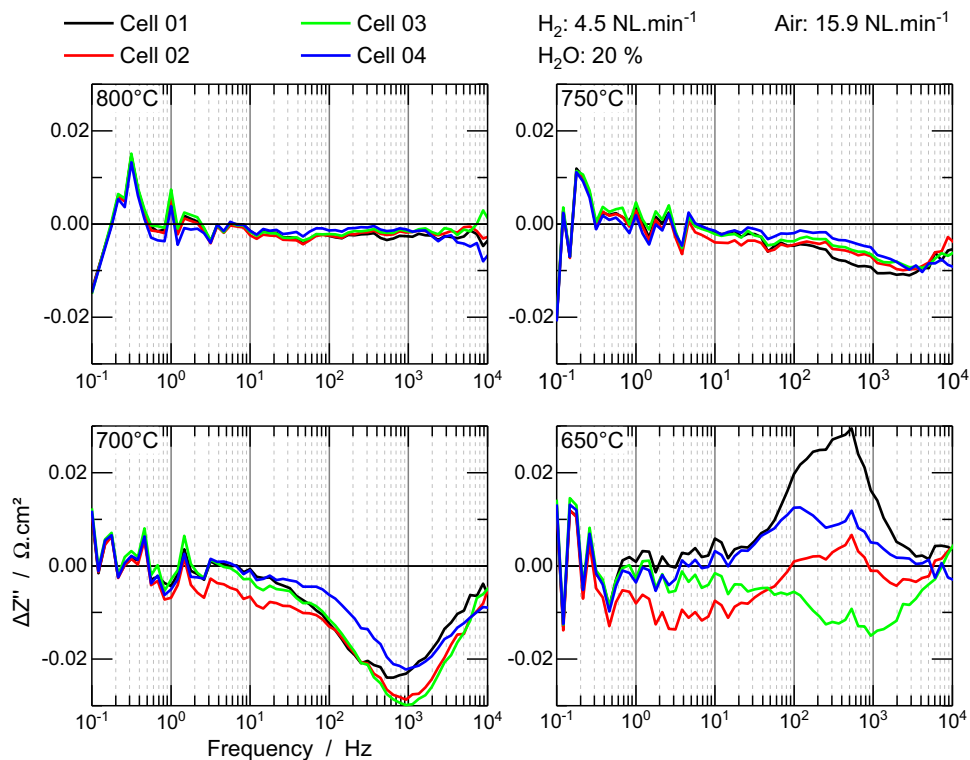


Figure 9. Analysis of differences in impedance spectra (F1004-86 vs. F1004-87).

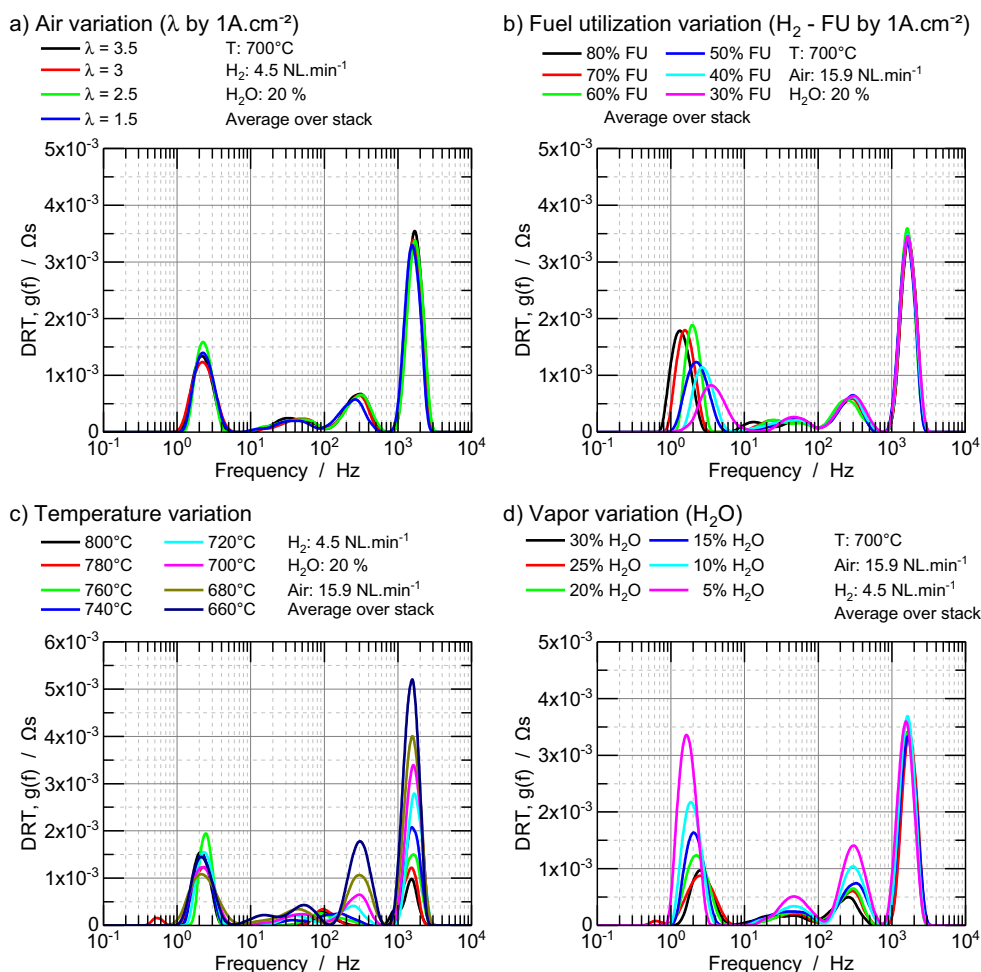


Figure 10. DRT analysis of stack F1004-86 for different operating conditions.

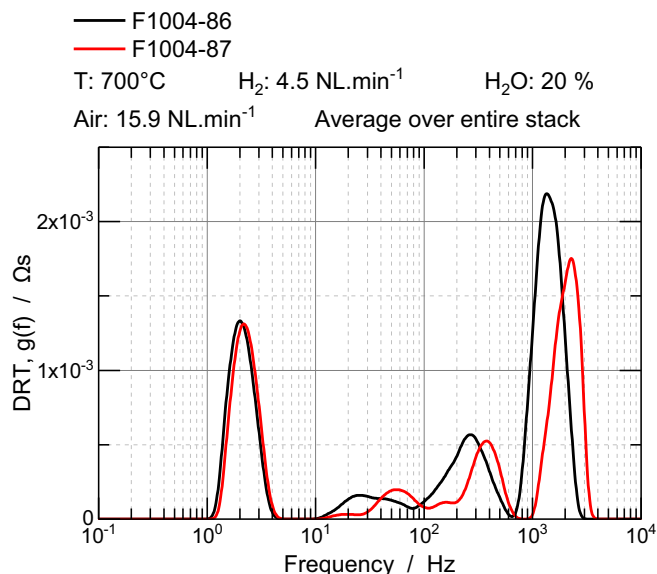


Figure 11. DRT comparison of stacks F1004-86 and F1004-87.

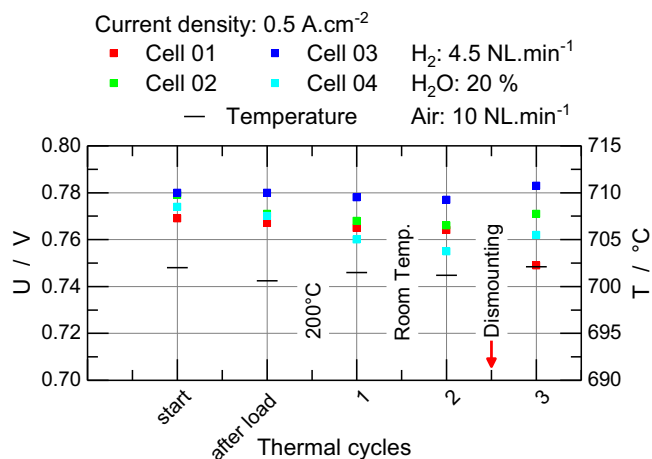


Figure 12. F1004-84 Evolution of voltage at 0.5 A.cm^{-2} versus thermal cycles.

impacted by thermal cycles 1 and 2. However, a notable decrease can be noticed in the lowest layer (cell 01) when the stack is also dismantled from the test bench. This has been observed in multiple investigations.

For stack F1004-84, EIS measurements were carried out during each cycle. The data is presented in Figure 13. The comparison of cells 01 and 04 highlights the increase in both ohmic and polarization resistance in cell 01 after the dismantling/remounting of the stack. The DRT analysis is presented in Figure 14. The increase in the 10^3 – 10^4 Hz peak, as well as the slight shift in the lower frequency correlate well with the observation made on stack F1004-86. This would point toward a partial detachment of the interconnector as the cause of the performance degradation. This deterioration in the cathode contact could be due to the lack of mechanical clamping between dismantling and remounting of the stack. However, a smaller peak below 1 Hz is also detected. This response was not seen in stack F1004-86. This could mean that an additional degradation mechanism is happening here. However, it could also be a measurement artifact.

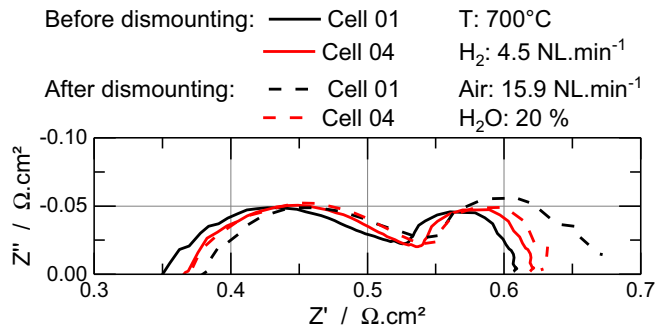


Figure 13. F1004-84 EIS Data before and after thermal cycle with dismantling.

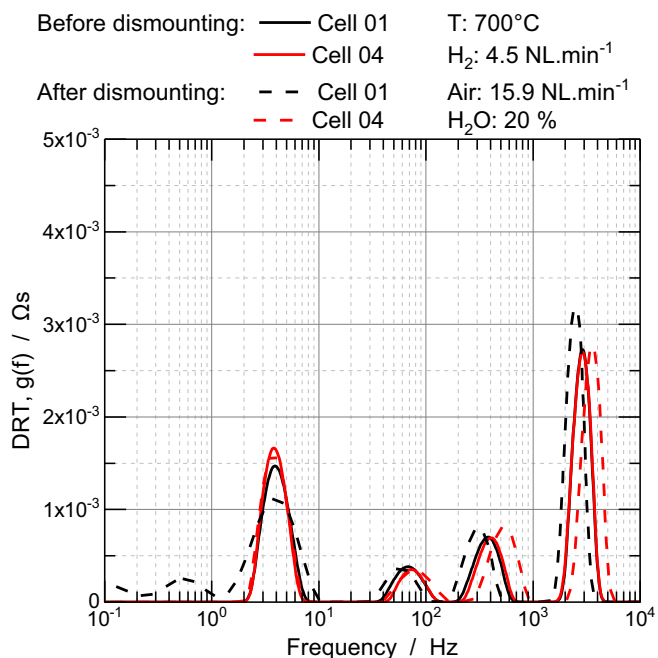


Figure 14. DRT Analysis of F1004-84 EIS Data before and after thermal cycle with dismantling.

Conclusions

The importance of the cathode contact in the performance of an SOFC stack was highlighted. Its effect was identified using EIS and DRT data. An increase in both the ohmic and polarization resistances was observed. This increase was quantified thanks to the calculation of the electrolyte and cathode contact resistances. It was observed that when the contact layer area was reduced by 35%, the performance was only reduced by 20–25%. This can be explained by in-plane electronic conduction partially making up for the reduced contact area. The experimental observations compare well with the predictive models. In the DRT data, the response to a reduction of the contact area was witnessed in higher frequency peaks (~ 300 – 500 Hz and above 1 kHz). A peak identification confirmed that they were related to electrochemical activity, presumably related to a charge transfer process in the air electrode. With a standard stack (F1004-84), the performance decrease of the lowest cell observed upon dismantling/remounting stacks, was partly related to the degradation of the contact layer. Observations made on the standard stack correlate well with the results drawn from the stack purposefully built with a reduced contact area.

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