An Automatic Baseline Regulation in a Highly Integrated Receiver Chip for JUNO

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An Automatic Baseline Regulation in a Highly Integrated Receiver Chip for JUNO

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Abstract. This paper describes the data processing unit and an automatic baseline regulation of a highly integrated readout chip (Vulcan) for JUNO. The chip collects data continuously at 1 Gsamples/sec. The Primary data processing which is performed in the integrated circuit can aid to reduce the memory and data processing efforts in the subsequent stages. In addition, a baseline regulator compensating a shift in the baseline is described.

1. Introduction

The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose neutrino experiment based on a 20,000 t liquid scintillator. The primary objective is the determination of the neutrino mass hierarchy by observing reactor anti-neutrinos [1]. The detection system has to accomplish both accurate energy measurements of the incoming neutrinos as well as precise muon tracking for background reduction [1]. Thus, the readout system must provide good timing for the position reconstruction and a triggerless charge measurement of the signals delivered by around 17,000 photomultipliers (PMT).

The readout electronics is integrated into the PMT housing for best performance, minimum power dissipation and reduction of the number of cables in the detector. The accuracy of the charge integration is achieved by a highly-integrated receiver chip called Vulcan, which includes the analog to digital converter (ADC) and the analog front-end. The current generated by the PMT is first converted into a voltage and then into a digital data stream.

The current signal is measured to detect the amount of photoelectrons (p.e.) that hit the PMT. The load of a single p.e. is calculated from the signal amplitude with respect to the average baseline of the signal. This baseline can shift due to biasing changes of the PMT, and fluctuations in the biasing of the front end circuitry. In order to minimize the influence of these baseline shifts, a compensation scheme is described.

In parallel, the digital part of the receiver chip compresses the data and includes timing information, as well as processing the signal in parallel for a fast trigger generation. A major feature in the processing scheme of the highly-integrated receiver chip is the vast configurability that enables alternative modes and tuneable operation parameters. Out of the many blocks that

compose the highly integrated receiver, two units are presented in this paper: the central data processing unit and the baseline regulator.

2. The Data Processing Unit and the Baseline Regulator

The data processing unit receives its input from analog to digital converters in the chip. Vulcan is equipped with three ADCs working in a configurable voltage range. Due to the different voltage ranges of each receiver, the chip needs a customized data processing unit to distinguish data from each ADC. Additionally, noise detection is deployed to reduce the data rate in-between signal events.

A key objective in the data processing concept is to avoid the loss of data even during periods of high neutrino fluxes. This is the case for nearby super nova ($\sim 3\,\mathrm{kpc}$) explosions that cause 6×10^5 neutrino events in a duration of 10 seconds [2]. To ensure the proper dimension of the internal processing memory, a simulation has been performed [3]. The maximum observed filling was 5 kB, so the size of the ring buffer was set to 20 kB including a safety factor of four.

Due to the weakly interacting nature of neutrinos, the detector will scarcely measure neutrino signals and mostly dark noise [2]. The data processing unit was customized to identify and compress this noise by applying a threshold criterion. Short periods of noise mode are suppressed with a hysteresis mechanism to avoid overhead from unnecessary bus mode changes. Effectively, the data processing unit can filter 3 GByte/s data to 1 GByte/s data and with an additional noise compression further down to 0.5 GByte/s.

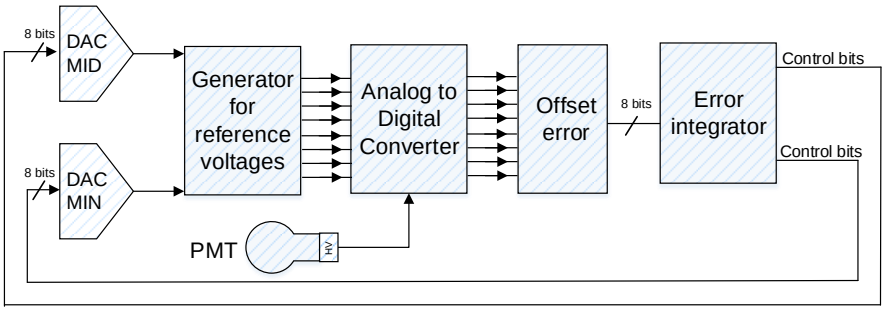

Figure 1. Block diagram of the baseline regulator.

The baseline regulation is designed as a control loop with its concept shown in Figure 1. The regulator encloses a resistor ladder which provides the reference voltages for the ADC comparators. Ideally, the ADC measures the signal starting from 0 volts but an offset in the system will shift the baseline to a non-zero value. If this baseline shift is not corrected, the measured signal will include the offset. The baseline regulator that is proposed here will estimate the offset and adjust the reference of the comparators to counteract the shift.

As a first stage, the error signal generator produces a voltage signal by calculating the difference between the incoming signal and the baseline. This error signal is scaled down to lower the impact of spikes and then integrated. The outputs of the integrator are two sets of control bits to the digital to analog converters, which in turn set the reference voltages of the comparators. The proposed regulation loop is active only during calibration phases and is turned off during measurement phases, in case of the latter the reference voltages are retained to the previously calibrated value.

3. Simulation Results

Functional verifications for the data processing unit with Modelsim simulation tool complied with the requirement of the experiment for range selection, noise reduction and data output format. The impact of baseline shifts to a signal without and with regulation were investigated

with MATLAB simulations and are shown in Figures 2 and 3. They show that an active regulation corrects the ADC output such that it matches the input signal. The offset in the baseline produces an error signal, which is integrated and the integrator consequently adjusts the reference voltage (refer to Figure 4) which in turn decreases the offset and causes the integrator to settle to a constant value as can be seen in Figure 5.

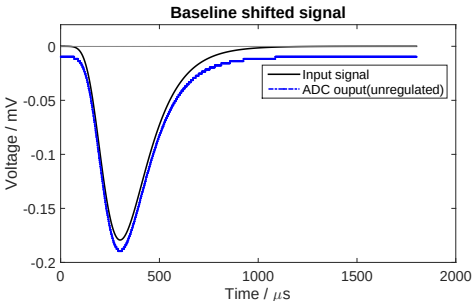

Figure 2. Input signal (black) and unregulated ADC output signal (blue) with a baseline shift.

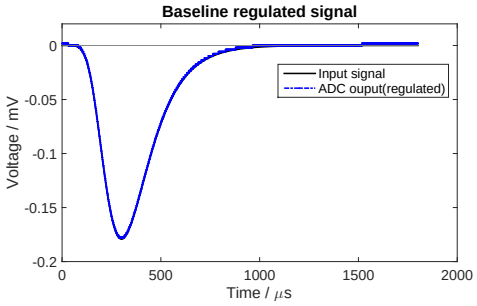

Figure 3. Input signal (black) and ADC output (blue) with baseline shift compensated.

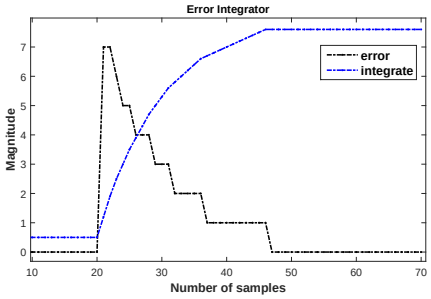

Figure 4. Instantaneous (black) and integrated (blue) error signals of the error integrator block.

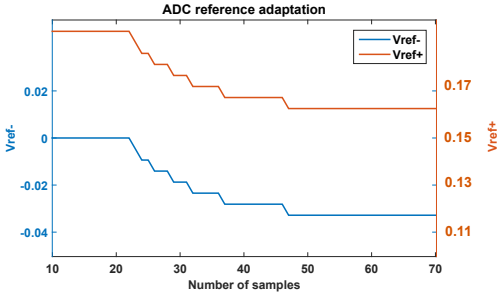

Figure 5. Changes in the reference voltages of the ADC, blue for the lower end and orange for the middle DAC.

4. Summary

A highly integrated receiver chip is designed for the PMT readout of the JUNO experiment. The data processing unit was tailored to the required data reduction capabilities and the output data format. In addition, the design of the baseline regulation and its impact on the system performance is presented. This effectively counteracts baseline shifting effects of parasitic distortion and thus increases the accuracy of the measurement.

References

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