VERIFICATION OF A 65NM CMOS IC FOR VARIOUS APPLICATIONS
(NEUTRINO DETECTION, HIGH ENERGY PHYSICS, ETC.)

18TH APRIL 2018  I  CHRISTIAN ROTH
VULCAN CHIP OVERVIEW

• The Vulcan Chip
  • Highly linear, fully integrated circuit – **Vulcan**
    • Sampling ADC with approx. 80 dB linearity (3 signal chains with 3 different gains)
    • No external components required
    • On-chip clock generation from ref. clock
  • Precise signal reconstruction
    • No analog delay line (reducing noise & distortion)
    • Control loop to suppress DC variations
    • Optional overshoot compensation
  • Further key parameters of Vulcan:
    • ADC with 9.5 bit (3x 8 bit), 1 Gsample/s
    • Transimpedance Amplifier (TIA) Input impedance of < 10 Ohm
    • Power consumption ~ 1.2 Watt
VULCAN
IC LAYOUT

Key Parameter of Vulcan

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Active Area</td>
<td>22 mm²</td>
</tr>
<tr>
<td>Power</td>
<td>~ 1.2 W</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>&lt; 10 Ohm</td>
</tr>
<tr>
<td>Input Bandwidth</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>1 Gsample/s</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>80 dB</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>3x 8 bit</td>
</tr>
<tr>
<td>High Gain</td>
<td>0.06 p.e./bit</td>
</tr>
<tr>
<td>Medium Gain</td>
<td>0.4 p.e./bit</td>
</tr>
<tr>
<td>Low Gain</td>
<td>8 p.e./bit</td>
</tr>
</tbody>
</table>
VULCAN SIGNAL MODES

Signal Modes – Small & Medium Signals

- First two signal chains
  - Parallel TIA input
  - Programmable gains
  - Combined input resistance $R \approx 5 \Omega$

Diagram showing small & medium signal mode with patent pending.
VULCAN SIGNAL MODES

• Signal Modes – Large Signals

Third signal chain
• Current > 20 mA
• TIA input saturates, ESD diodes open
• Voltage over diodes measured
• Combined input resistance $R \approx 5 \, \Omega$
LAB SETUP
OVERVIEW
BOARD CONCEPT

Verification Board
- Board for IC verification
- Every ADC can be measured
- Best RF/Impedance performance
- Optimized for verification measurements

Socket Board
- Socket can be populated on board
- For measurement of many samples
- Limited performance measurements
- Functional checks

PMT Board
- For direct usage with PMT
- Protection circuit
- All 3 ADCs connected

Main Board
- Logic analyser connection
- Power supply connection
- JTAG interface
- DC measurements
- Samtec board to board connectors

System Board
- All 3 ADCs connected
- Protection circuit
- Reference design for system implementation
VERIFICATION BOARD CONCEPT

Main Board

Verification Board or
Socket Board or
PMT Board or
System Board
VERIFICATION BOARD

Vulcan

Analog Connectors
VERIFICATION BOARD

Samtec LVDS Digital Connector

Samtec Supply Connector
VERIFICATION BOARD SETUP
SOCKET BOARD SETUP

• Yamaichi Socket for functional testing
For Verification Software Framework:

**Run Measurement**
Devices are initialized, Chip programming environment is set up, all testcases that should be executed are started from this Matlab file and the parameters for the testcases (Temperatures, Voltages…) are defined here.

**Testcases**
Each testcase is started with the parameters given, measurement equipment and the chip is programmed and the measurement is executed.

**Measurement Results**
Measurement results from all executed testcases are stored in a new measurement data folder, the folder name is containing the execution Date.

**Output Formats:**
- Excel, including template, plots and raw data
- Plots .jpg
- Plots .fig
- Raw data
VERIFICATION RESULTS OF VULCAN ES2

• LVDS Data Lines
VCO AND PLL INVESTIGATIONS

- VCO running @4GHz
- Reference clock for PLL @31.25MHz
- Measurement VCO/4 -> 1GHz
CLOCK AND PLL INVESTIGATIONS

- **VCO Tuning Range @ 25°C**

- **PLL Phase Noise @ 25°C**
TRANSIMPEDEANCE AMPLIFIER INPUT IMPEDANCE
TIA Low Gain

2. Low Gain setting -> 620mV / 10mA -> slope -62Ω
TIA High Gain

3. High Gain setting → 1200mV / -2mA → slope -600Ω
Full Range ADC Characteristic (low Gain)
Full Range ADC DNL (low Gain)

Vulcan 2.0 RX1 ADC + TIA DNL (Differential nonlinearity) Measurement ($TIA_{Input}$ to $ADC_{Output}$)

- Input Current vs. $ADC_{Max} = \sum_{i=0}^{N_{max}} ADC_i$
- Polyfit function 1st order, Slope $\Delta = 49.54$ dB
- Linear Interpolated Values taken for DNL Calculation:

$$DNL_\Delta = \frac{DAC_{Input}}{DAC_{Output}} - 1$$
Full Range ADC INL (low Gain)

Vulcan 2.0 RX1 ADC + TIA INL (Integral nonlinearity) Measurement ($TIA_{Input}$ to $ADC_{Output}$)

Input Current vs. $ADC_{Output} = \frac{\text{Input Current}}{\text{Gain}}$

Polylift function 1st order, Slope $\Delta = 0.50\,\text{INL}$

Linear Interpolated Values taken for INL Calculation

Ideal Values taken for INL Calculation

Absolute INL Errorbar

INL, $\Delta = \frac{\text{INL}}{\text{Gain}}$
Sinewave Signal 1 MHz (700Msamples/s)
ENOB without Distortion = 6.25
ENOB with Distortion = 6.17

\[ \text{ENOB} = \frac{\text{SNR} - 1.76 + 20 \times \log_{10} \left( \frac{\text{Fullscale}}{\text{Usedscale}} \right)}{6.02} \]
10ns Pulse ADC Output

Vulcan 2.0 ADC 10ns Pulse Output
Vielen Dank!