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The processing chain of the wide bandgap semiconductor SiC – How small steps enabled a mature technology

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ABSTRACT

This work paper was presented as a keynote lecture at the international conference on diamond and related materials in Lisbon (Portugal) in the year 2022. This paper summarizes in the first part the processing chain of the semiconductor material SiC from the raw material to epitaxially-ready wafers as they are used for electronic device manufacturing. In the second part a current research study, the reduction of the basal plane dislocation density in SiC crystal growth is presented. Among other defects, basal plane dislocations belong to the more severe structural defects in SiC with respect to degradation during electronic device operation. In the third part the applicability of X-ray topography to reveal dislocations and other structural defects in SiC is outlined in a review style.

1. Introduction

The wide bandgap semiconductor SiC comprises physical properties well suited for power electronic and novel photonic applications which go far beyond the standard electronic material Si but do not reach the extraordinary features of diamond. Compared to diamond, SiC exhibits a more feasible doping and crystal growth processing technology which is nevertheless extremely complex compared to the case of Si. After a long-lasting and challenging development period of more than four decades, SiC is currently taking over the power electronic device market segment from its semiconductor counterpart Si. Due to several similarities of the physical and chemical properties of SiC and diamond, some aspects of the long-lasting development time of the SiC process technology may be valuable for the ongoing transformation of semiconductor diamond from a niche into a broader industrial application field.

A major inhibiting factor during the development of today's SiC semiconductor device technology was the development of high quality, large area SiC wafers as carrier of the electronic circuits. For an extended review of the SiC growth process see [1]. For a review on the complete SiC technology chain from materials, through devices to systems it is referred to [2]. The first aim of this work is to look retrospectively at major obstacles and milestones during the development of the SiC crystal growth and wafer manufacturing technology. The second goal is to outline the current research target to further reduce the basal plane dislocation density. In this context the application of X-ray topography as a powerful characterization tool will be introduced.

2. The processing chain of the wide bandgap semiconductor SiC

The phase diagram of SiC is characterized by a peritectic decomposition of the material into carbon and a silicon rich silicon-carbon solution (Fig. 1a)([3,4] and references therein). Although solution growth may be performed to grow large SiC crystals [5–14], the process stability to grow long boules is still an unresolved issue. In fact, the physical vapor transport (PVT) method first introduced by Tairov and Tsvetkov in 1978 [15–21] and further developed in the early days by Ziegler et al. [22] has become the standard growth method. A number of research teams in academia and industry [15,16,18,22–33] paved the way for today's standard crystal diameters of 150 mm [34] and the next generation of even 200 mm in size [35]. The PVT process is usually operated at elevated temperatures above 2000 °C. In this temperature regime mainly carbon materials are applied inside the hot-zone of the growth

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machine. Although SiC provides many benefits for power electronic applications, the usage of SiC in blue and green InGaN-based light emitting devices strongly supported the development of a mature crystal growth technology in the late 1990 and early 2000 years.

As source material SiC powder with a grain size in the range on ca. 50 μm to several millimeter is used. For electronic device applications, purity plays an important role. SiC from the Acheson process usually needs a further purification and a mechanical processing in order to produce grains of regular shape. The application of liquid and gaseous precursors for chemical vapor deposition of high purity SiC source material or the direct synthesis of SiC particles from electronic grade Si and pure carbon particles offer another appropriate synthesis route for application of SiC source material in the PVT growth process. While the Acheson process offers the best potential for lower production costs, this SiC source may meet purity for the growth of nitrogen doped n-Type 4H-SiC. By trend, the direct SiC synthesis route results in by on to two orders of magnitude higher purity of the source materials compared to the Acheson route. Chemical vapor deposition exhibits the broadest palette of high purity precursors to synthesize SiC source materials which fulfill the specification for the growth of high purity semi-insulating SiC crystals. In particular the Acheson as well as the chemical vapor deposition route could demand crushing of bigger SiC pieces into the desired smaller SiC particle size distribution. Precaution to omit unintentional contamination of the SiC particles is obligatory. Almost independent of the processing route, higher SiC source purities go hand in hand in hand with higher production costs.

Usually, the PVT setup (Fig. 1c) is composed out of a growth chamber fabricated out of a tubular quartz glass surrounded by an induction heating coil. Alternatively, also a resistive heating system can be implemented inside the quartz tube or inside a stainless-steel autoclave. Note: By trend, resistive heating results in more homogeneous T-field distribution while inductive heating allows a simpler power control of the average temperature setting. The top and bottom flanges of the quartz tube are usually water cooled. The quartz embodiment may be either a water-cooled double wall tube system or an air-stream cooled single wall tube. The hot-zone is usually composed out of the graphite crucible and surrounded by an isolation made of carbon materials. In order to establish a mass transport of the Si, Si_2C and SiC_2 gas species

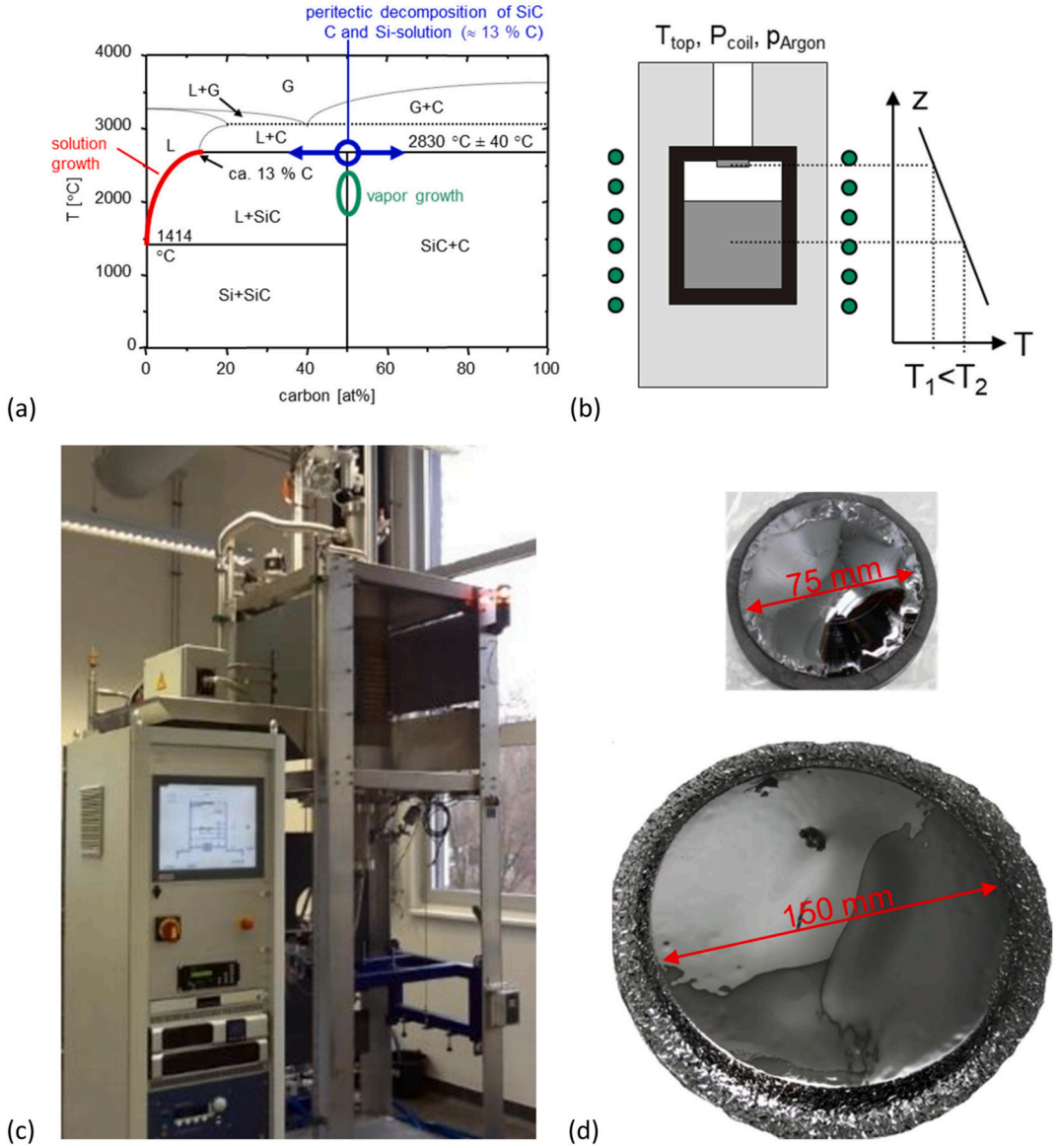

Fig. 1. (a) Phase diagram of SiC according to data of [3,4], (b) Basic scheme of the PVT hot-zone. (c) Image of a state-of-the-art PVT setup for industrial application (designed and manufactured at FAU). (d) Images of two SiC boules exhibiting a single crystalline diameter of 75 mm and 150 mm, respectively (grown at the crystal growth lab of FAU).

[36] from the SiC source to the growth interface, an axial temperature gradient needs to be established inside the growth cell (Fig. 1b). The design of the hot-zone components together with the heater system have a strong impact on the axial and radial temperature gradients inside the growth cell. A further degree of freedom in setting up the growth cell is the application of Ta and TaC coatings or even bulk parts inside the hot-zone [37–39]. For energy saving reasons, a proper choice of the carbon isolation materials is mandatory to run a cost-effective growth process. At growth temperatures above 2000 °C, the Si partial pressure exceeds the value of a few millibars and therefore may cause a significant unintentional decomposition of the graphite crucible parts. The identification of proper graphite materials qualities is an ongoing issue. The PVT growth process in the closed graphite crucible does not allow a visible access to growth chamber like known from the Czochralski process of silicon. Optical pyrometers are used to measure the temperature gradient on top and at the bottom of the crucible.

Using numerical modeling, the temperature field inside the crucible may be determined which is detrimental for optimizing the growth condition towards low radial temperature gradients [41–57]. A breakthrough of in-situ visualization of the PVT growth process was introduced by the application of 2D and 3D X-ray visualization tools [40,58–61]. Fig. 2 depicts a series of 3D-images acquired live during the PVT growth process at 2300 °C. While 3D in-situ visualization is a powerful tool for fundamental research in SiC crystal growth, the less complex 2D in-situ visualization process may be applied as a routing method in SiC boule production. Generally spoken: The further development of a growth process significantly profits from in-situ measurement techniques which monitor the physical and/or chemical processes going on. The typical growth rates and crystal lengths of the PVT process lie in the 120–180 μm/h and 20–40 mm range, respectively. Fig. 1d depicts two typical SiC boules with a single crystalline diameter of 75 mm and 150 mm, respectively, fabricated in the Crystal Growth lab of FAU.

Subsequent to the bulk growth process, grinding of the SiC boule is carried out to prepare a defined cylinder as well as the so-called flats or notch that indicate the substrate orientation. Here the challenge is related to the extreme mechanical hardness of SiC which confines the selection of processing tools. Wafer cutting is done by a multi-wire saw using stainless steel wire and a diamond slurry. As a modification also a diamond coated steel wire could be applied as it is standard for sapphire crystals for instance. As a novel alternative to the wire sawing, a method which makes use of a laser split technique has been introduced which significantly reduced the kerf loss. To smooth the wafer surface after cutting, lapping, polishing using a diamond slurry and chemical-mechanical-polishing (CMP) are applied to prepare an epitaxial ready surface (RMS value of typically <0.2 nm).

Today, nitrogen doped n-type 4H-SiC wafers with a diameter of 150 mm are mainly used in SiC-based power electronics. Since the presentation of the first crystals with a diameter of 200 mm [35] almost a mature technology has been developed. Standard SiC wafers with a diameter of 150 mm and even 200 mm exhibit a remarkably high crystalline quality. The micropipe density is basically zero. The usable wafer area for electronic devices fabrication lies in the high 90 % range. Concerning production yield no data are available. However, the availability of a quite broad spectrum of SiC wafer qualities indicates that there is still a reasonable room for process optimization. N-type 4H-SiC wafers of medium to high quality exhibits a threading screw and basal plane dislocation density of well below 10^3 cm^{-2}. So far, every significant increase of the wafer diameter was accompanied by new critical technologic questions which needed a three to five years [5–14] period to find the right solutions. With the development of wafers with a diameter of >100 mm the handling of residual strain in the material which causes a great wafer-bow and -warp popped up. Current hot topics in R&D topics of bulk growth of SiC include the increase of the process yield. At which stage a further enlargement of the crystal diameter towards 300 mm will be pushed forward will strongly depend on its potential to reduce device production costs. At least for large area power devices the percentage of usable area of a wafer would be increased by such step.

3. Crystalline defects in SiC - how small steps enabled a mature technology

Dislocations are in many semiconductor materials the main source for device degradation and failure. Micropipes in the active zone of an electronic devices usually cause an immediate breakdown [62]. Basal plane dislocations (BPDs) proved to be destructive for the operation of bipolar diodes because of the generation of stacking faults which extend during device operation under forward bias [63]. In addition, BPDs increase the leakage current in MOSFETs or JFETS [77,78] devices. Threading edge (TED) and threading screw dislocation (TSD) as well as mixed type dislocations in the substrate and epitaxial layer alter the performance of electronic devices like Schottky diodes and Metal-Oxide-Field-Effect-Transistors (MOSFET) [64,65] and should be reduced in their density as well.

3.1. Micropipes

The perhaps most famous line defect in SiC is the so called micropipe [66] which is a screw dislocations exhibiting a large burgers vector of a multitude of 3 to ca. 10 of the c-lattice parameter [29,67]. Micropipes are mainly aligned along the ⟨0001⟩ direction and may also exist as

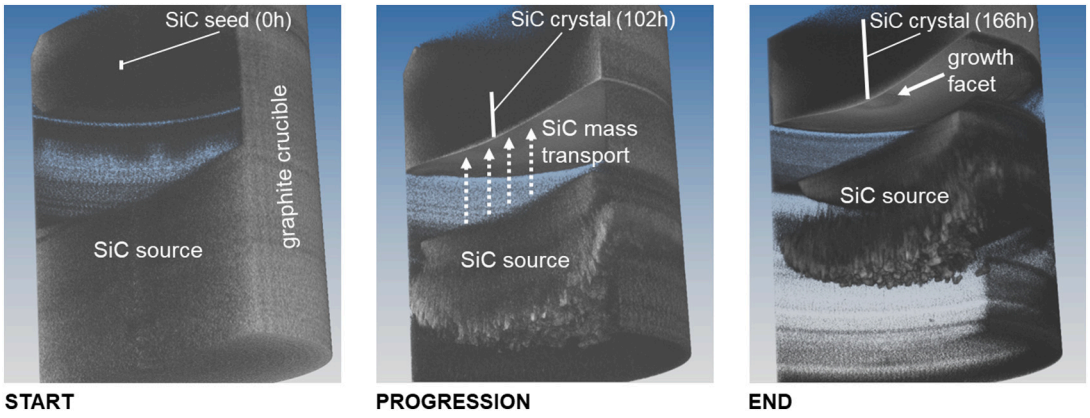

Fig. 2. Series of three in-situ 3D computed tomography images of the interior of the PVT growth cell at $T > 2000$ °C. Using this measurement technique, tracking of the evolution of the crystal growth interface including shape, size and position of the facet are possible (see also [40]). The thicknesses of the shown SiC seed/crystal images in the central area are approximately 1 mm (start), 13 mm (progression) and 25 mm (end), respectively.

mixed type dislocation with a deflection from the c-direction [68]. There are a number of possible origins for the appearance of micropipes. Micropipes often stem from the SiC seed and extend into the newly grown crystal. Another and today perhaps most important source for micro pipes are macroscopic defects like polytype changes, inclusions (=carbon particles or silicon droplets) and voids (=decomposition cavities). The inhibition of un-intentional polytype switches during the seeding process or at a later growth stage of the growth process may be identified as the most effective effort to maintain a low or even zero micropipe density in the SiC boule [24,30]. Once the generation of new micropipes in the growth process is suppressed, the termination of existing micropipes moves into the foreground. Near equilibrium conditions in the initial growth phase during seeding are important to reduce the micropipe density in the grown SiC boule [69]. In the case of sublimation epitaxy of SiC a kind of micropipe filling was reported [70]. By the choice of the right surface step height during growth, micropipes dislocations may be deflected into the basal plane. Crystal growth of SiC on tilted or even perpendicular surfaces with respect to the basal plane is another way to diminish the occurrence of micropipes [71–73].

3.2. Basal plane dislocation

In hexagonal polytypes of SiC, basal plane dislocations (BPDs) are expressed by a burgers vector along the a/3 < 11$\bar{2}$0> direction and a dislocation line parallel to the basal plane. Since the dislocation line of this defect lies perpendicular to the growth direction, in contrast to MPs the growing crystal does not inherit the defect distribution of the seed. However, stress induced into the crystal either during or after growth can activate the <11$\bar{2}$0>{0001} slip system and in turn promotes generation and propagation of BPDs if a relaxation process occurs [74–76]. At growth temperatures >2000 °C, the activation energy for this slip system only amounts to about 1 MPa [44]. These stress limits are easily reached due to the characteristics of PVT growth, where several sources of stress exist. Therefore, in contrast to the complete elimination of MPs even state-of-the-art 4H-SiC wafers currently exhibit BPD densities in the range of 10^2–10^3 cm^{-2}. As mentioned above, BPDs are known for increasing the leakage current in MOSFETs or JFETS [77,78]. Consequently, the reduction of BPD density is subject of current research.

Another mechanism of BPD generation besides stress is the conversion of TEDs into BPDs during crystal growth. TEDs are dislocations arranged parallel to the growth direction, similar to MPs. However, in contrast to the screw-type MPs their burgers vector aligns perpendicular to the growth direction, resulting in an edge dislocation. Both BPD to TED and TED to BPD conversion is possible [79,80]. The latter one is preferable though, since TEDs have a comparatively benign effect on device performance. The conversion rate hereby depends on the degree of step-bunching on the growth interface. With an intensified step-bunching, the conversion rate increases. However, even if all BPDs are converted into TEDs during the first few layers of crystal growth, stress will still lead to BPD multiplication, for example through double-ended or single-ended so-called hopping Frank-Read sources [81,82]. Therefore, all sources of stress have to be minimized. Several different origins of stress are of importance, requiring different approaches. First, the difference in the coefficient of thermal expansion (CTE) of the different materials utilized in PVT growth has to be considered. It can be assumed that a crystal will grow in a stress-free manner at growth temperatures, since the thermal energy will promote dislocations generation to adapt to occurring strain immediately. A crystal fixed to graphite parts like the seed holder, or the crucible wall will experience stress during cooldown due to the different CTEs of SiC and graphite. This in turn will lead to the generation of BPDs before reaching the ductile-brittle transition temperature of 1050 °C [83]. Secondly, for mass transport inside the graphite crucible temperature gradients are necessary. These temperature gradients inside the crystal will bend the basal plane and generate BPDs to accommodate the resulting strain. Once the crystal cools down these BPDs will induce further stress [75,84]. While axial temperature gradients are necessary for the growth rate, radial temperature gradients are selected in such a way to promote a convex growth interface. Note: a convex growth interface would result in the generation of additional dislocations as well as occasional unintentional SiC polytype switches. Similar to axial temperature gradients, they will induce stress during the cool-down phase and therefore need to be kept at a minimum while still achieving a convex crystal shape. The fine control of temperature gradients becomes increasingly more important if bigger diameters of crystals are to be grown, since the radial gradients have a higher impact overall.

Another additional source of stress in PVT growth can be caused by inhomogeneous doping. In SiC, nitrogen replaces the carbon lattice site and leads to reduced lattice constants in the crystal. This leads to strain during the growth phase. However, nitrogen doping in SiC also modifies the CTE of hexagonal SiC [85]. During the seeding phase of PVT growth adsorbed nitrogen gas species can release from the highly porous graphite isolations and consequently lead to a sharp increase of the doping concentration until this adsorbed nitrogen is depleted. As a result, the initial seeding portion of a crystal is often stressed to a high amount [86]. It is possible to compensate for the initially higher nitrogen gas concentration in the graphite crucible with a finely tuned gradual increase of the nitrogen gas flux during the start of growth. The adsorbed nitrogen species in the graphite parts can further be reduced by purging steps prior to growth. Moreover, the utilized graphite parts should be of high purity in the range of 6 N. If semi-insulating SiC is required such as in the processing of GaN on SiC devices, the need for purity is elevated into magnitudes of 7 N to 8 N.

Besides the doping, the CTEs of different materials inside the growth chamber and the temperature gradients, the shape of the growth interface itself can induce stress into the crystal. It was demonstrated numerically and experimentally that from the shoulder region of a crystal BPD arrays can form and propagate into the crystal. The higher the curvature of the growth interface, the more arrays of BPDs will form [76,87]. Fig. 3 illustrates the alignment of the oval shaped BPD etch pits into BPD arrays. The occurrence of these arrays can be reduced by minimizing the amount of stress the crystal experiences during growth, proving the correlating nature between stress and BPD density.

To show this correlation, two 4H-SiC crystals A and B of 100 mm diameter were grown via PVT with comparative growth parameters such as pressure, nitrogen doping and growth temperature. The pressure in the growth phase was set between 5 and 30 mbar, and the growth temperature was maintained between 2050 and 2100 °C. This temperature is measured on top of the graphite crucible. As mentioned before, the nitrogen flux is adapted to compensate the initial nitrogen surge from the graphite isolation. It was ramped up from zero during the initial decrease to ambient pressure, reaching to 5 % of the argon gas flux. This adaptation prevents a sharp increase in nitrogen doping, instead resulting in a smooth transition of the doping concentration between the seed and the newly grown crystal. A seed was taken from crystal A for the use in the growth of crystal B. This achieved a similar doping

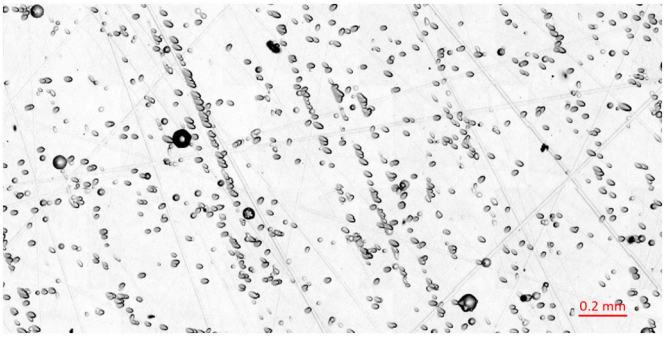

Fig. 3. KOH-etched Si-face of a 4H-SiC wafer with visible BPD arrays.

concentration of the seed for crystal B compared to the rest of crystal B. The off-axis angle of both seeds amounted to 4° towards the <11$\bar{2}$0> direction.

Besides minimizing the impact of the nitrogen and therefore reducing the stress, the growth cell of crystal B has been modified to tailor temperature gradients in such a way that both the radial and the axial temperature gradients are reduced. The axial temperature gradients inside the crystal were determined numerically and amounted to be 33 K/cm and 25 K/cm for crystal A and B, respectively. The same was done for the radial temperature gradients, amounting to 4.0 K/cm and 1.8 K/cm for crystal A and B, respectively. Besides reducing the stress due to temperature differences in the crystal, the reduced radial temperature of the growth cell of crystal B also leads to a decrease of the convex growth interface shape. To reduce the impact of the graphite seed holder on the seed due to differences of the thermal expansion coefficients of both materials, its thickness was reduced by 85 %. The last modification for the growth of crystal B consists in an adaption of the growth cell in such a way that the crystal does not connect to the graphite crucible's side walls.

Both crystals A and B were sliced and the resulting wafer polished for characterization of the defect distribution. For this, several characterization methods were applied. X-Ray topography (XRT) is a powerful non-destructive method to investigate the bow of the basal plane and the defects in the crystal, such as MPs, TEDs or BPDs. The measurements of two wafers A1 and B1 taken from crystal A and B were carried out by the Fraunhofer department IISB in Erlangen (Germany), employing a Rigaku XRTmicron advanced X-ray topography setup. Raman spectroscopy was used to determine the doping concentration via the optical-phonon plasmon couple (LOPC) mode of all sliced wafers from both crystals. A Horiba LabRAM HR Evolution confocal Raman microscope utilizing a 532 nm laser in combination with an 1800 gr/mm grating and a magnification of 100 times was employed. The LOPC's peak position can be used to estimate the doping concentration [88]. The knowledge of the nitrogen doping level allows a more accurate numerical calculation concerning the CTE of 4H-SiC [85]. Consequently, the model can implement the doping concentration into the stress calculations of the crystal. At last, wafer A1 was etched with molten potassium hydroxide (KOH) with our in-house KOH-etching setup. This was done to reveal the etch pits and verify the type of defects seen in the XRT measurements. The etching process was carried out for 5 min at 520 °C.

Fig. 4a and b illustrate X-ray images taken during the PVT growth of crystal A and B while still inside the graphite crucible. The growth interface of crystal B exhibits a significantly decreased curvature compared to the one of crystal A, a result of the hot zone modifications and the reduced radial temperature gradients. As a consequence, the size of the shoulder region has been decreased. This should lead to less BPD array generation during the growth, as observed by Nakano et al. [76].

Fig. 4c and d show the shear stress in the region of crystal A and B as marked by the dotted rectangle after the crystal has cooled down to room temperature. The temperature gradients, the different CTEs of the materials, the reduced seed holder thickness and the impact of the nitrogen doping concentration as determined by Raman measurements are taken into account. This region is the same as the one the wafers A1 and B1 were cut from. The reduction of the shear stress between the two wafers is obvious, reaching a maximum of 18.0 MPa in case of wafer A1 and a maximum of 8.3 MPa in case of wafer B1, respectively.

To investigate if these modifications to the growth process parameters of crystal B had a significant impact on the occurrence of BPD arrays, XRT measurements of wafer A1 and B1 were conducted. The results are illustrated in Fig. 5. The scans were taken with a 11$\bar{2}$0 reflex. Wafer A1 is characterized by distinct lines appearing in similar distances perpendicular to the off-cut direction of the wafer. To verify if these features are a result of stacking faults or BPDs, wafer A1 was KOH-etched. The results can be seen in Fig. 5c and d. The oval shape of the etch pits are clearly identifying the lines as BPD-arrays. In contrast to wafer A1, wafer B1 shows no such features at all. The defect cluster in the center of both wafers was identified as an accumulation of MPs. These were present in crystal A and were caused by an early 4H/6H/4H polytype switch. Since all MPs in the seed will get inherited by the growing crystal and the seed of crystal B was a wafer taken from crystal A, it was to be expected that both wafers A1 and B1 express this defect cluster. The distance between the arrays depends on the initial lattice plane bending of the SiC seed at the beginning of the growth process and was calculated to be approximately 0.38 ± 0.10 mm along the c-axis. A similar magnitude was reported by Sonoda and Nakano [74,76]. The low contrast region on the right side in Fig. 5b is a consequence of the basal plane bending of the wafer. The basal plane bending can be determined with the help of the XRT measurements. It amounts to a radius of 12 m in case of crystal A and 26 m in case of crystal B. The increase of the radius for crystal B further proves that the modifications of the growth process led to a reduced amount of stress during and after the growth. 26 m is still a relatively high amount of bow for a 4H-SiC wafer (for high quality SiC crystal, radii of up to 800 m have been reported in literature [89], typical values of commercial 150 mm wafers lie in the order of 300 m). However, apparently it is enough to completely suppress the formation of BPD arrays. The BPD density can also be determined with the information from the XRT mappings. Wafer A1 exhibits a BPD density of approximately $>10^4$ cm^{-2}. The BPD density of wafer B1 is observed to be approximately 10^3 cm^{-2}, so a decrease of one order of magnitude. It has to be noted that the growth rate of crystal

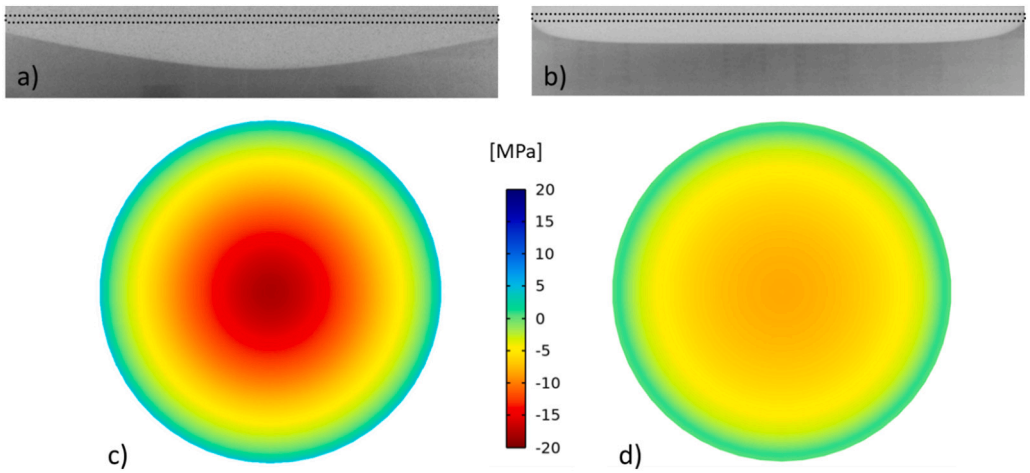

Fig. 4. X-ray images taken during PVT growth of a) crystal A and b) crystal B. The numerical calculation of the stress present in the wafers A1 and B1 cut from crystal A and B (as marked in a) and b)) are illustrated in c) and d), respectively.

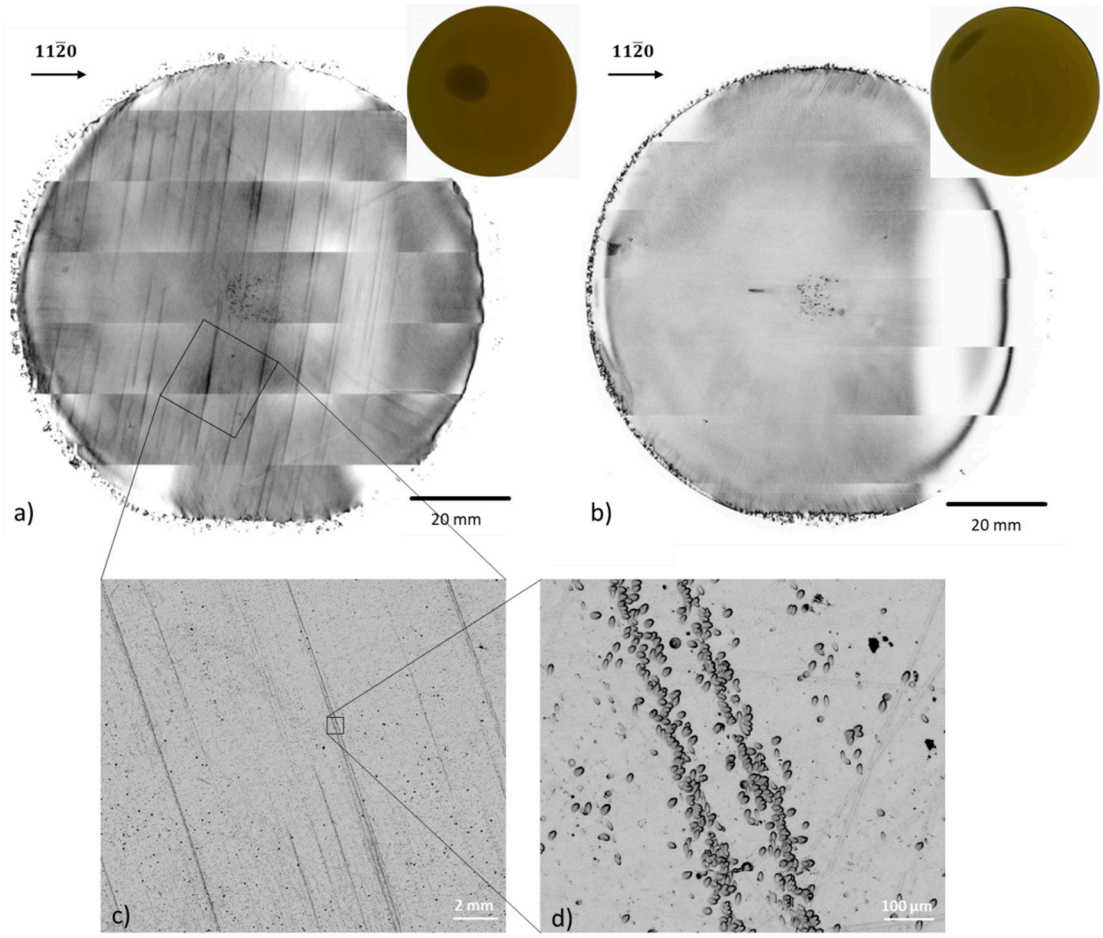

Fig. 5. XRT mappings of a) wafer A1 and b) wafer B1. The inset shows an optical scan of the respective wafers. c) and d) show magnified areas of the KOH-etched wafer A1 including BPD arrays.

A amounted to 172 µm/h, almost two times as fast as the one of crystal B with only 90 µm/h. This is a result of the decreased axial temperature gradient while keeping the growth temperature and the growth pressure at similar values.

As a conclusion, the connection between stress and BPD defect density and also array formation was demonstrated. By reducing the axial and radial temperature gradients, reducing the shoulder width of the growth interface, controlling the doping concentration, keeping the contact to materials with different CTE values as low as possible and consequently keeping the shear stress acting on the crystal to a minimum, the formation of BPD arrays can be suppressed. A good compromise between the growth rate and the axial temperature gradient has to be found. Minimizing the radial temperature gradients has to be implemented carefully to prevent a concave growth interface and cause a possible polytype switch. The absence of any BPD array in crystal B suggests that these modifications led to a stress field below a critical value needed for the formation of such arrays.

3.3. Unintentional SiC polytype switches

As pointed out above, unintentional SiC polytype switches have been identified as a source of various dislocations. Polytype switches occur in SiC crystals grown along the (0001) or (000−1) crystallographic direction because of the low stacking fault energy present in SiC. Large basal plane terraces at the growth interface caused e.g. by step-bunching enable unintentional polytype switches if the growth conditions are not precisely aligned to the anticipated polytype. In power electronic application the 4H-SiC polytype is applied. 4H-SiC growth is favored in the case of high supersaturation at the growth interface, a more carbon rich gas phase compared to 6H-, 15R- and 3C-SiC, an average growth temperature around 2000 to 2150 °C and nitrogen doping, to name a few important impact factors. For a more in-depth going discussion it is referred to [1].

4. X-ray topography as a powerful characterization tool of line defects in SiC

X-Ray topography can be differentiated into two types. Conventional XRT is performed with laboratory-sized setups with similar sized X-Ray sources. Modern systems have pixel sizes of around 2–5 µm. The second type are systems with a synchrotron radiation source. Synchrotron radiation has the advantage of long beam-lines, low divergence and resolutions of below 1 µm. This resolution is mainly limited by the type of detector. The theoretical resolution lies in the range of 0.04 µm/cm, where cm is the distance between the detector and the specimen. The disadvantage is the high cost of such systems and the availability of beam time. The underlying principle of both types is the same however. A sample is exposed to X-Ray radiation and will diffract the radiation according to Bragg's law. A perfect crystal with no defects will diffract an incoming beam homogeneously, therefore giving a homogeneous intensity distribution. However, defects such as dislocations will change the diffraction angle and therefore the intensity profile. This way, numerous defects in the crystal lattice can be detected, as long as the crystal lattice is strained. XRT can either be conducted in reflection geometry (Bragg-case) or transmission geometry (Laue-case). A more elaborate description of the XRT methodology can be read about

elsewhere [90].

The application of XRT is used extensively for the characterization of defects in SiC since individual dislocations can be observed if the defect density is low enough. To correlate the exact intensity profile with the respective defect type, extensive research has been conducted. This includes TSDs and MPs [91,92], TEDs and low angle grain boundaries (LAGB) [93,94] and BPDs [95]. The BPD arrays mentioned before were characterized utilizing XRT by Sonoda and Nakano et al. [74,76]. Sonoda furthermore investigated the interaction between TSDs and BPDs during the growth. XRT allows to utilize different kind of reflexes such as $11\overline{2}\overline{8}$ and $1\overline{1}0\overline{7}$. Depending on the type of reflex, either BPDs or TSDs can be distinguished. This allowed the authors to observe the formation of BPDs at the outcrops of TSDs on the growth interface. They argued that TSDs impose a stress field during the growth, promoting the nucleation of BPDs. Therefore, the density of TSDs and BPDs can be seen as closely linked. To reduce the BPD density, TSDs also have to be minimized as much as possible. This type of screw dislocations normally is introduced to the crystal either by the seed, but can also nucleate in the initial seeding phase due to stacking faults [96].

As another example and as mentioned before, BPDs can be converted into TEDs and vice versa. This was directly observed by Ohno et al. who used XRT to observe the BPD propagation in homoepitaxial layer growth. The authors detected BPD to TED conversion, TED to TED propagation and BPD to BPD propagation in newly grown layers [97] (see Fig. 6). Kallinger et al. reported an influence of the surface roughness on the conversion rate of BPDs to TEDs [80]. The main driving force was suggested to be the minimization of the dislocation line energy during growth, in contrast to the findings of Ha et al., who defined the image force of the dislocation as the leading influence on the conversion rate [79].

Another interaction between BPDs, TEDs and TSDs was shown by Chen et al. [98]. They demonstrated with XRT measurements that BPDs can be pinned by TSDs, leading to bowed out dislocation lines of BPDs. However, not all TSDs had such an impact on BPDs. The proposed model suggests a cross slip of the segment of the BPD interacting with the TSD. This segment can glide on the step introduced by the TSD by prismatic glide and realign with the BPD line as a super jog. However, low angle grain boundaries (LAGB) consisting of a multitude of TEDs cannot be overcome by BPDs. As a consequence, at LAGBs aggregations of BPDs were observed.

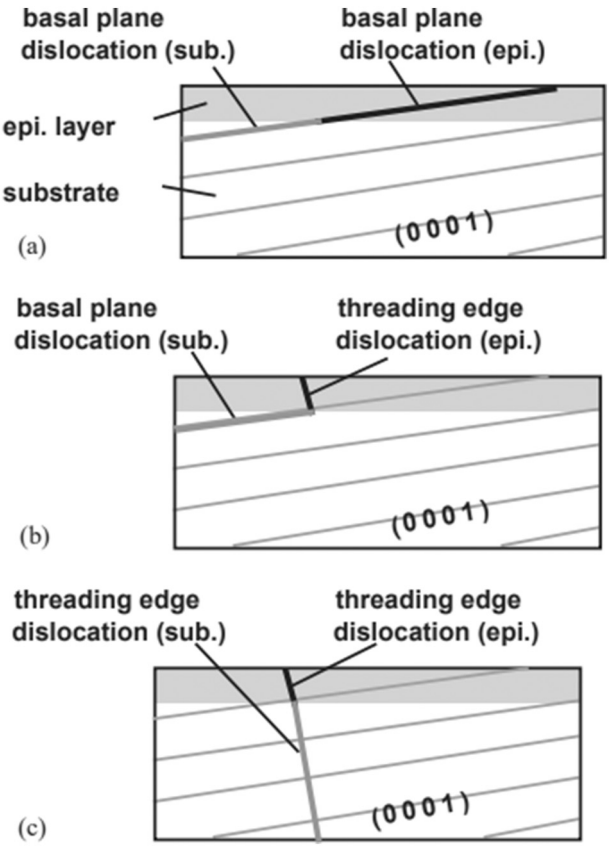

Fig. 6. Possible propagation of TEDs and BPDs during homoepitaxial growth. (Reproduces from [97] with permission.)

Not only BPDs and TEDs can be deflected during the growth. Dhanaraj et al. observed a reduction of 1c TSDs (burgers vector height of one unit cell in c-direction) during CVD growth of SiC as well as the known conversion of BPDs to TEDs [99]. TSDs can form growth islands during the initial seeding phase due to their tendency to create an unlimited supply of steps. These islands can interact with macro-steps on the growth interface and the TSD can get deflected either in a partial or fully horizontal direction. In case of a full horizontal deflection the TSD gets pulled towards the growth interface due to the image force. This leads to a mixed TSD, where the burgers vector exhibits both an a and c component. The determination of the dislocation's burgers vector and its components is another use case for XRT. Shinagawa et al. investigated the ratio of pure- and mixed-type TSDs in PVT-grown 4H-SiC crystals. They prepared longitudinal slices along the $(11\overline{2}0)$ direction and utili0/zed a conventional XRT system in transmission geometry with an exhaustive amount of different reflexes. Depending on the reflexes a wide variety of burgers vectors for TSDs was uncovered. Only approximately 10 % of TSDs exhibit a pure-type screw character with an exclusive c component of the burgers vector. TSDs tend to propagate perpendicular to the growth interface, which due to its convex shape leads to TSDs expressing an angle towards the c-axis [100]. The movement of MPs in respect to the crystal facet and next to it was investigated by Arzig et al. [101], leading to a similar conclusion of propagating TSDs (or MPs) perpendicular to the growth interface. MPs inside the flat crystal facet did not exhibit nearly as much horizontal movement as the ones outside the crystal facet on the crystal shoulder region [101].

Since the components of the burgers vector can be determined with XRT, it is also possible to gain insight into the origin of the formation of dislocations. One example was shown by Shioura et al., where the initial seeding interface is examined in detail with XRT and Raman measurements [84]. The authors examined the defect distributions in PVT growth at the initial growth interface. They discovered BPD dislocation networks in the seed and determined via a follow-up experiment that these BPD networks must have formed after growth. They could demonstrate via XRT that the newly formed BPDs in the seed crystal point towards the growth interface and not towards the seed crystal. The reason for the induced stress was proposed to lie in axial temperature gradients and the resulting stress due to different expansion of the crystal lattice. The propagation of the BPD networks into the seed crystal was implied to be an interaction between BPDs and point defects such as vacancies.

Besides the type of defects, XRT is also useful to determine the different ways a crystal relaxes either during the cooldown-phase of PVT growth or also during annealing [102]. Guo et al. researched the impact of prismatic glide on the defect distribution in PVT-grown crystals [103,104]. While the basal plane requires less energy for dislocation glide due to the small a lattice spacing, the prismatic glide system is relevant as well, especially at bigger diameters of grown crystals. By increasing the diameter of the crystal, the total temperature difference between the center and the edge increases as well, resulting in strain in the crystal. Therefore, the possibility for prismatic slip increases towards the edges of a crystal. This effect was observed via XRT by Guo et al. They found prismatic dislocations and explained this with a gliding BPD segment of a TED due to high thermal stresses at the outer regions of a commercial 150 mm 4H-SiC wafer and proposed a model with good agreement.

XRT can also be employed to investigate the multiplication mechanisms of defects in crystals. The Frank-Read sources is a well-known phenomenon where a dislocation such as a BPD gets pinned between two immobile dislocations, for example TSDs or TEDs. Under sufficient stress, the BPD will bow out and form a circular dislocation line, recombining behind the two TSDs. The BPD between the two TSDs remains. This process can then start again as long as the stress is high enough to promote the initial bending of the dislocation line into at least a half circle between the two TSDs. In SiC, also a so called hopping or single-pinned Frank-Read source was observed [105]. This process was observed directly with the help of synchrotron XRT.

The results of the extensive usage of XRT for the characterization of dislocations in SiC allowed to identify the critical parameters for the formation and propagation of these respective dislocations such as temperature gradients, different CTEs of different materials or even the same material with different doping concentrations, Si to C rations for the conversions between BPDs and TEDs, the connection between TSDs, TEDs and BPDs and the consequent need to reduce every type of dislocation. As a result, the defect density of commercially available wafers is low enough to create power electronics with an acceptable reliability.

5. Summary

The maturity of today's SiC processing technology enables its application in customer products. The development of large area (150 mm and 200 mm wafers) of high crystalline quality over the last ten to 15 years represents one of the main pillars. As a matter of fact, since initially unavoidable obstacles like the MP defects were diminished and because the BPD density was significantly reduced in recent years of ongoing research and development, is a clear sign that certain technologic developments need time. In a retro-perspective view, small steps in the growth process development as pointed out throughout this article paved the way for SiC to be now the bright semiconductor star in the power electronic world. With respect to diamond, the successful process development of SiC bulk growth strongly indicates that today's limitations in the large bulk growth process of diamond also may be overcome in conjunction with an incessant further development where progress may depend on a series of small steps.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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