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# Lateral Electrochemical Metallization Cells for Reconfigurable Interconnect Systems

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**ABSTRACT** Lateral electrochemical metallization (ECM) cells are fabricated with a combined spacer/damascene process. The process allows the realization of nanoscale geometrical distances between the two electrodes independent of lithography. Such lateral ECM cells are an essential part in a reconfigurable interconnect system that may yield a strongly increased connectivity in artificial neural networks. The lateral cells show memristive properties comparable to vertical cells with switching voltages in the range of  $-1.5$  V to  $2.5$  V. The influence of electrode line edge roughness on SET kinetics of such lateral cells is investigated via kinetic Monte Carlo simulations, finding a minor influence on SET time variability.

**INDEX TERMS** Electrochemical metallization (ECM), lift-off, memristor, neuromorphic hardware, RRAM, ReRAM, line edge roughness, Kinetic Monte Carlo.

## I. INTRODUCTION

The human brain is the most complex and most sophisticated information processing system known. Due to a massively parallel operation, it is able to process huge amounts of data with very little energy consumption. This extremely parallel information processing is made possible by a very high degree of interconnects between neurons that can be set and reset autonomously during learning processes. Demonstrating a similarly complex yet flexible interconnectivity is a major challenge of artificial neural networks.

Flexible setting/re-setting of interconnects can be realized using, e.g., field-programmable gate arrays (FPGAs) [1], [2], [3]. Recently, neuromorphic circuits based on FPGAs were demonstrated and employed for a number of applications including recognition of handwriting [12], classification of musical notes [2], and biomimetic pattern generation [3]

(for further applications see [13]). However, the gate configuration of FPGAs is not remanent and additional storage is necessary. While high-capacity flash memory can be manufactured by 3D integration [14], the combination of a flash memory and an FPGA increases space and power requirements.

As an alternative, reconfigurable circuits based on a combination of CMOS and memristive crossbar structures have been investigated in view of realizing field-programmable interconnects [7], [8], [9]. In particular, electrochemical metallization (ECM) materials [4], [5], [6] have attracted a great deal of attention for such reconfigurable structures: the functionality of a synapse can be mimicked since a conductive filament (CF) of adjustable strength can be grown in between two metallic electrodes (consisting, e.g., of platinum and copper) with an appropriate electric field; reversing the field, the interconnect can be erased [15], [18]. Transistor-free

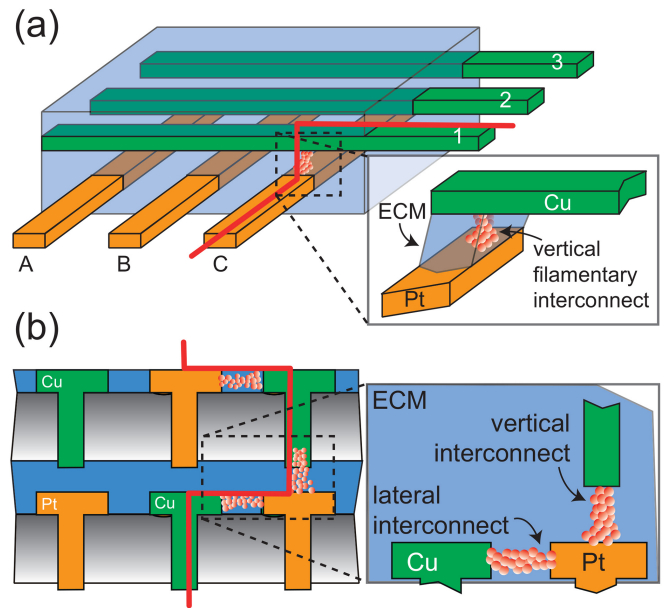
crossbar memristors based on metal-oxides were applied to the computation of an analogue of vector-matrix multiplication [16]. Moreover, crossbar structures consisting of several crossbar layers have been fabricated [7], [8], [9], [10], [11].

In such multilayer memristive crossbar devices sneak current paths can form. These are indirect current paths through non-selected cells during READ/WRITE operations, increasing the power consumption and causing voltage drop along the line [25]. One solution to this problem are selector devices placed at the memristor-crossbar junction [26], [27]. By design, these selectors suppress conductivity for all indirect connections between two crossbar lines. This simultaneously limits any memristive cell-to-cell interconnectivity since the suppressed sneak paths are the only available mechanism for behavior of this type.

By comparison, in a network of biological neurons, many neuron-to-neuron connections of different strength are possible. To emulate this interconnectivity in memristive cell arrays, we suggest to shrink the line-shaped electrodes to a geometry resembling mushrooms, consisting alternately of, e.g., platinum and copper, placed on a quadratic lattice. The top parts of the mushroom-electrodes are embedded into an ECM material and the stems are connected to a buried CMOS layer that allows applying the three voltage levels  $-V_{dd}$ , 0 and  $+V_{dd}$  to each mushroom-electrode independently.

This layout enables formation of CFs between any two adjacent electrodes in the 2D array, providing interconnectivity at the cell level. The CMOS layer offers additional flexibility compared to addressing by conventional crossbar schemes, as applying potential to Cu electrodes along a crossbar line will always select two electrodes adjacent to any selected Pt electrode simultaneously. On top of the proposed 2D system, additional layers may be fabricated, allowing connections to be SET and RESET both laterally and vertically as illustrated in Fig. 1 (b). The mushroom-shaped electrodes also facilitate alignment between layers, as the thin stem can be positioned anywhere on the larger cap of the opposing electrode in the previous layer.

A central ingredient of such a 3D interconnect system is the realization of low-resistivity CF growth in-between two lateral electrodes. Whereas lateral filamentary growth has recently been investigated [19], [20], [21], the separation between the electrodes is on the order of a few hundred nanometers and hence far larger than in typical vertical ECM cells. The reason for this is that in the fabrication of those lateral ECM cells, two lithography processes are necessary leading to variability issues and requiring sufficient overlay alignment tolerances. In contrast, in vertical cells, the separation between the two electrodes is defined by the unprecedented film thickness control of state-of-the-art deposition processes (e.g., sputter or atomic layer deposition). As a result, in existing lateral ECM cells large voltages (e.g., 30 V in [21]) are required for the growth of a CF, prohibiting nanoscale dimensions and high integration



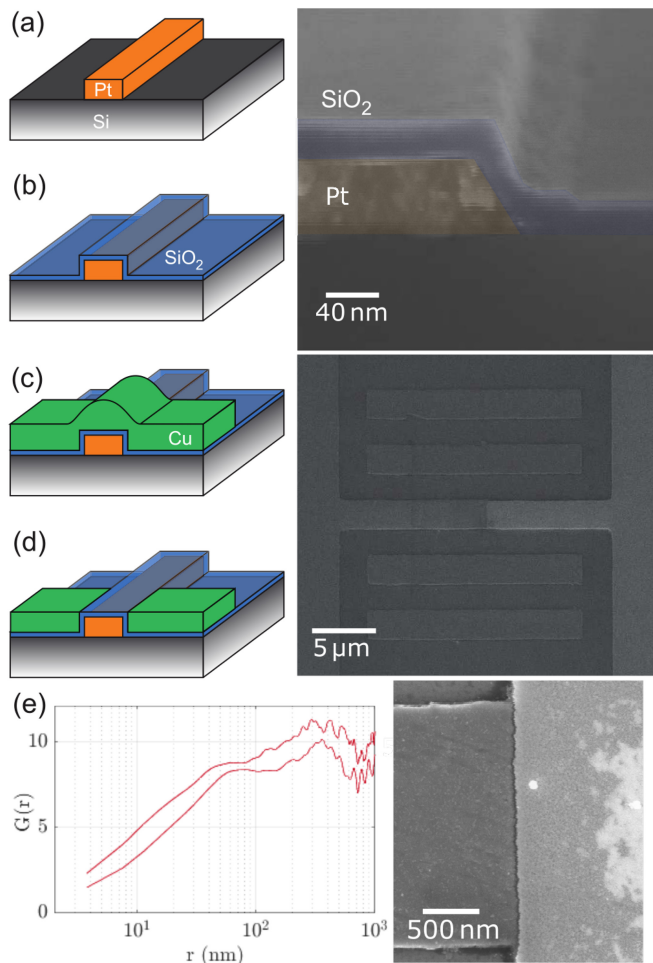
**FIGURE 1. (a) Schematics of a crossbar array consisting of perpendicular line-electrodes embedded into a memristive ECM material. The two levels consist of appropriate materials (e.g., Cu and Pt) enabling vertical filament growth as illustrated in the inset. (b) Schematic cross-section of a possible 3D interconnect system. To increase connectivity, the line-electrodes need to be shrunk to nodes that are controlled by an active CMOS layer and facilitate lateral and vertical filamentary connections to their nearest neighbors. The mushroom-shape of the electrodes reduces the alignment precision required for patterning of the second electrode layer.**

densities, and resistivity after SET is higher due to the length of the grown CF.

We have therefore developed a combined damascene-spacer process where the lateral electrode interdistance is determined by the ECM deposition process enabling true nanoscale lateral ECM cells. Here, we demonstrate the functionality of lateral ECM cells with a sub-25 nm switching layer (SL). Furthermore, we investigate the influence of electrode line edge roughness on the SET kinetics of such lateral devices with a simulation based on a kinetic Monte Carlo approach.

## II. DEVICE FABRICATION

Lateral ECM cells are fabricated as illustrated in Fig. 2. A first electrode is patterned onto a silicon substrate using electron-beam lithography (EBL), electron-beam evaporation (EBV) and lift-off (Fig. 2 (a)). To avoid resist blistering/shrinking during EBV and achieve appropriate deposition results, we employed the EBV technique presented in [22]. Next,  $\text{SiO}_2$  doped with 142 ppm of Al and 5 ppm of Cu is sputter-deposited on top of the substrate (b) serving as the SL [23], [24]. Low pressure magnetron sputtering is employed to ensure a deposition with proper conformality; the top right panel of Fig. 2 shows a cross-sectional electron micrograph as an example. Subsequently, a second electrode is fabricated using EBL, EBV and lift-off (c). Finally, chemical-mechanical-polishing is used to remove the second electrode material from the top of the first electrode



**FIGURE 2.** Left panels: Schematics of the fabrication process of lateral ECM cells: (a) definition of the first electrode, (b) sputter-deposition of an appropriate ECM material, (c) fabrication of a second electrode and (d) chemical-mechanical polishing. The right panels show scanning electron micrographs of process step (b) (top right, cross-section) and (d) (bottom right, top-down). In the top-down view the contact pads can be seen at the left and right sides and disconnected Cu lines assisting in the polishing process are visible at top and bottom. (e) Shows the extracted correlation functions  $G(r)$  for points of distance  $r$  along the metal edges of the device interface seen in the bottom SEM micrograph. The  $r$  values for local minima in  $G$  signify dominant wavelengths of the LER.

and a lateral ECM cells is formed (d). In the sketch a cell is formed on either side of the Pt electrode because of the crossed-line pattern.

Importantly, although two lithography processes have been employed during the fabrication, the distance between the two electrodes is determined exclusively by the deposition of the  $\text{SiO}_2$  SL. Hence, the use of EBL was only for convenience and the process itself does not require the overlay accuracy and resolution enabled by EBL. Due to the excellent control over the thickness of the deposited films, lateral ECM cells with only a few nanometers distance between the two electrodes become feasible. After polishing, another ECM layer and electrode could be deposited on top of the lateral ECM cell yielding connected vertical and lateral ECM

cells for which the inter-electrode distance is not controlled by lithography.

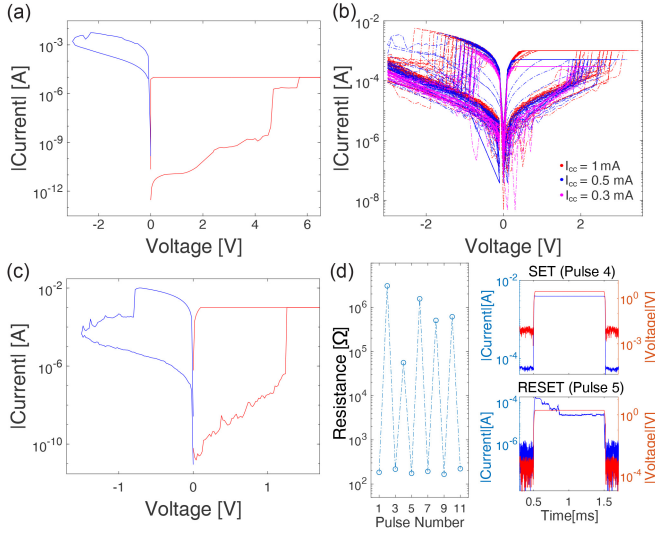
For a lateral device the edge and not the top surface of the metal will be the cell interface. Accordingly, the line edge roughness (LER) at that interface is a combination of the roughness of the deposited film and the typically much larger LER from the lithography process (see Fig. 2 (e)). Provided that the SL deposition is conformal and sufficiently thin, the LER of the first electrode will transfer to both the SL and second electrode which reduces the overall thickness variability compared to an interface defined by two independent LER profiles. For a thicker SL film (in the order of the dominant wavelength of the horizontal LER of the first electrode) the conformal deposition will cause valleys in the roughness profile to fill, smoothing the edge profile but causing variations in effective distance between the electrodes along the interface. In Section IV we investigate one mechanism by which LER may affect switching behavior, which is the position of the initial filament site (valley, hill or flank of the roughness profile), by modeling the subsequent CF growth from these seeds with a kinetic Monte Carlo approach.

Using the fabrication process detailed above, ECM cells with  $2\text{ }\mu\text{m}$  wide contacts consisting of Pt (on a Ti adhesion layer, counter electrode (CE)) and Cu (active electrode (AE)) are created in two variations. For the first variant, the CE is Pt-capped Ti (20 nm Pt on 80 nm Ti), the oxide thickness is 40 nm and the AE is 90 nm Cu. In the second variant, the respective thicknesses are 80 nm Pt on 5 nm Ti, 25 nm  $\text{SiO}_2$  and 90 nm Cu. The given oxide thickness is a nominal value as non-ideal conformity of the deposition process yields reduced thickness on the sides of the electrode (see Fig. 2 top right). The center SEM micrograph in Fig. 2 shows a top-down SEM image of a complete device with contact pads (left and right), Cu dummy lines to improve polishing (top and bottom) and the laterally oriented metal-insulator-metal interfaces (magnified in the bottom micrograph).

### III. RESULTS AND DISCUSSION

Measurements of the lateral ECM cells are carried out with Keithley 2636A (first variant) and Keithley 4200A-SCS (second variant) source meters connected to a probe station. A voltage bias is applied to the Cu AE, while the Ti/Pt CE is connected to ground.

For the first variant (40 nm  $\text{SiO}_2$ ) a current compliance of  $10\text{ }\mu\text{A}$  is used for the initial CF formation, which occurs at approximately 5.7 V. The high resistance state is recovered at  $-2.5\text{ V}$  (Fig. 3 (a)). Subsequently, the device shows resistive switching behavior at three different current compliance levels (1 mA,  $500\text{ }\mu\text{A}$ ,  $300\text{ }\mu\text{A}$ ), as shown in Fig. 3 (b). The transition from the high resistance state (HRS) to the low resistance state (LRS) occurs at approximately 2.5V (HRS to LRS) and  $-1.5\text{ V}$  (LRS to HRS). In addition to a relatively large variation for cycles using the same current compliance, a trend towards lower switching voltages for lower current compliances can be observed. By comparison, in a vertical



**FIGURE 3.** Electrical characteristics of lateral devices with Cu/Pt electrodes and SiO<sub>2</sub> ECM layer. (a) Initial forming of a CF and first RESET in a device with 40 nm SiO<sub>2</sub> thickness. The CF forms at 5.7 V (current compliance is 10 μA). The CF is erased at -2.5 V. (b) Switching behavior of 40 nm SiO<sub>2</sub> variant at multiple current compliance (*I<sub>cc</sub>*) settings (indicated by color). An overall trend towards lower switching voltages for decreasing current compliance can be observed, though variance at all compliance levels is relatively large. (c) Initial forming of a CF and first RESET in a device with 25 nm SiO<sub>2</sub> thickness. The CF forms at a much lower voltage of 1.3 V (current compliance is 1 mA). The RESET occurs at approximately -1 V. (d) LRS and HRS resistivity in a device with 25 nm SiO<sub>2</sub> after switching by 1 ms pulses (3 V SET and -2 V RESET). The LRS are at approximately 100 Ω, the HRS range from 4 kΩ to 3 MΩ. On the right, current/voltage-time plots (absolute values) corresponding to a SET and RESET operation are shown. The switching process during the SET is faster than the time resolution of the measurement setup (1 μs).

device (50 μm by 50 μm electrodes, data not shown here) using the same materials and SL thickness, slightly lower switching voltages (approximately 0.5 V) are observed with cycle-to-cycle variation scaling by a similar factor.

For the second variant of lateral device (25 nm SiO<sub>2</sub> layer), a Keithley 4200A-SCS equipped with a pulse measure unit is used. As expected with a thinner SL, the formation of the CF occurs at a significantly lower voltage of 1.3 V. A current compliance of 10 mA is used. Switching back to the HRS is observed below -1 V, as can be seen in Fig. 3 (c). The device is subsequently switched using 1 ms square pulses (20 μs rise and fall time) with 3 V SET and -2 V RESET amplitude (Fig. 3 (d) right). Equivalent pulses with an amplitude of only 0.5 V are used for READ operations and show LRS near 100 Ω, achieving the goal of low-ohmic SET-states, and HRS in the range of 4 kΩ to 3 MΩ (Fig. 3 (d) left).

#### IV. SIMULATED EFFECTS OF LINE EDGE ROUGHNESS ON SET KINETICS

A previously reported kinetic Monte Carlo (KMC) model [28] was used to investigate the influence of the measured LER on the SET kinetics of ECM cells. The approach is to use an established set of simulation parameters to investigate the influence of electrode/electrolyte interface LER on

SET kinetics in comparison to planar electrode/electrolyte interfaces. This allows the difference between lateral cells with LER and vertical cells with planar electrodes to be estimated. The considered processes contain motion of ions, reduction and oxidation. The rate equation for ionic motion is defined as

$$\Gamma_{\text{hop}} = \omega_{0,\text{hop}} \exp\left(-\frac{\Delta W_{\text{hop}} - 0.5ze\Delta\phi}{k_B T}\right)$$

with the vibrational frequency  $\omega_{\text{hop}}$ , the migration barrier  $\Delta W_{\text{hop}}$ , the ion charge number  $z$ , the elementary charge  $e$ , the Boltzmann constant  $k_B$ , the local temperature  $T$  and the potential difference between two adjacent cells  $\Delta\phi$ . The reduction rate can be written as

$$\Gamma_{\text{red}} = k_{\text{red}}\omega_{0,\text{red}} \exp\left(-\frac{\Delta W_{\text{red}} - \alpha ze\eta}{k_B T}\right)$$

and the oxidation rate as

$$\Gamma_{\text{ox}} = k_{\text{ox}}\omega_{0,\text{ox}} \exp\left(-\frac{\Delta W_{\text{ox}} + (1 - \alpha)ze\eta}{k_B T}\right)$$

with the reaction rate constants  $k_{\text{red}}$  and  $k_{\text{ox}}$ , the charge transfer coefficient  $\alpha$ , the overpotential  $\eta$ , and the activation energy for reduction/oxidation  $\Delta W_{\text{red}}/\Delta W_{\text{ox}}$ . Note that these energies are slightly different depending on the site of reduction/oxidation (c.f Table 1), as explained in [28]. The electric potential is calculated by coupling of two Laplace equations. One accounts for the metallic domains and describes electronic currents, the other one accounts for the SL and describes ionic currents. The Laplace equations are defined as

$$\nabla\sigma_{\text{me}}\nabla\varphi_1 = 0 \quad (1)$$

and

$$\nabla\sigma_{\text{ion}}\nabla\varphi_2 = 0 \quad (2)$$

with the electric potential  $\varphi_1$  within the metallic areas (AE, CE, CF), the electric potential  $\varphi_2$  within the SL, the electronic conductivity  $\sigma_{\text{me}}$  of the AE/CE/CF material and the ionic conductivity  $\sigma_{\text{ion}}$  of the SL. The ionic conductivity is further defined via the local ion concentration  $c_{\text{ion}}$ , defined as the average number of ions in a surrounding square with edge length  $5a$ , where  $a$  is the lattice constant of the SL material. With the mobility  $\mu_{\text{ion}}$  of an active ion, the ionic conductivity can be written as

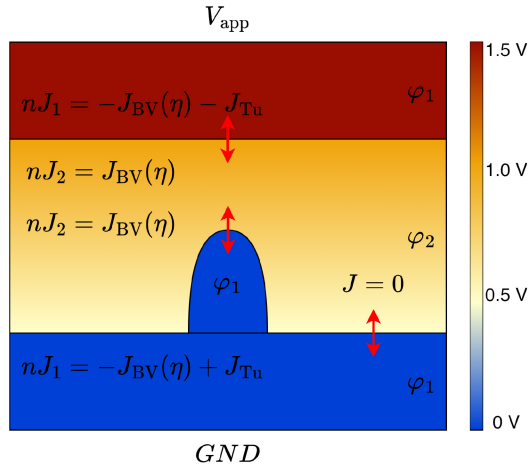
$$\sigma_{\text{ion}} = ze\mu_{\text{ion}}c_{\text{ion}}.$$

The coupling of equation (1) and equation (2) is achieved by Neumann boundary conditions, which include the electron exchange mechanism calculated by Butler-Volmer currents (Fig. 4). This implementation leads to continuous current through the cell, but creates a voltage jump at the AE/SL, CE/SL and CF/SL interfaces, called overpotential  $\eta$ .

The Butler-Volmer equation is denoted as

$$J_{\text{BV}} = J_0 \left( \exp\left(\frac{(1 - \alpha)ze\eta}{k_B T}\right) - \exp\left(-\frac{\alpha ze\eta}{k_B T}\right) \right)$$





**FIGURE 4.** Simulation model for FEM calculation of the electric potential  $\phi$  and currents based on Eq. (1) and Eq. (2) for the metallic ( $\phi_1$ ) and electrolytic ( $\phi_2$ ) domains. At the AE/SL, SL/CF and SL/CE interfaces, Neumann boundary conditions apply, leading to the reaction overpotential  $\eta$ .

**TABLE 1.** Simulation model parameters.

Symbol	Value	Symbol	Value	Symbol	Value
$W_{\text{hop,surf}}$	0.27 eV	$W_{\text{ox,hole}}$	0.58 eV	$k_{\text{red}}$	1
$W_{\text{hop,bulk}}$	0.3 eV	$W_{\text{ox,kink}}$	0.46 eV	$k_{\text{ox}}$	1
$W_{\text{hop,adsorb}}$	0.25 eV	$a$	0.25 nm	$z$	1
$W_{\text{hop,desorb}}$	0.27 eV	$I_{\text{cc}}$	100 nA	$m_{\text{eff}}$	$0.5 m_0$
$W_{\text{red,adatom}}$	0.58 eV	$\omega_{0,\text{hop}}$	$2\text{e}13$ Hz	$\Delta W_0$	4 eV
$W_{\text{red,kink}}$	0.52 eV	$\omega_{0,\text{red}}$	$1\text{e}13$ Hz	$\mu_{\text{ion}}$	$1\text{e}-9 \frac{\text{cm}^2}{\text{Vs}}$
$W_{\text{red,hole}}$	0.45 eV	$\omega_{0,\text{ox}}$	$2\text{e}13$ Hz	$\alpha$	0.3
$W_{\text{ox,adatom}}$	0.41 eV	$T$	300 K		

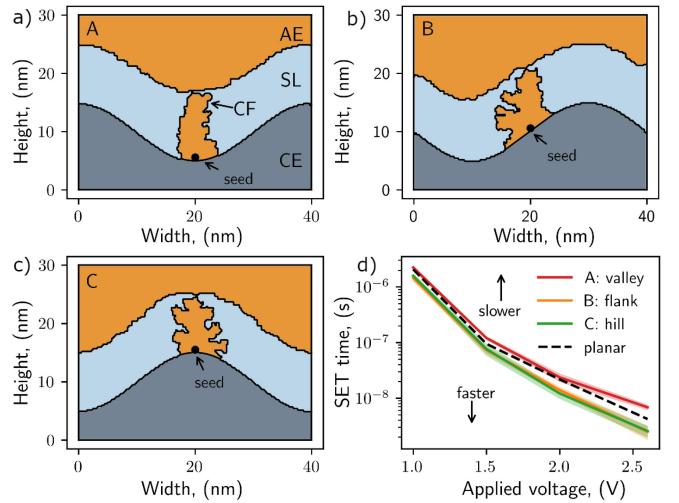
with the exchange current density  $J_0$  defined as

$$J_0 = z e c_{\text{ion}} k_{\text{et}} \exp\left(-\frac{\Delta W_{\text{et}}}{k_B T}\right)$$

with the heterogeneous rate constant  $k_{\text{et}}$  and the activation energy  $\Delta W_{\text{et}}$ . When the gap between CF and AE gets small compared to the SL height, a significant tunnel current sets in. This tunnel current is defined as current density between CF and AE. The tunnel current density between similar electrodes is defined using the linear Simmons equation [30].

$$J_{\text{TU}} = \frac{3\sqrt{2m_{\text{eff}}\Delta W_0}}{2x} \left(\frac{e}{h}\right)^2 \exp\left(-\frac{4\pi x}{h} \sqrt{2m_{\text{eff}}\Delta W_0}\right) V_{\text{TU}}$$

with the effective electron mass  $m_{\text{eff}}$ , the distance  $x$  between CF and AE, the tunnel barrier height  $\Delta W_0$ , the Plank's constant  $h$  and the tunnel voltage  $V_{\text{TU}}$  defined as the voltage difference  $V_{\text{TU}} = \phi_{1,\text{AE}} - \phi_{2,\text{CF}}$  between AE and CF. The parameters used in the simulations are shown in Table 1. As stimulus a rectangular voltage signal with variable amplitude  $V_{\text{app}}$  is applied to the AE. When the current reaches the maximum current  $I_{\text{CC}}$ , the simulation is aborted and the time to reach  $I_{\text{CC}}$  is stored as SET time  $t_{\text{SET}}$ .



**FIGURE 5.** (a)-(c) Grown CFs from KMC simulations with LER of 10 nm,  $V_{\text{app}}=1.5$  V,  $I_{\text{CC}}=100$  nA and  $t=t_{\text{SET}}$ , seed location changes between all three possible and relevant positions (A: valley, B: flank, C: hill). CF morphology changes with seed location, for seeds in the valley directed growth occurs, for the other positions rather isotropic growth occurs. (d) Simulated SET times for all 3 seed positions for applied voltages of 1 V, 1.5 V, 2 V and 2.6 V in comparison to the kinetics of a planar geometry with a LER of 0 nm. While the results of hill and flank overlap, the CF grows slowest within a valley. Light outlines of the curves show the standard deviation of the mean.

A realistic LER profile is needed as a starting point for the described simulation. Such a profile was extracted from an SEM micrograph of the interfaces of a fully fabricated lateral ECM device, with the LER wavelengths being quantified by calculation of the correlation function for points on either edge (see Fig. 2 (e)) and the amplitude estimated directly from the line fit of the edges. The dominant spacial wavelength was roughly 100 nm (first dip in the correlation function) while the  $3\sigma$  edge variation was approximately 19 nm (over a 90 nm length). To investigate the possible effects of LER on switching kinetics, the simulation was then done for a slightly more pronounced LER profile: the AE/CF and CF/CE domains were evenly, sinusoidally warped with an amplitude of 10 nm and a wavelength of 40 nm over a width of one full wavelength.

The seed, also called critical nucleus, was then placed at 3 relevant positions, which are valley (Fig. 5 (a)), flank (Fig. 5 (b)) and hill (Fig. 5 (c)). The simulated applied voltages  $V_{\text{app}}$  are 1 V, 1.5 V, 2 V and 2.6 V. Due to the statistical nature of a KMC model, each simulation was performed ten times for every seed position and at every voltage and the mean values are plotted in Fig. 5 (d). The light outlines of the curves show the standard deviation of the mean. The results for flank and hill overlap, while the results for valley clearly show slower switching. For comparison, the kinetics of a planar geometry corresponding to a regular vertical cell were also simulated. Of the three LER cases examined (valley, hill, flank), the planar geometry corresponds most closely to the flank case; accordingly, both SET times almost coincide. Compared to the scattering of real measurements [29] the influence of the LER on the SET kinetics is negligible.

This leads to the conclusion that the reported self-aligned, conformal fabrication can be used for the development of 2D and 3D ECM structures without additional concerns due to LER effects.

## V. CONCLUSION

We have presented a novel process for the fabrication of lateral ECM cells. With this process, the achievable distance between electrodes can be reduced to the few tens of nanometer scale without need for a lithography process with extreme overlay accuracy. Using this process, ECM cells with less than 25 nm lateral separation between electrodes were created and shown to exhibit resistive switching behavior, as well as functionality in pulsed operation. Through the use of a kinetic Monte Carlo simulation we also found that line edge roughness effects on SET kinetics are small and unlikely to be a problem with lateral ECM devices.

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