

Semiconductor Membranes for Electrostatic Exciton Trapping in Optically Addressable Quantum Transport Devices

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 (Received 11 September 2022; revised 15 March 2023; accepted 21 March 2023; published 28 April 2023)

Combining the capabilities of gate-defined quantum transport devices in GaAs-based heterostructures and of optically addressed self-assembled quantum dots could open up broad perspectives in quantum technologies. For example, interfacing stationary solid-state qubits with photonic quantum states would open up a pathway towards the realization of a quantum network with extended quantum processing capacity in each node. While gated devices allow very flexible confinement of electrons or holes, the confinement of excitons without some element of self-assembly is much harder. To address this limitation, we introduce a technique to realize exciton traps in quantum wells via local electric fields by thinning a heterostructure down to a 220-nm-thick membrane. We show that mobilities over $1 \times 10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ can be retained and that quantum point contacts and Coulomb oscillations can be observed on this structure, which implies that the thinning does not compromise the heterostructure quality. Furthermore, the local lowering of the exciton energy via the quantum-confined Stark effect is confirmed, thus forming exciton traps. These results lay the technological foundations for devices like single-photon sources, spin-photon interfaces and eventually quantum network nodes in GaAs quantum wells, realized entirely with a top-down fabrication process.

DOI: [10.1103/PhysRevApplied.19.044095](https://doi.org/10.1103/PhysRevApplied.19.044095)

I. INTRODUCTION

A tremendous amount of insight has been gained from a broad range of quantum transport experiments, ranging from the first observations of quantum point contacts and Coulomb blockade over quantum Hall physics all the way to the realization of spin qubits aspiring to become a highly scalable platform for quantum computing. For all of these topics, gateable two-dimensional electron gases (2DEGs) in semiconductor heterostructures have been a veritable workhorse. A similar wealth of results has emerged from semiconductor (quantum) optics experiments using

self-assembled quantum dots that accommodate confined exciton states. Yet, these domains have developed largely separately, partly due to the difficulty of electrostatically confining excitons. Notable exceptions include the detection of a the charge state of an ensemble of quantum dots via transport of a 2DEG or a doped back gate [1,2] and the confinement of a small number of indirect excitons using gates [3]. One may thus expect very rich possibilities from devices that combine both gateable carrier gases allowing the formation of quantum dots and controllably confined exciton states.

A specific application of such a device, which is also the main motivation for this work, would be an interface between a matter qubit and a photonic qubit, which is an essential requirement to build a quantum communication network or a distributed quantum computer [4]. Over the last decade, major steps towards such networks have been made with optically active solid-state qubits, in particular nitrogen-vacancy centers in diamond [5–7] and self-assembled quantum dots (SAQDs) [8–10]. While the photonic quantum resource can be exploited

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in remarkable ways [11,12], using the spin resource of these qubits (electron-hole spin for SAQDs or vacancy electron/nitrogen-14 nuclear spin for nitrogen-vacancy centers in diamond) for quantum computing remains challenging [12–14].

For quantum computing nodes with at least tens of locally connected qubits, gate-defined quantum dots (GDQDs) formed in a semiconductor heterostructure are a potentially more compelling platform. While silicon is a natural choice for isolated quantum processors, devices in a GaAs/Al_xGa_{1-x}As heterostructure have pioneered the field [15–20] and offer advantages for optical interfacing due to the direct band gap. Yet the absence of hole confinement in a conventional electron GDQD prevents the confinement of excitons and hence the coherent coupling to light. Earlier works have already demonstrated detection [21] and capture [22] of a single photoelectron by a GDQD. However, the photohole could not be confined in these previous studies, leading to a loss of phase information. To remedy this limitation, one approach is to engineer the *g*-factor of electrons and holes to break their entanglement [23–26]. Another idea pursued here is to add an optically active quantum dot (OAQD) able to confine excitons and acting as spin-photon interface in close vicinity of the GDQD [27].

One candidate for an OAQD would be a SAQD grown above or below the 2DEG [28]. These dots can be directly embedded into the III–V heterostructure and they have been proven to be efficient single-photon sources [13] or spin-photon interfaces [29]. Tunnel coupling between an InAs SAQD and a reservoir has also been demonstrated [2]. However, all these major steps were achieved on SAQDs randomly distributed and having varying optical features due to the Stranski-Krastanov growth process. In other words, the dots showing the best features have to be found manually, which limits the scalability of this approach. Besides, the strain introduced in the lattice by the SAQDs degrades the electron mobility of the 2DEG underneath. While values not much below $10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are desirable to reliably form GDQDs, the mobility of a 2DEG with embedded SAQDs typically remains one or two orders of magnitude lower [1].

Here, we introduce a top-down approach where the OAQD is fabricated deterministically and can be directly embedded in close vicinity to the GDQD to ensure tunnel coupling [Fig. 1(a)]. To trap excitons the idea is to use the quantum-confined Stark effect in a quantum well (QW) [30–32] in the following way [Fig. 1(b)]. A QW or two coupled quantum wells confine excitons in the direction of growth. If an electric field is applied perpendicular to the QW, the exciton energy is lowered as the electron and hole can partially dissociate, thus creating an electric dipole interacting with the electric field. A complete dissociation is prevented by the confinement so that an

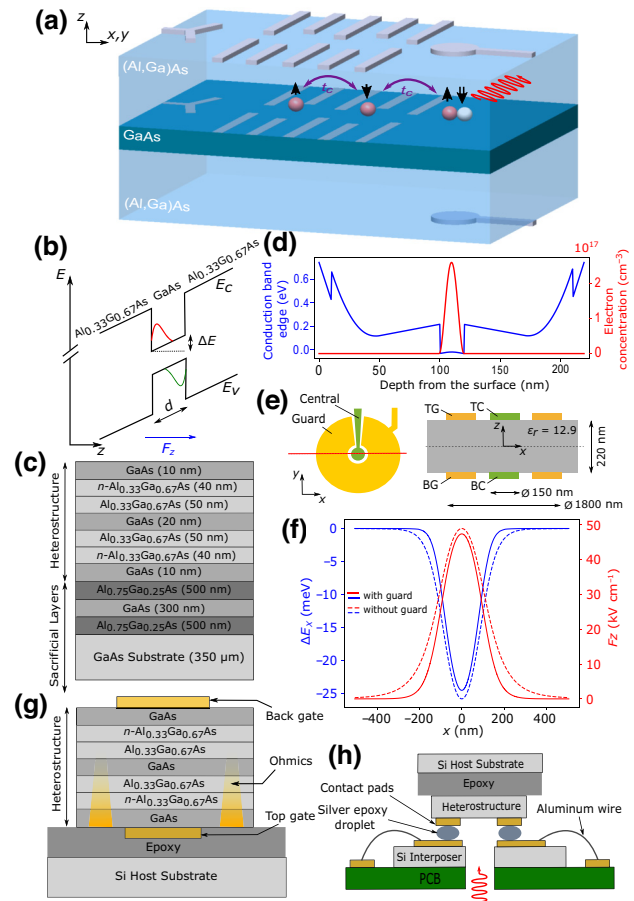


FIG. 1. (a) Sketch of an optical interface for GDQDs (left side) based on an electrostatically defined exciton trap (right side). The transfer of information is mediated by tunnel coupling t_c . (b) Quantum-confined Stark effect on a (Al,Ga)As/GaAs/(Al,Ga)As heterostructure resulting from an electric field F_z applied in the growth direction z . E_C and E_V are the conduction and valence band edges, respectively. The electron and heavy-hole ground-state wave functions inside the quantum well (QW) are depicted. (c) Full layer stack composed of the sacrificial layers and the thin heterostructure investigated. (d) Self-consistent simulation of the conduction band edge. (e) Sketch of the exciton trap consisting of the central (C) gates and the guard (G) gates separated by a 50 nm slit. The same gates were patterned on the top (T) and bottom (B) surface. The cross section of the sample along the red dotted line is used to simulate the electric field profile in COMSOL in the x direction at the center of the QW. The heterostructure was modeled without dopants and 2DEG. (f) Calculated electric field and exciton energy shift when $V_{TC} = -1.2 \text{ V}$ and the other gates are set to 0 V. (g) Device layout for Hall measurements where the thin heterostructure is bonded to a silicon host with epoxy. Note that the original top surface is now in contact with the epoxy. (h) Scheme to connect the contact pads on the device to a printed circuit board.

overlap between the electron and hole wave function and thus optical addressability are retained. To achieve lateral confinement, the electric field needs to be applied locally, which can be achieved with appropriately patterned gates.

Such traps filled with only a few (indirect) excitons under sufficiently weak illumination have been demonstrated in a double quantum well gated by an unstructured, heavily doped back gate in the heterostructure and a patterned metal top gate [3]. An additional expected advantage is better control of the operating wavelength, which depends on the QW width and the electric field. Tuning with the latter is possible over a range wider than the fluctuations of the well width, giving the possibility of fabricating photon sources with identical wavelength for interlinking different quantum devices.

One limitation of this specific realization is that a transverse electric field is necessarily associated with an in-plane field of similar magnitude due to the fixed potential at the back gate. This can laterally dissociate excitons in III–V semiconductor quantum wells, which typically have a binding energy below 10 meV [33]. Besides, it is not possible to independently control the electric field determining the Stark shift and the electrostatic potential, which would be very advantageous for coupling confined exciton states to electrons in GDQDs. More recently, electrically controllable trapping of indirect and direct excitons has been demonstrated in transition dichalcogenide semiconductors [34–37]. The larger binding energy of the excitons in the materials (in the range of tens of meV) eases the limitation posed by the in-plane electric field, but the fabrication of these traps remains challenging to scale up and to integrate next to a GDQD.

Here, we address these limitations by demonstrating a fabrication process and devices on a 200-nm-thick membrane accommodating a QW with gates on both sides of the structure that were patterned using high resolution electron-beam lithography. Due to the small size of the gates, a sufficient confinement to resolve the orbital level splitting between exciton states is expected (Sec. II). The electric field across the heterostructure is set by the voltage difference between the top and the bottom gates (difference mode) while the electric potential is independently controlled by the sum of these two voltages (common mode). Based on this device design, we demonstrate a local lowering of the exciton energy by up to 15 meV with 150-nm large gates (Sec. V).

A key ingredient of such structures is the removal of the GaAs substrate to pattern a metal gate on the bottom side of the heterostructure. This removal leaves an etched surface, which might degrade the quality of the heterostructure and cause detrimental charge noise. With our fabrication process (Sec. II), we show that mobilities similar to those required for single-electron quantum dots can be achieved (Sec. III) and demonstrate a quantum point contact and a quantum dot with high-quality characteristics in such a structure (Sec. IV). Our process thus overcomes key hurdles on the way to electrostatic exciton traps for devices like highly tunable single-photon sources and spin-photon interfaces.

Heterostructures released from the substrate have been used previously both for transport and optical experiments, using different approaches for their realization. One possibility is to grow a sacrificial layer between the substrate and the heterostructure, which is locally removed to create a suspended membrane. Transport studies have been carried out for this type of membrane hosting an electron gas [38–40]. Alternatively, the substrate is completely removed to fully expose the bottom side of the heterostructure. The second approach is more suited for our final purpose as it allows patterning of the two sides of the heterostructure with standard techniques. Weckwerth *et al.* [41] demonstrated contacts to two coupled QWs grown on a doped heterostructure and control of their respective carrier densities with Schottky gates on each side on the heterostructure. The electron mobility of their doped device was $3.3 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (for an electron density between 1 and $4 \times 10^{11} \text{ cm}^{-2}$). On an undoped heterostructure, Gupta *et al.* [42] showed that mobility close to $10^7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (for an electron density of $5.8 \times 10^{11} \text{ cm}^{-2}$) can be reached with this device architecture. This high mobility is comparable to the high-quality as-grown doped heterostructure which is typically higher than $10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [43] and commonly desirable for GDQDs. However, the thickness of the heterostructure and its gate stack was a few micrometers, which is much too large to achieve sufficiently tight exciton confinement and to realize single-electron quantum dots. In the nanophotonics community, suspended membranes hosting SAQDs have been fabricated to create photonic cavities enhancing the light-matter interaction [44] or to couple the emitted light to photonic waveguides [45]. Complete removal of the substrate was also done to improve the collection efficiency by incorporating a metallic mirror underneath the heterostructure [46] or to tune the exciton emission with a piezoelectric substrate [47]. Apart from the more conventional approach to confine excitons, these devices did not involve double-sided, high-resolution patterning.

II. DESIGN AND FABRICATION OF THE DEVICES

To implement the coupling concept between a GDQD and an electrostatically defined exciton trap, we considered the GaAs/Al_{0.33}Ga_{0.67}As modulation-doped heterostructure illustrated in Fig. 1(c). The first layers until the bottom GaAs cap consist of GaAs smoothing layers and Al_{0.75}Ga_{0.25}As sacrificial layers that will be etched away during the fabrication process. It is the remaining upper layers from the 220-nm-thin heterostructure that will be investigated throughout this paper. The 20-nm undoped GaAs quantum well is separated from the silicon dopants ($6.5 \times 10^{17} \text{ cm}^{-3}$) in the Al_{0.33}Ga_{0.67}As barrier layers by a 50-nm spacer of intrinsic Al_{0.33}Ga_{0.67}As. Figure 1(d)

shows the conduction band profile simulated with a self-consistent Poisson-Schrödinger solver. The pinning level for the as-grown and the etched surface was assumed near mid-gap. The density and the position of the dopants were chosen to compensate for the surface states while still obtaining a high fraction of ionized dopants. Assuming that the Fermi level is pinned 120 meV below the conduction band edge in the doped region due to a high density of deep donor levels (DX centers) [48], the expected carrier density is of the order of $n_s = 2.8 \times 10^{11} \text{ cm}^{-2}$ and only the lowest subband is populated. Given good electrical stability, this heterostructure is suited to fabricating GDQDs, but the ideal layout of the depletion gates will not be discussed in this study.

The exciton trap consists of one circular gate called the central gate and one surrounding ring gate called the guard gate separated by a narrow slit, both patterned on the two sides of the heterostructure. The top central (guard) gate is vertically aligned with the bottom central (guard) gate [Fig. 1(e)]. The central gates are used to confine excitons underneath them by the quantum-confined Stark effect. By applying a negative voltage V_{TC} to the top central gate and a zero voltage to the three other gates, the 2DEG can be depleted and a vertical electric field is built locally under the central gates. Figure 1(f) shows that the COMSOL-modeled electric field profile in the x -direction at the center of the QW has a parabolic shape (the heterostructure has been modeled free of charges). The exciton energy is reduced by this vertical electric field and the energy shift has been computed by solving the Schrodinger equation for the electron and holes with Coulomb interaction [49]. The trapping potential is also approximately parabolic towards the center of the central gate. The guard gates improve the reduction of the electric field outside the central gates and thus provide a steeper confinement. When $V_{TC} = -1.2 \text{ V}$, the model for the geometry considered in Fig. 1(e) predicts a maximum trapping potential with a depth of -24.5 meV . By fitting the bottom of the potential simulated to a quantum harmonic oscillator solution, we obtain an energy splitting between exciton states of $741 \text{ } \mu\text{eV}$ and a ground-state wave function with a spatial width of 14.1 nm . The energy splitting is comparable to the single particle orbital level spacing of GaAs GDQD (approximately 1 meV [15]) and can be resolved by operating the sample in a dilution refrigerator around 20 mK . Quantum confinement of excitons can therefore be expected for this trap geometry.

Our overall strategy to fabricate a device on a thin semiconductor heterostructure follows the guidelines described by Weckwerth *et al.* [41]. We optimized or adapted some steps to match our requirements. The strategy starts with the patterning of the as-grown surface. The sample is then flipped and glued to a host Si substrate. The original GaAs substrate is completely etched away until the bottom cap and the resulting etched surface can finally be patterned.

The final sample architecture of an exemplary Hall bar with a top and bottom Schottky gate to assess the electrical properties of the 2DEG (Sec. III) is shown in Fig. 1(g). Conventional photolithography is used to pattern a Hall bar on the top side. A mesa (not shown) is etched down to at least 210 nm , thus removing the complete heterostructure, with a $100 : 3 : 3 \text{ H}_2\text{O}/\text{H}_2\text{O}_2/\text{H}_3\text{PO}_4$ solution, and Au/Ge/Ni ohmics are metallized and annealed at 480°C for 60 s in a N_2/H_2 atmosphere. The top Schottky gate is then patterned on top of the mesa and a semitransparent metal stack ($2 \text{ nm Ti}/7 \text{ nm Au}$) was deposited. The top-side of the resulting Hall bar is then glued with a thin layer of low-curing temperature and low-stress epoxy (Epotech 353ND) to a Si host substrate before removal of the GaAs substrate. This epoxy shows the appropriate viscosity to be dispensed as a small drop on the sample. The host substrate is manually pressed on top with a low force and slid back and forth to spread the epoxy over the surface of the sample. The resulting thickness of the squeezed epoxy is not precisely controlled but is typically around a few micrometers. In principle, any type of substrate can be used as a host as long as the epoxy has good adhesion on it, but we found silicon convenient as it is not damaged by the chemicals used in the process. An etching solution ($\text{H}_2\text{O}_2 + \text{citric acid}$) selectively etches the whole GaAs substrate until the $500\text{-nm Al}_{0.75}\text{Ga}_{0.25}\text{As}$ etch stop, which is not attacked [50]. It was prepared from citric acid monohydrate dissolved $1 : 1$ by weight into deionized water, and H_2O_2 was added so that the overall citric acid/ H_2O_2 mixing ratio was $4 : 1$ by volume. This ratio turned out to be a good compromise between fast etch rate (around 7 nm/s) and good selectivity. The etch stop is removed by a 1% diluted hydrofluoric acid (HF) solution (around 8 nm/s). Fine particles typically remain on the surface, and they are speculated to be a hydroxide of aluminum [51] formed during the etch stop removal. They can be dissolved by a 30-s dip in a hydroxide potassium solution ($25 \text{ g}/100 \text{ ml}$ deionized water). Our experience showed that a full chemical etching of the substrate instead of a combination mechanical polishing and chemical etching [41,42] reduces the risk of cracks on the thin semiconductor heterostructure. Another cycle of ($\text{H}_2\text{O}_2 + \text{citric acid}$) + HF etches the 300-nm GaAs buffer layer and the $30\text{-nm Al}_{0.75}\text{Ga}_{0.25}\text{As}$ second etch stop. These are not fundamentally necessary for the fabrication process, but a two-step substrate removal consisting of a first thick etch stop followed by a thinner one is expected to provide a smoother surface at the bottom GaAs cap. Once the latter is accessible, the back gate can be patterned in the same way as the top gate. The alignment accuracy achieved with optical lithography between the top and bottom features is a few micrometers as the 220-nm heterostructure is sufficiently transparent. Finally, holes are etched through to access the contact pads of the buried ohmics and top gate. Following all these steps, we were able to achieve

yields around 80% for Hall Bars. The most common failure mode is physical damage of the sample during processing. For the other devices discussed in Secs. IV and V, the nanometer-scale gates were written with electron beam lithography. Two thicknesses (2 nm Ti/7 nm Au and 5 nm Ti/20 nm Au) for these gates were considered depending on the transparency requirement. The alignment of the top and bottom gates used for the exciton trap was simplified by the transparency of the thinned heterostructure: the markers written on the top side are visible with scanning electron microscopy through the membrane and could be imaged on the bottom side after flipping. On the scanning electron micrograph of the exciton trap in Fig. 5(a), the top gates located under the flipped heterostructure (blurry edges) and the bottom gates located on top (sharp edges) were imaged simultaneously. While spatially separated far from the trap region, the top and bottom gates overlap near the exciton trap [inset of Fig. 5(a)] with an alignment accuracy of ± 35 nm. To obtain this estimate, two concentric metal disks were placed on both surfaces (2.5 μm radius/9 nm thick on the bottom surface and 1 μm radius/25 nm thick on the top surface). The measured center-to-center distance between the two disks reflects the misalignment.

Conventional wire or ball bonding techniques were not successful in connecting the ohmics and the gates of our samples to a chip carrier due to the softness of the membrane and the epoxy. The bonding technique that we opted for is sketched in Fig. 1(h). Fine droplets of silver epoxy are placed on the contact pads of a silicon interposer either manually or with a stencil. The 220-nm heterostructure is then flipped and pressed onto a Si interposer with a flip-chip bonder. The silver epoxy is baked for 5 min on the bonder while the interposer and the membrane are aligned. A longer curing (20 min) then takes place in an oven to strengthen the bond. The interposer can finally be connected to a printed circuit board (PCB) with a wire bonder. Compared to the manual gluing of a wire with silver epoxy between the contact pads of the sample and chip carrier, our approach is more reliable and can easily connect a large number of pads. If illumination of the surface of the sample is needed, an opening can be made through the PCB and the silicon interposer before the bonding procedure. The PCB is simply drilled and a 3×3 mm² hole is cut on the interposer with a laser marker (Coherent CombiLine Advanced). Typical writing parameters were 33 A driving current of the laser head, 15 kHz pulse repetition rate and 50 mm/s scanning speed. The surface of the interposer was protected beforehand with a thick layer of photoresist (1.4 μm). The accuracy on the position of the hole was of the order of a few hundred micrometers, which is good enough for our purposes. We found the laser cutting much easier and quicker than wet or dry etching of silicon. Compared to a glass interposer, an open window in silicon avoids transmission and reflection losses and ensures that

the thermal expansion of the interposer is matched to that of the host substrate.

III. ELECTRON GAS PROPERTIES ON THIN SEMICONDUCTOR HETEROSTRUCTURE

The Hall bar described above was characterized electrically and optically to extract the carrier density n_s and the mobility μ of the 2DEG. Only the lowest subband of the 2DEG is supposed to be populated and the device should be gateable without hysteresis. The Hall bar was cooled to 35 mK in a dilution refrigerator equipped with optical windows. An objective lens was mounted on the sample stage for confocal microscopy. This temperature and mounting configuration corresponds to the operating conditions for the exciton trap and qubits coupled to it. We performed Hall measurements with a standard four-terminal method with a driving current of 30 μA without illumination. Figure 2(a) shows the longitudinal and transverse voltage when the top gate voltage (V_{TG}) and back gate voltage (V_{BG}) are set to zero. Clear Shubnikov–de Haas oscillations can be seen and the $1/B$ spectrum [inset Fig. 2(a)] shows a single period. Note that the splitting

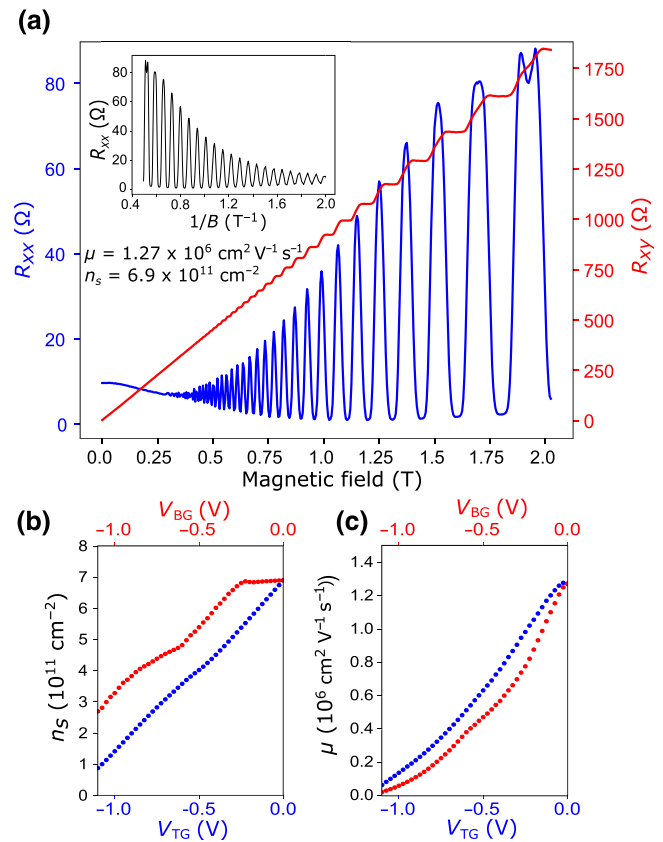


FIG. 2. (a) Hall resistance R_{xy} and Shubnikov–de Haas oscillations for $V_{\text{TG}} = V_{\text{BG}} = 0$ V. The inset shows the clear $1/B$ period of the oscillations. The carrier density n_s (b) and the mobility μ (c) can be tuned with the top gate and back gate voltage.

of the peaks starting to occur around 2 T corresponds to the lifting of the spin degeneracy. Hence, the conduction channel consists of only the lowest subband. From the minima of the oscillations, the carrier density of the 2DEG is $n_s = 6.9 \pm 0.2 \times 10^{11} \text{ cm}^{-2}$ and the mobility reaches $\mu = 1.27 \pm 0.01 \times 10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (uncertainties derived from the fitting errors). An identical carrier density within the error range was found from the slope of the Hall voltage as a function of magnetic field. As a reference, the same heterostructure as Fig. 1(c) was grown in the same molecular beam epitaxy (MBE) chamber without the sacrificial layers to avoid an undesired electron channel at the interface between the 30-nm $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ etch stop and the 300-nm GaAs buffer layer. A Hall bar with identical geometry, was made on this wafer, but without etching away the GaAs substrate. At 4.2 K, the carrier density was $n_s = 7.1 \times 10^{11} \text{ cm}^{-2}$ and the mobility $\mu = 1.51 \times 10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Keeping in mind the different measurement temperatures and the growth fluctuations, we can conclude that the heterostructure was not significantly damaged after the substrate removal and further processing. The mobility of the thinned heterostructure remains above $10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is commonly considered sufficient to form single-electron quantum dots. In both samples, the carrier concentrations measured are larger than the simulated value. This discrepancy may be due to an insufficient concentration of DX centers (deep Si donor levels) in the doped barriers [48], which leads to pinning of the Fermi level just a few milli-electron-volts below the conduction band due to shallow, unstable traps. The response of the carrier density to the top gate and back gate [Fig. 2(b)] is consistent with this hypothesis. While the top gate can directly deplete the gas, the back gate starts to have an effect only after a threshold voltage of -0.25 V . This behavior may be due to the filling of shallow traps or excess surface states on the etched surface, either of which would screen the back-gate voltage. The high carrier density and the fact that the mobility in Fig. 2(c) declines even at fixed density suggest that shallow traps are the more likely cause. We thus expect that fine adjustments of the growth parameters, in particular the material fluxes, can improve the gateability and stability of the device, which is backed up by results from quantum point contacts on a different heterostructure discussed below.

The single subband nature of the 2DEG can also be confirmed by photoluminescence (PL) measurements under magnetic fields. The sample was illuminated by a 795-nm continuous laser. The excitation energy is below the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ energy barrier to avoid the creation of carriers in the barrier. The spot size on the sample was approximately $3 \mu\text{m}$ with an average power of 100 nW. The PL was dispersed by a 1-m grating spectrometer and detected by a charge couple device thermoelectrically cooled to -80°C . Figure 3(a) shows the PL spectrum at zero magnetic field. The asymmetric and broad line shape

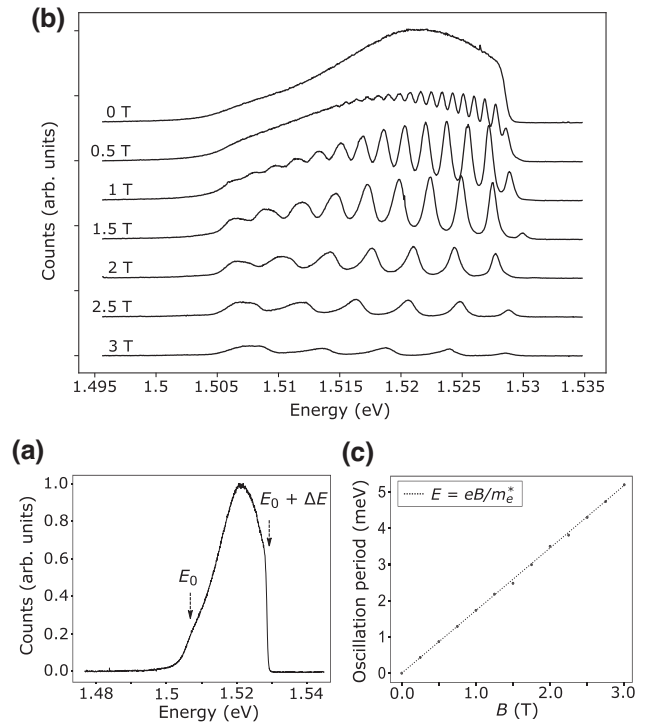


FIG. 3. (a) Photoluminescence (PL) lineshape of the double-side-doped heterostructure. E_0 corresponds to the bottom of the QW energy band. The Fermi edge can be seen at $E_0 + \Delta E$. (b) PL spectra at different magnetic fields. (c) Period of the oscillations as a function of the perpendicular magnetic field. The dashed line corresponds to the theoretical cyclotron energy.

exhibits the characteristic features of a QW hosting an electron gas [52,53]: the bottom of the QW energy band at $E_0 = 1.507 \text{ eV}$ and the Fermi edge at higher energy $E_0 + \Delta E = 1.527 \text{ eV}$. The absence of a shoulder near the Fermi edge shows that the second conduction subband is not occupied [54,55]. The energy E_0 is redshifted by approximately 15 meV compared to the energy measured at 8 K for a 20-nm QW on GaAs substrate [56]. In addition to lower temperature, we attribute this difference to a change of strain on the QW after substrate removal [57]. The overall width of the emission ΔE gives an estimate of the Fermi energy [52–54] of $E_F = \Delta E / (1 + m_e^*/m_h^*) = 23 \text{ meV}$, where m_e^* (m_h^*) is the effective electron (hole) mass. Assuming the 2D electron density of states of GaAs is $g = 2.8 \times 10^{10} \text{ meV}^{-1} \text{ cm}^{-2}$, the corresponding carrier density is $n = gE_F = 6.48 \times 10^{11} \text{ cm}^{-2}$, which is close to the value found from the transport measurement discussed above. Upon applying a fixed perpendicular magnetic field [Fig. 3(b)], the PL spectra exhibit periodic oscillations on the high-energy side corresponding to the different Landau levels being populated [53]. The period of the oscillations as a function of the magnetic field is plotted in Fig. 3(c) with the theoretical cyclotron energy $\omega_e = eB/\hbar m_e^*$ corresponding to the energy spacing between two consecutive

Landau levels of the first subband. The energies found experimentally are very close to the expected values, which confirms that only the lowest subband is occupied.

IV. QUANTUM TRANSPORT MEASUREMENTS

To complement the assessment of the heterostructure quality with a Hall bar and to verify the suitability for quantum transport experiments, we fabricated a GDQD on the thinned heterostructure membrane. Depletion Ti/Au (5 nm Ti, 20 nm Au) gates were patterned on the top side as shown in Fig. 4(a). The device was cooled to 35 mK and only the left part (sensor dot) was investigated. The conductance was measured with a standard low-frequency lock-in technique with an ac source-drain voltage between 80 and 150 μ V. Figure 4(b) shows the conductance through the sensor dot at fixed voltages V_T and V_B as a function of V_{SB} and V_{ST} , where the subscripts refer to the gate names shown in Fig. 4(a). In this regime, the device consists of a single large dot as Coulomb oscillations can be identified clearly. When the T and ST gate voltages V_T and V_{ST} are swept symmetrically with all other gates grounded [Fig. 4(c)], clear plateaus resulting from the quantization of the conductance can be resolved, which demonstrate that the two split gates behave as a quantum point contact.

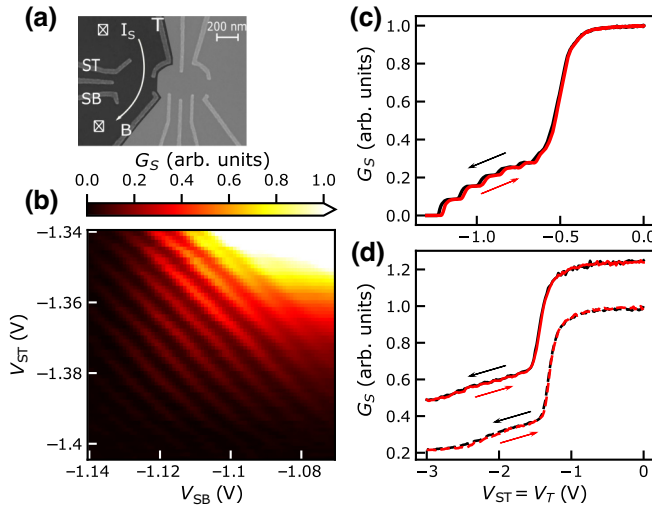


FIG. 4. (a) Scanning electron micrograph of the device. Only the left part of the device is used to form a quantum dot, which would be used for charge sensing when operating the full device. (b) Sensor dot conductance for fixed gate voltages $V_T = -1.5$ V and $V_B = -1.4$ V showing clean Coulomb oscillations. (c) Conductance G_S through the sensor dot when the two gates ST and T were swept symmetrically ($V_{SB} = V_B = 0$ V). (d) Sweep as in (c) but on a different wafer using gates on the unetched (solid lines, offset by 0.3 for clarity) and etched (dashed lines) side of the heterostructure. No qualitative difference can be seen, indicating the etching does not harm the transport properties of the structure.

To further investigate the influence of etching the heterostructure down to a thin membrane on the transport properties, the same gate pattern was fabricated once on the unetched side and once on the etched side with an in-plane offset of a few micrometers. This sample was fabricated on a heterostructure grown in an MBE system different from the one used for the heterostructure investigated earlier. Although nominally identical, variations in the dopant concentration, the layer thicknesses, the growth temperature, and the arsenic flux are expected due to the error margins in determining these parameters. Figure 4(d) shows the pinch-off behavior for the unetched (solid lines) and etched (dashed lines) sides for the lithographically identical pair of gates V_{ST} and V_T measured at 4 K. The curves are offset for clarity. While on this particular wafer the channel could not be completely pinched off even with much more negative voltages, there is no discernible difference between the data for the front and back sides of the membrane for all gate pairs of the devices, indicating that the etched surface does not deteriorate the electrical properties of the sample, for example due to increased interface defects introduced by surface roughness or chemical damage. In particular, these measurements as well as reference measurements on other heterostructures confirm that signs of hysteresis seen in Figs. 2(b) and 4(c) and other measurements on the same structure are related to the heterostructure itself rather than a consequence of the etching process.

V. EXCITON TRAP

The second key ingredient to implement an electrostatic exciton trap is the spatially localized electric field, which requires patterning of the gates on a much shorter length scale than in a Hall bar. To realize optical coupling to a gate-defined spin qubit, for example using the scheme described by Joecker *et al.* [27], this OAQD will ultimately have to be embedded next to the GDQD. Figure 5(a) shows the geometry of an isolated trapping dot. On each side of the heterostructure from same the wafer as characterized in Sec. III, two semitransparent metal gates are fabricated by electron-beam lithography: one circular gate called the central gate (diameter 150 nm) and one surrounding ring gate called the guard gate (diameter 1800 nm) separated by a 50-nm gap. The top central (guard) gate is vertically aligned with the bottom central (guard) gate.

The sample was characterized optically at 35 mK with the same optical setup as described in Sec. III. It was excited at 790 nm with an average power of 300 nW on the surface. Figure 5(b) shows the PL spectra measured as a function of the voltage applied to the top central gate V_{TC} with all other gates grounded. Until $V_{TC} = -1$ V, the gate voltage does not noticeably affect the QW emission energy centered around 1.52 eV. Despite the expected gradual depletion of the 2DEG, the electron density remains large enough in this range to screen the excitons [58]. As the gate

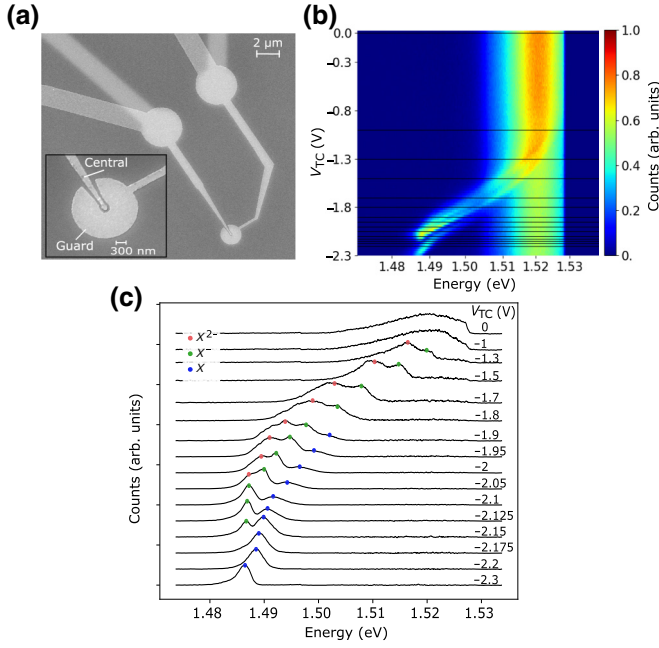


FIG. 5. (a) A scanning electron micrograph image of the central gates and the guard gates used to create the exciton trap. The same gates were also patterned on the top and bottom surface. (b) PL measurement at different top central gate V_{TC} voltage. All the other gates of the exciton trap were set to 0 V. (c) Normalized PL spectrum extracted from (b) (horizontal black lines) at various top central gate V_{TC} . Each spectrum has been shifted for clarity. The dots on the spectra identify the different exciton lines. The PL emission of the unbiased QW outside the metal gates ($V_{TC} = 0$ V) has been subtracted from all the spectra for $V_{TC} < -1$ V.

voltage decreases further from -1 V [$n_s \approx 1 \times 10^{11} \text{ cm}^{-2}$ according to Fig. 2(b)], the electron carrier density keeps decreasing to the stage where a transition from a populated to an empty well occurs. As a result, a strong Stark shift is observed. Note that the unbiased QW is always visible as well since the laser spot size is larger than the diameter of the top central gate.

To further examine the Stark shift effect, individual spectra from Fig. 5(b) are plotted in Fig. 5(c). Here, the PL of the unbiased QW outside the metal gate (corresponding to the spectrum at $V_{TC} = 0$ V) has been subtracted from the spectra for $V_{TC} < -1$ V for clarity. At $-2.1 < V_{TC} < -1.90$ V, three exciton lines gradually shifting to lower energies by the quantum-confined Stark effect can be identified. Following earlier polarization and photoluminescence studies carried out by Finkelstein *et al.* [58] on a doped GaAs QW, we propose the following peak identification. The carrier density still being large in that range, the heavy-hole exciton bound to two electrons X^{2-} and the heavy-hole exciton bound to one electron, also called a negative trion, X^- , dominate the spectrum. The heavy-hole neutral exciton X is only weakly observed. From $V_{TC} < -2.1$ V, the doubly charged exciton X^{2-} disappears

and only the trion X^- and the neutral exciton X remain distinctly separated on the spectrum. The X^- trion line originally dominates the neutral exciton X , and at $V_{TC} = -2.15$ V the intensity of the two peaks becomes comparable. From $V_{TC} < -2.175$ V, the trion peak vanishes and the neutral exciton peak eventually dominates the spectrum, showing that the 2DEG has been completely depleted. According to Fig. 2, we would expect the electron gas to be depleted around -1.5 V. The depletion occurs at larger voltages in Fig. 5 due to partial screening of the central gate voltage by the guard gate. At $V_{TC} = -2.2$ V, the neutral exciton X line is redshifted from the low-energy tail of the unbiased QW by 15 meV. A spatially localized exciton trap with a confinement potential of 15 meV is therefore formed under the central gate. Considering that the voltage applied on the top central gate was effective from -1 V, this energy is much lower than expected from simulation in an undoped material in Fig. 1(f), which we attribute to the presence of residual charges in the QW partially screening the electric field. From -2.2 V to -2.3 V, the linewidth at FWHM of the neutral exciton peak decreases by 0.8 meV, which originates from the depletion of the trap and reduction of the interaction between excitons. Similar behaviors are obtained when the bias is applied on the bottom central gate.

VI. CONCLUSION

In summary, we describe a process that allows the fabrication of fine gate structures with electron-beam lithography on both sides of a 220-nm-thick membrane containing a GaAs/(Al,Ga)As heterostructure. We show that removing the original GaAs substrate using wet etching and etch stops does not deteriorate the electrical and optical properties of the 2DEG hosted. Quantum point contacts and GDQDs with clean signatures of Coulomb blockade can be formed. Using an appropriate gate pattern on both sides, the exciton energy can be lowered locally by up to 15 meV. These results lay the technological foundations for more advanced experiments and devices uniting aspects from the field of quantum transport and semiconductor (quantum) optics. One specific motivation is the realization of a spin-photon interface for qubits hosted in gate-defined quantum dots. On the transport side, this will require the realization of single-electron quantum dots and qubit operation in membrane devices. The next steps for optical experiments are the verification of single-photon source properties and level structure of the exciton traps to confirm that an optically active quantum dot can indeed be formed. Subsequently, more complex devices combining both aspects must be realized.

ACKNOWLEDGMENTS

This work was funded by the European Research Council (ERC) under the European Union's Horizon 2020

research and innovation program (Grant Agreement No. 679342), by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Germany's Excellence Strategy—Cluster of Excellence Matter and Light for Quantum Computing (ML4Q) EXC 2004/1—390534769, and by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation)—328514164.

We acknowledge the support of the cleanroom Helmholtz Nano Facility (HNF) at Forschungszentrum Jülich, in particular Florian Lentz and Stefan Trellkamp for their support with the electron-beam lithography. Furthermore, we thank the Institut für Werkstoffe der Elektrotechnik (IWE 1) at RWTH Aachen University for giving us access to their flip-chip bonder and the Institute für Halbleitertechnik (IHT) at RWTH Aachen University for allowing us to use their laser marker.

C.Z., M.I.L., J.L., A.L., and A.D.W. grew prototype wafers and in particular the wafer used for this project. T.D. fabricated the devices. T.D. and R.O. developed the bonding technique. T.D. and F.L. designed the cryostat. T. D. measured the samples. T.H. performed additional transport measurements. T.D., S.K., and H.B. analyzed the data. H.B. and B.E.K. provided guidance on various aspects of the experiments. T.D. and H.B. wrote the manuscript with input from other authors.

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