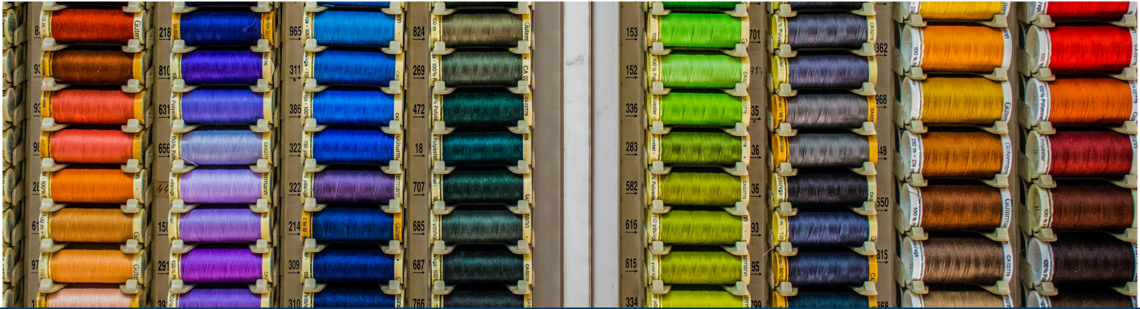

CUDA Introduction

GPU Programming *Foundations* 2023

17 April 2023 | Andreas Herten | Forschungszentrum Jülich

JÜLICH Forschungszentrum | JÜLICH SUPERCOMPUTING CENTRE

Outline

History of GPUs

A short but unparalleled story

1999 Graphics computation pipeline implemented in dedicated *graphics hardware*
Computations using OpenGL graphics library [2]
»GPU« coined by NVIDIA [3]

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*: *Effective* FLOP/s, *not theoretical peak*

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- *Soon* EU: JUPITER (≈ 1 EFLOP/s, JSC)
  US: Aurora (≈ 2 EFLOP/s, Argonne), Intel GPUs; El Capitan (≈ 2 EFLOP/s, LLNL), AMD GPUs

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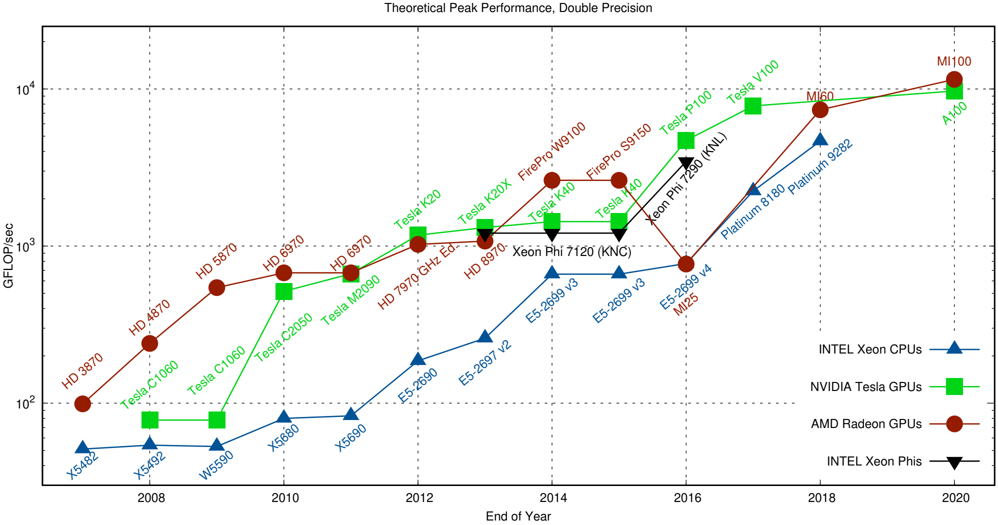
Status Quo Across Architectures

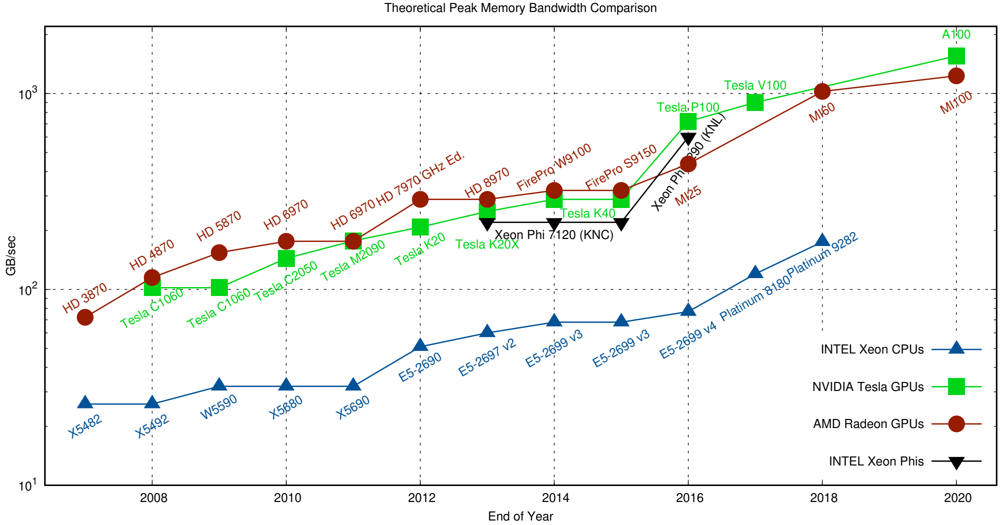
Performance



Graphic: Rupp [6]

Status Quo Across Architectures

Memory Bandwidth



Graphic: Rupp [6]

JUWELS Cluster – Jülich's Scalable System

- 2500 nodes with Intel Xeon CPUs (2×24 cores)
- $46 + 10$ nodes with 4 NVIDIA Tesla V100 cards (16 GB memory)
- 10.4 (CPU) + 1.6 (GPU) PFLOP/s peak performance (Top500: #86)

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JUWELS Booster – Scaling Higher!

- 936 nodes with AMD EPYC Rome CPUs (2 × 24 cores)
- Each with 4 NVIDIA A100 Ampere GPUs (each: *FP64TC:* 19.5 / *FP64:* 9.7 TFLOP/s, 40 GB memory)
- InfiniBand DragonFly+ HDR-200 network; 4 × 200 Gbit/s per node

TOP 500 The List.

Top500 List Nov 2020:

- #1 Europe
- #7 World
- #4* Top/Green500

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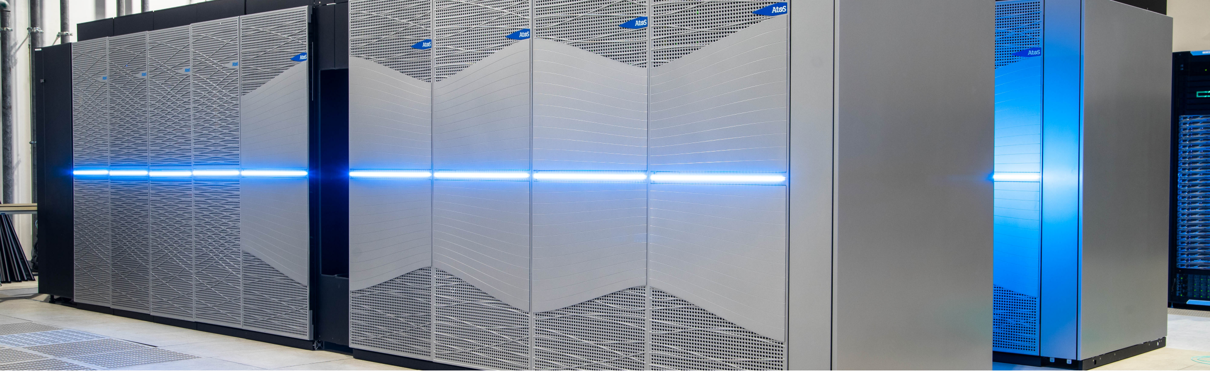

JURECA DC – Multi-Purpose

- 768 nodes with AMD EPYC Rome CPUs (2 $\times$ 64 cores)
- 192 nodes with 4 NVIDIA A100 Ampere GPUs
- InfiniBand DragonFly+ HDR-100 network

Getting GPU-Acquainted

Some Applications

TASK

Location of Code:

`1-Introduction-GPU-Programming/Tasks/getting-started`

See `Instructions.iypnb` for hints.

Make sure to have sourced the course environment!

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TASK

GEMM

N-Body

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Mandelbrot

Dot Product

Getting GPU-Acquainted

Some Applications

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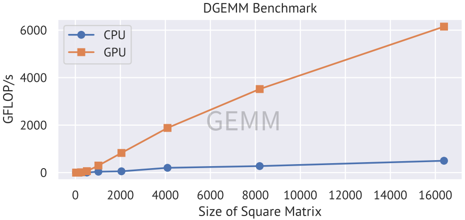
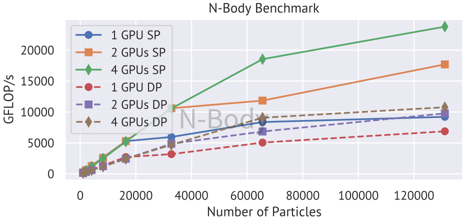
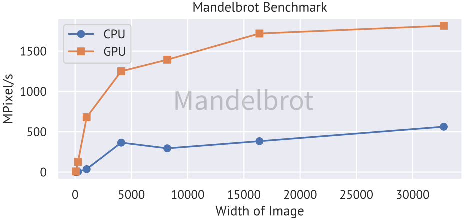
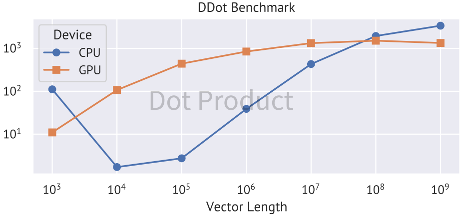








Platform

CPU vs. GPU

A matter of specialties

Graphics: Lee [7] and Shearings Holidays [8]

CPU vs. GPU

A matter of specialties

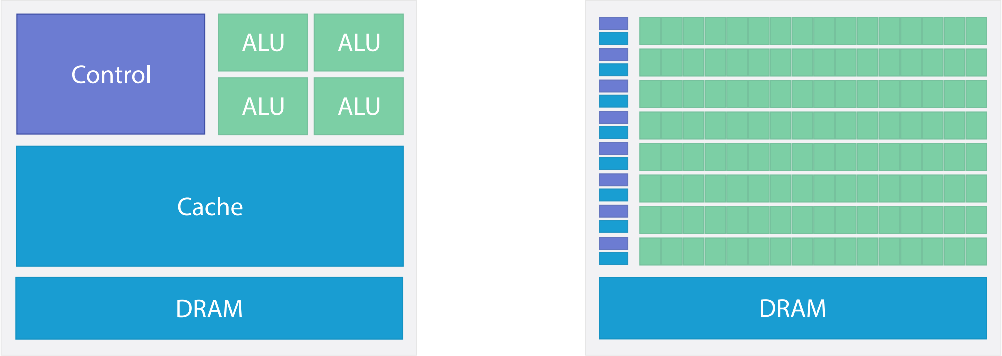
Transporting one

Transporting many

Graphics: Lee [7] and Shearings Holidays [8]

CPU vs. GPU

Chip



GPU Architecture

Overview

Aim: Hide Latency

Everything else follows

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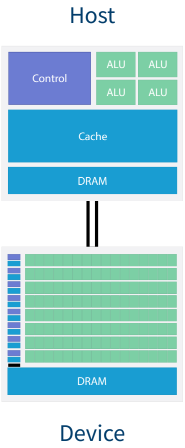
Memory

GPU memory ain't no CPU memory

- GPU: accelerator / extension card

→ Separate device from CPU



Memory

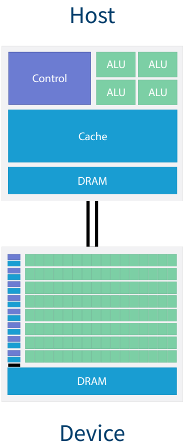
GPU memory ain't no CPU memory

Unified Virtual Addressing

- GPU: accelerator / extension card

→ Separate device from CPU

Separate memory, but UVA



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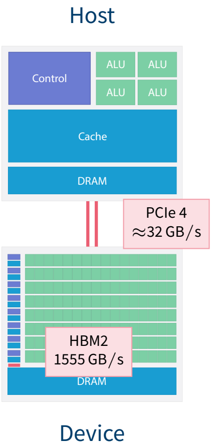

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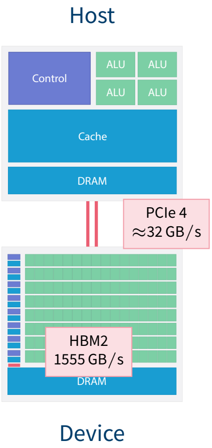
Separate memory, but UVA

- Memory transfers need special consideration!

Do as little as possible!



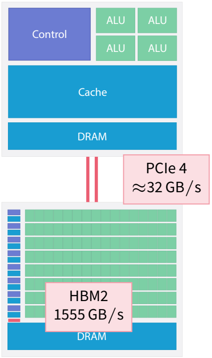
Memory

GPU memory ain't no CPU memory

Unified Memory

- GPU: accelerator / extension card
  → Separate device from CPU
  Separate memory, but UVA and UM
- Memory transfers need special consideration!
  Do as little as possible!
- Choice: automatic transfers (convenience) or manual transfers (control)

Host



Device

Memory

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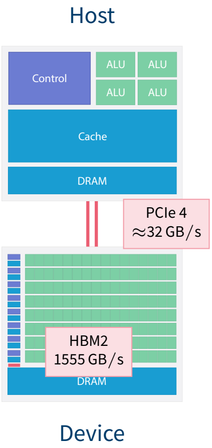

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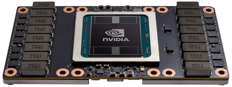
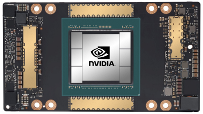
V100

32 GB RAM, 900 GB/s



A100

40 GB RAM, 1555 GB/s



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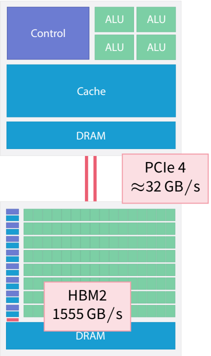
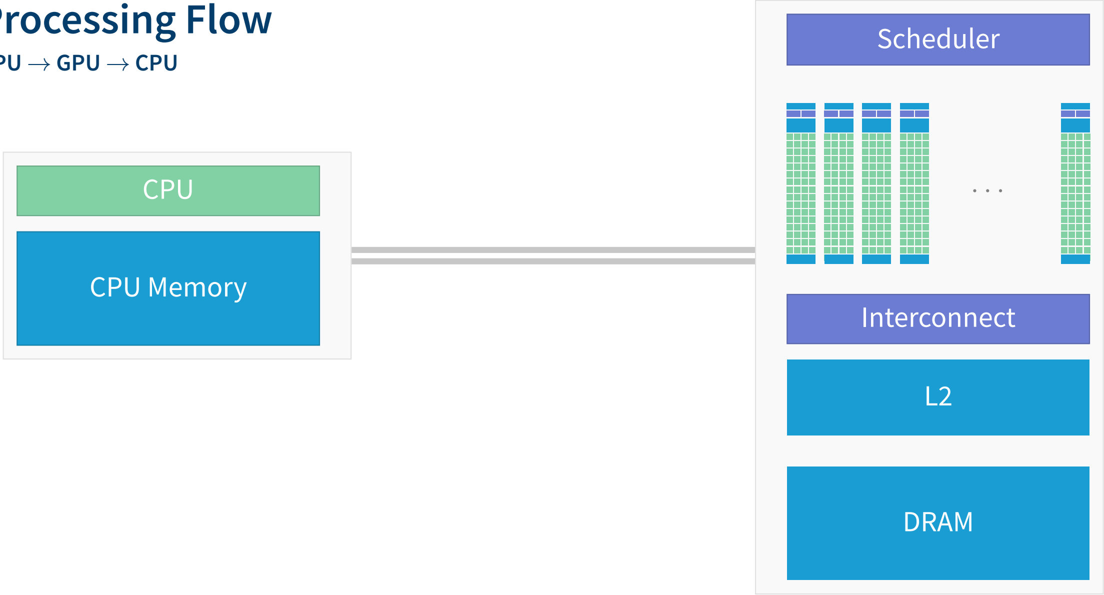


Device

Processing Flow

CPU → GPU → CPU



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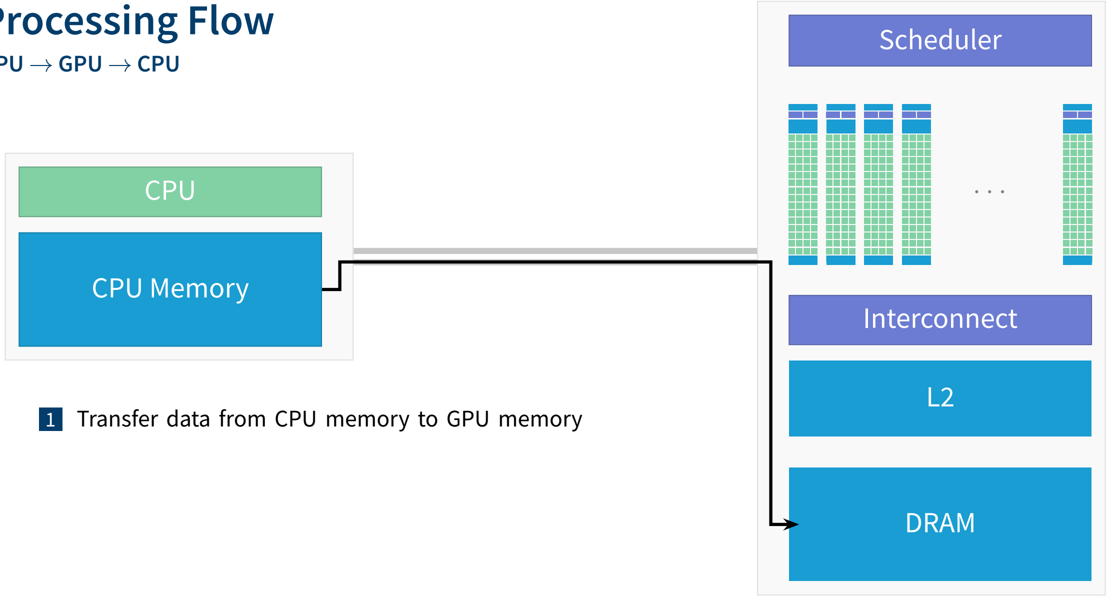

1. Transfer data from CPU memory to GPU memory

Processing Flow

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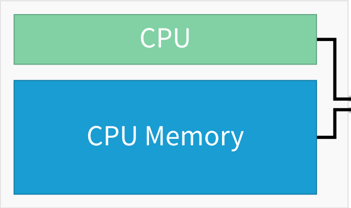

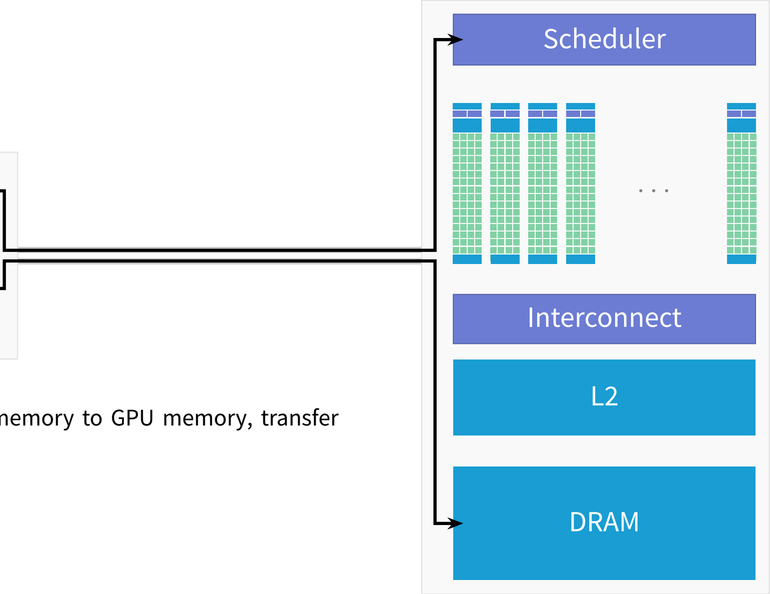

1. Transfer data from CPU memory to GPU memory, transfer program

Processing Flow

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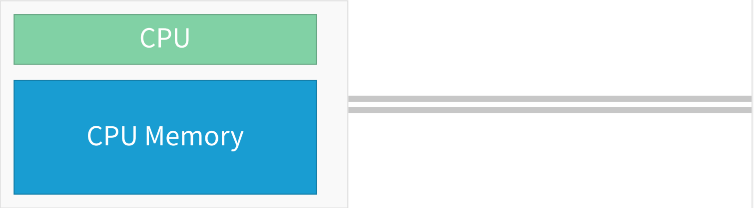

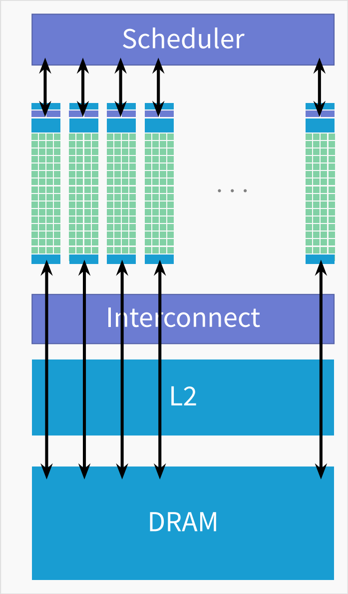

1. Transfer data from CPU memory to GPU memory, transfer program
2. Load GPU program, execute on SMs, get (cached) data from memory; write back

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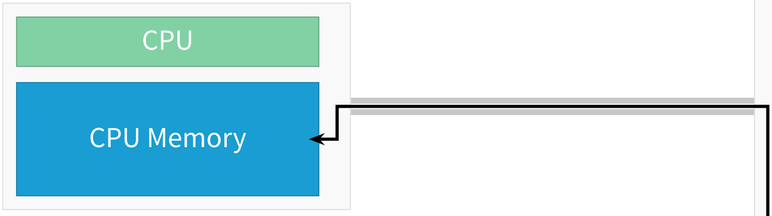

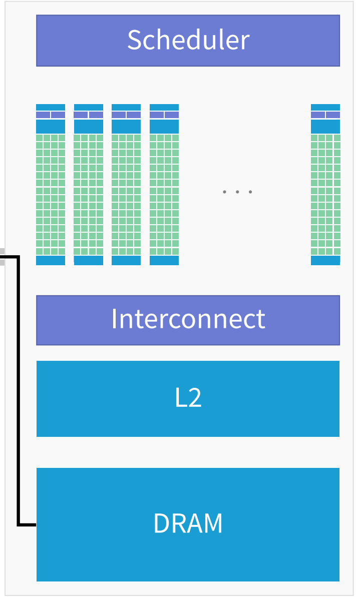

1. Transfer data from CPU memory to GPU memory, transfer program
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3. Transfer results back to host memory

GPU Architecture

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Aim: Hide Latency

Everything else follows

SIMT

Asynchronicity

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Async

Following different streams

- Problem: Memory transfer is comparably slow
  Solution: Do something else in meantime (**computation**)!

→ Overlap tasks

- Copy and compute engines run separately (*streams*)

- GPU needs to be fed: Schedule many computations
- CPU can do other work while GPU computes; synchronization

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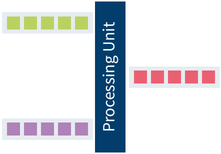
  SISD Single Instruction, Single Data

Flynn’s Taxonomy

SISD



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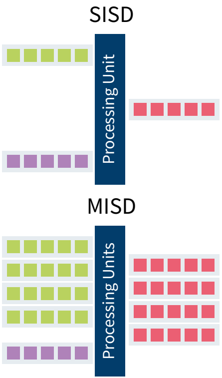

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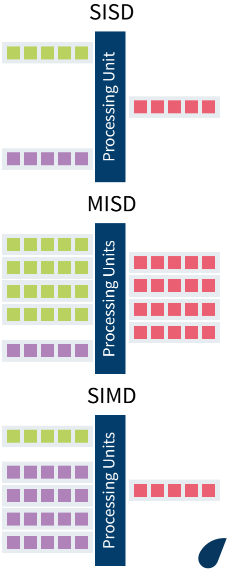
  SISD Single Instruction, Single Data
  MISD Multiple Instructions, Single Data
  SIMD Single Instruction, Multiple Data



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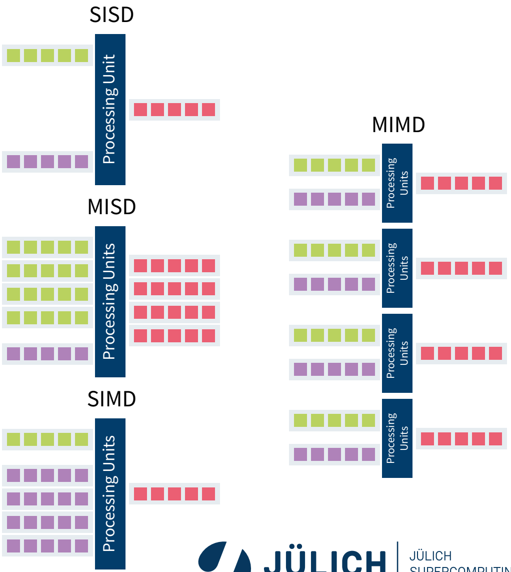

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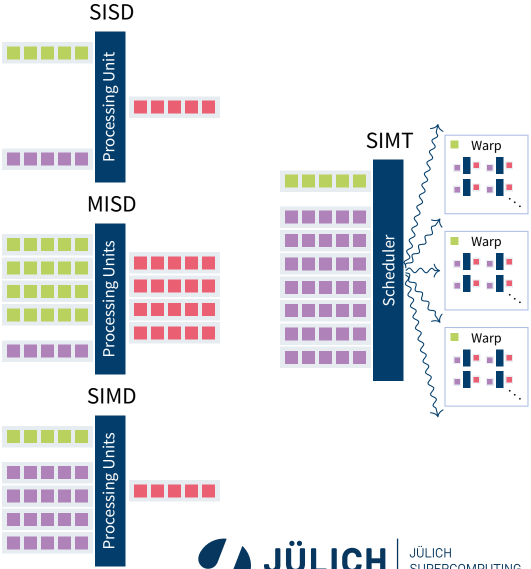
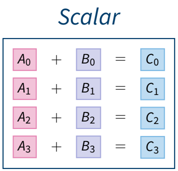
SIMT	Single Instruction, Multiple *Threads*



SIMT

SIMT $=$ SIMD $\oplus$ SMT

- CPU:
  - Single Instruction, Multiple Data (SIMD)



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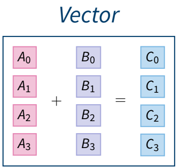

SIMT

SIMT $=$ SIMD $\oplus$ SMT

- CPU:
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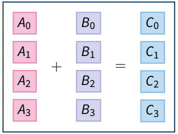
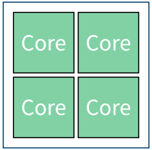
  - Simultaneous Multithreading (SMT)

Vector





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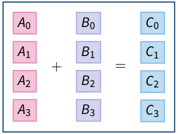
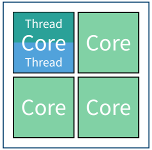


SMT



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SIMT

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- CPU:
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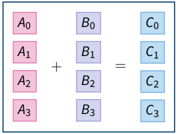
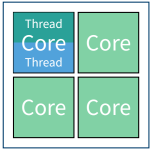
  - Simultaneous Multithreading (SMT)
- GPU: Single Instruction, Multiple Threads (SIMT)

Vector



SMT



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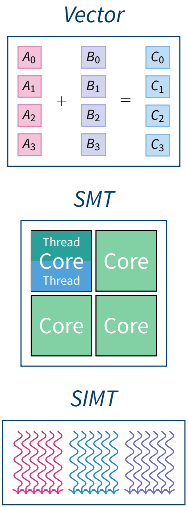

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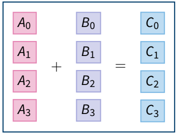
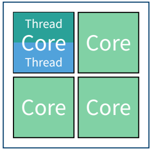
SIMT $=$ SIMD $\oplus$ SMT

- CPU:
  - Single Instruction, Multiple Data (SIMD)
  - Simultaneous Multithreading (SMT)
- GPU: Single Instruction, Multiple Threads (SIMT)
  - CPU core $\approxeq$ GPU multiprocessor (SM)
  - Working unit: set of threads (32, a *warp*)
  - Fast switching of threads (large register file)
  - Branching 

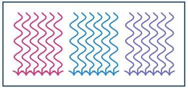
Vector



SMT

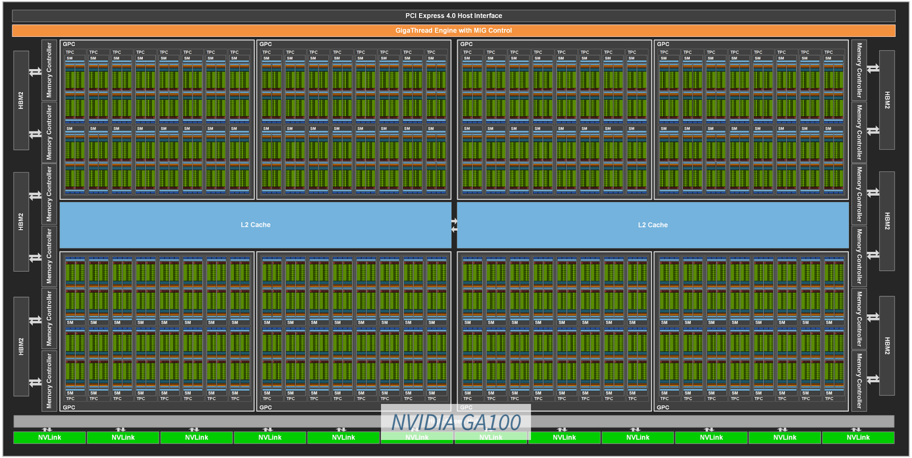


SIMT



SIMT

SIMT $=$ SIMD $\oplus$ SMT



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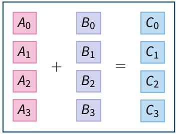

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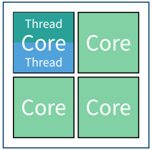

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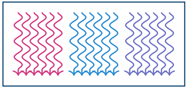

Graphics: img:amperepictures

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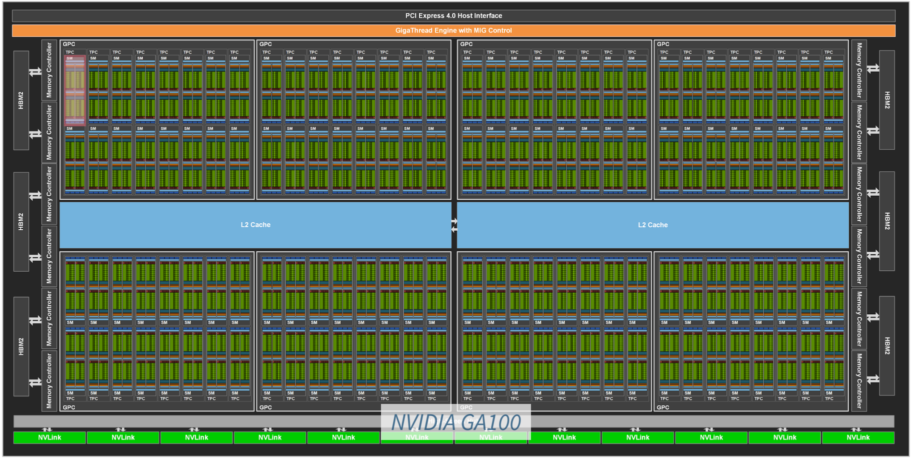

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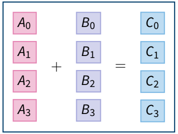

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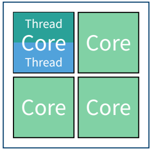

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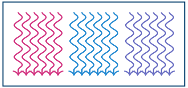

Graphics: img:amperepictures

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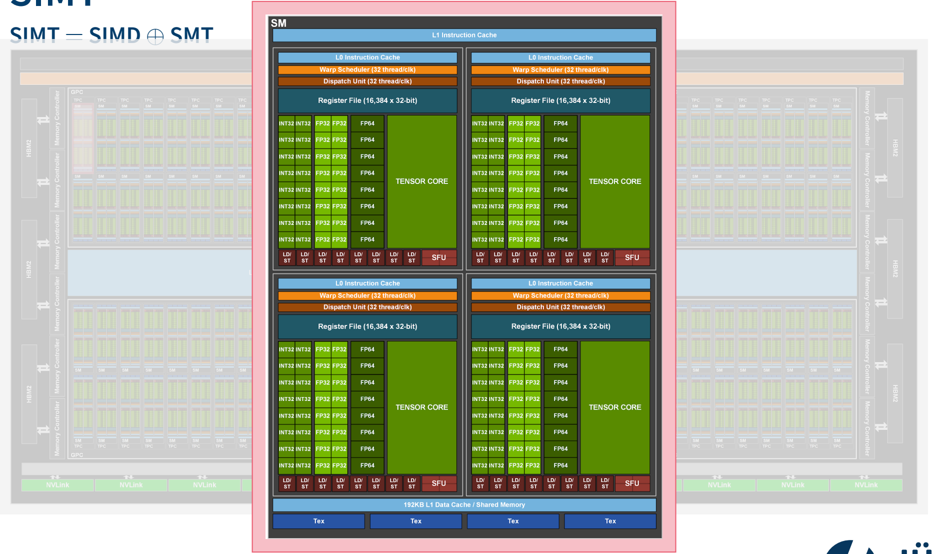
SIMT

SIMT = SIMD $\oplus$ SMT

Multiprocessor



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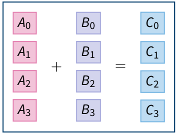

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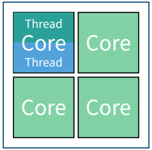

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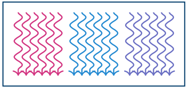
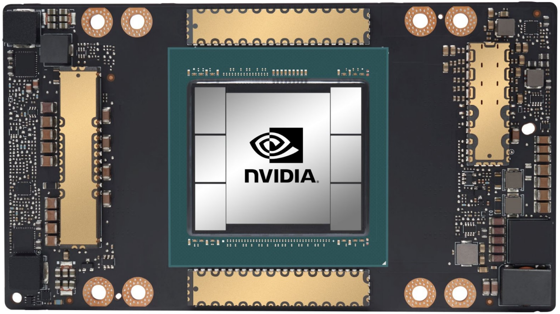


Graphics: img:amperepictures

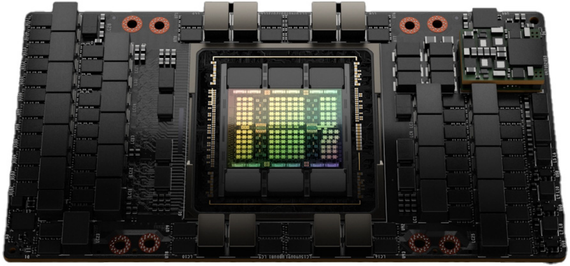
A100 vs H100

Comparison of current vs. next generation

A100



H100



A100 vs H100

Comparison of current vs. next generation

A100

H100

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A100 vs H100

Comparison of current vs. next generation

A100

H100

Low Latency vs. High Throughput

Maybe GPU's ultimate feature

CPU Minimizes latency within each thread

GPU Hides latency with computations from other thread warps

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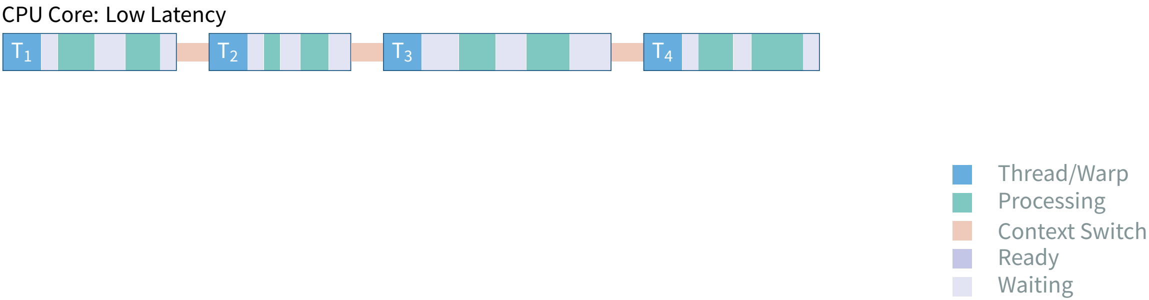

Low Latency vs. High Throughput

Maybe GPU’s ultimate feature

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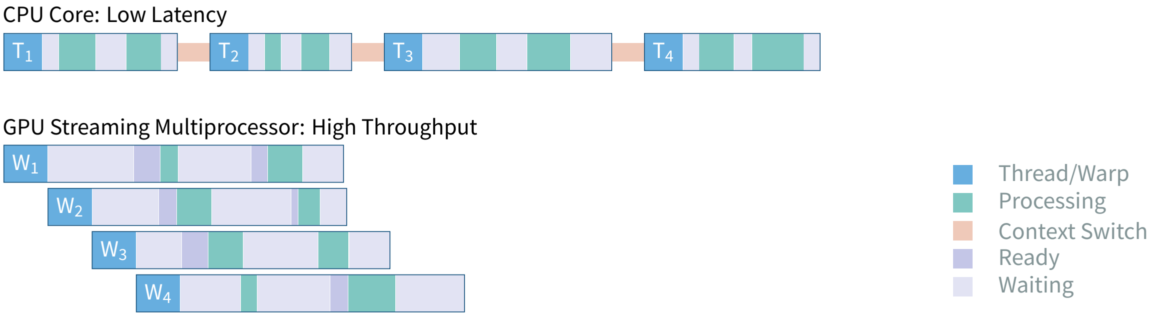
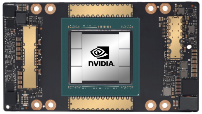


CPU vs. GPU

Let's summarize this!

Optimized for **low latency**

+ Large main memory
+ Fast clock rate
+ Large caches
+ Branch prediction
+ Powerful ALU
– Relatively low memory bandwidth
– Cache misses costly
– Low performance per watt



Optimized for **high throughput**

+ High bandwidth main memory
+ Latency tolerant (parallelism)
+ More compute resources
+ High performance per watt
– Limited memory capacity
– Low per-thread performance
– Extension card

Programming GPUs

Preface: CPU

A simple CPU program!

SAXPY: $\vec{y} = a\vec{x} + \vec{y}$, with single precision

Part of LAPACK BLAS Level 1

```c
void saxpy(int n, float a, float * x, float * y) {
  for (int i = 0; i < n; i++)
    y[i] = a * x[i] + y[i];
}

int a = 42;
int n = 10;
float x[n], y[n];
// fill x, y

saxpy(n, a, x, y);
```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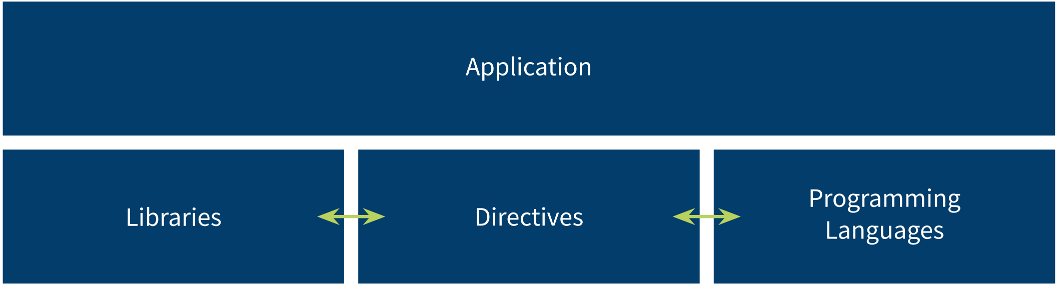
Summary of Acceleration Possibilities



Drop-in
Acceleration

Easy
Acceleration

Flexible
Acceleration

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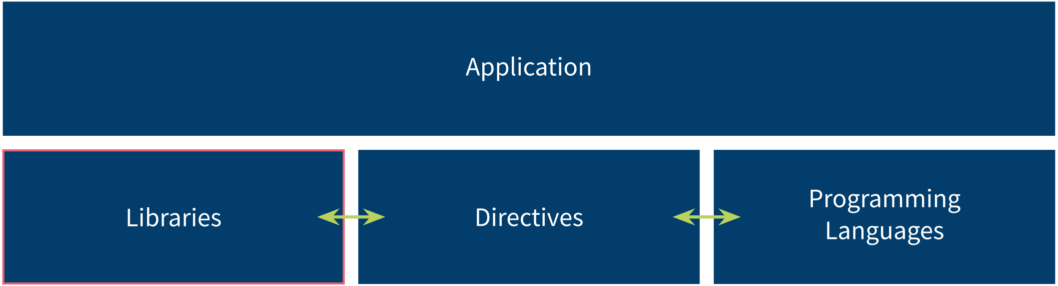
Summary of Acceleration Possibilities



Drop-in Acceleration

Easy Acceleration

Flexible Acceleration

Libraries

Programming GPUs is easy: Just don't!

Libraries

Programming GPUs is easy: Just don’t!

Use applications & libraries

Libraries

Programming GPUs is easy: Just don't!

Use applications & libraries

Wizard: Breazell [9]

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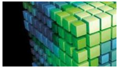
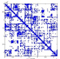
Libraries

Programming GPUs is easy: **Just don't!**

Use applications & libraries

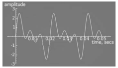


cuBLAS

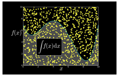


cuSPARSE

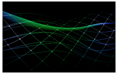
cuDNN



cuFFT



cuRAND



CUDA Math

OpenCV

Thrust

ArrayFire

Numba

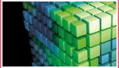
CuPy

Wizard: Breazell [9]

Libraries

Programming GPUs is easy: Just don't!

Use applications & libraries



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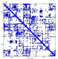

cuSPARSE

cuDNN

OpenCV

{A} ArrayFire

Thrust

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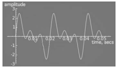

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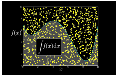

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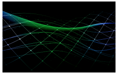

CUDA Math

Wizard: Breazell [9]

cuBLAS

Parallel algebra

- GPU-parallel BLAS (all 152 routines)
- Single, double, complex data types
- Constant competition with Intel's MKL
- Multi-GPU support

→ https://developer.nvidia.com/cublas
http://docs.nvidia.com/cuda/cublas

cuBLAS

Code example

```
int a = 42;  int n = 10;
float x[n], y[n];
// fill x, y

cublasHandle_t handle;
cublasCreate(&handle);

float * d_x, * d_y;
cudaMallocManaged(&d_x, n * sizeof(x[0]));
cudaMallocManaged(&d_y, n * sizeof(y[0]));

cublasSaxpy(handle, n, a, d_x, 1, d_y, 1);

cublasGetVector(n, sizeof(y[0]), d_y, 1, y, 1);

cudaFree(d_x); cudaFree(d_y);
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```

cuBLAS

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Initialize

cuBLAS

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Initialize

Allocate GPU memory

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Initialize

Allocate GPU memory

Call BLAS routine

cuBLAS

Code example

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Initialize

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Call BLAS routine

Copy result to host

cuBLAS

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cudaFree(d_x); cudaFree(d_y);
cublasDestroy(handle);
```

- `cublasCreate(&handle);` — Initialize
- `cudaMallocManaged(...)` — Allocate GPU memory
- `cublasSaxpy(...)` — Call BLAS routine
- `cublasGetVector(...)` — Copy result to host
- `cublasDestroy(handle);` — Finalize

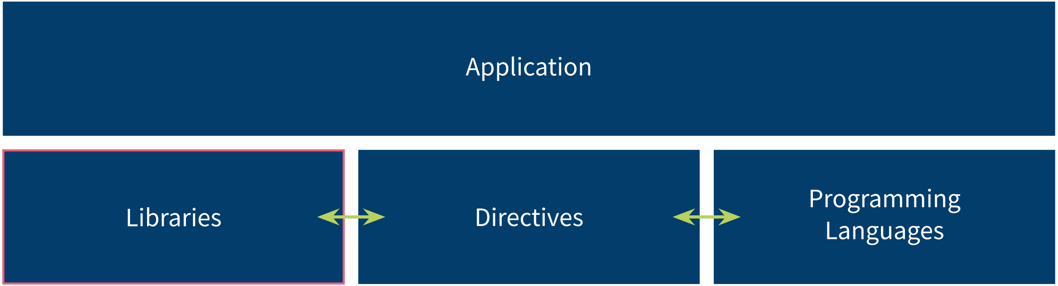
cuBLAS Task

TASK

Implement a matrix-matrix multiplication

- Location of code: `01-Basics/exercises/tasks/02-cuBLAS`
- Look at `Instructions.ipynb` Notebook for instructions
  1. Implement call to double-precision GEMM of cuBLAS
  2. Build with `make` (load modules of this task via `source setup.sh`!)
  3. Run with `make run`
- Check cuBLAS documentation for details on `cublasDgemm()`

Summary of Acceleration Possibilities



Drop-in
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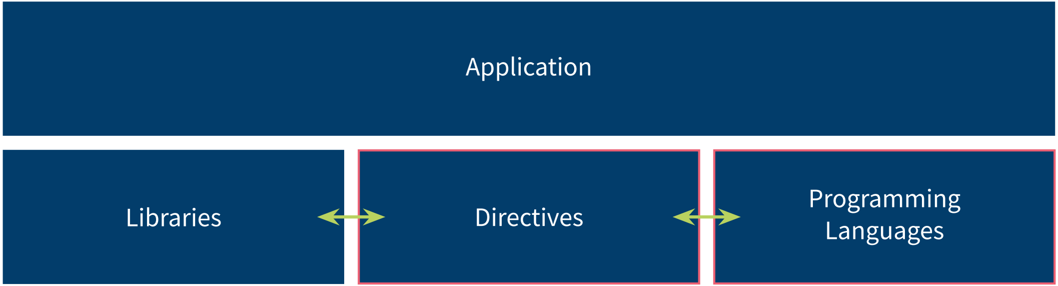

Drop-in Acceleration

Easy Acceleration

Flexible Acceleration

Parallelism

Libraries are not enough?

You think you want to write your own GPU code?

Primer on Parallel Scaling

Amdahl's Law

Possible maximum speedup for
N parallel processors

Total Time $t = t_{\textbf{s}\text{erial}} + t_{\textbf{p}\text{arallel}}$

Primer on Parallel Scaling

Amdahl's Law

Possible maximum speedup for N parallel processors

Total Time $t = t_{\textbf{serial}} + t_{\textbf{parallel}}$

N Processors $t(N) = t_s + t_p/N$

Primer on Parallel Scaling

Amdahl's Law

Possible maximum speedup for N parallel processors

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Speedup $s(N) = t/t(N) = \frac{t_s+t_p}{t_s+t_p/N}$

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Amdahl's Law

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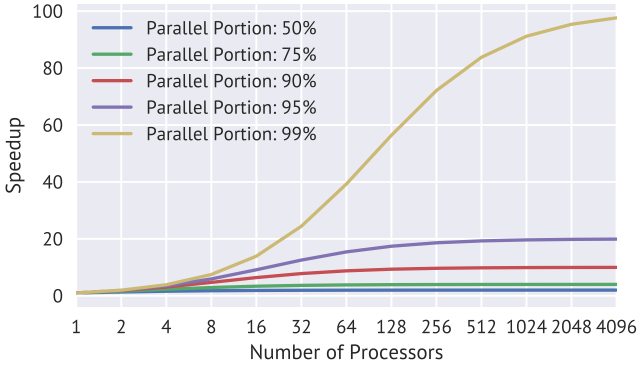

⚠ Parallelism

Parallel programming is not easy!

Things to consider:

- Is my application **computationally intensive** *enough*?
- What are the levels of **parallelism**?
- How much **data** needs to be **transferred**?
- Is the **gain** worth the pain?

Alternatives

The twilight

There are alternatives to CUDA C, which **can** ease the *pain*…

- OpenACC, OpenMP
- Thrust
- Kokkos, RAJA, ALPAKA, SYCL, DPC++, pSTL
- PyCUDA, Cupy, Numba

Other alternatives

- CUDA Fortran
- HIP
- OpenCL

Programming GPUs

Directives

GPU Programming with Directives

Keepin' you portable

- Annotate serial source code by directives

```
#pragma acc loop
for (int i = 0; i < 1; i++) {};
```

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Keepin' you portable

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- **OpenACC**: Especially for GPUs; **OpenMP**: Has GPU support
- Compiler interprets directives, creates according instructions

GPU Programming with Directives

Keepin' you portable

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```

- **OpenACC**: Especially for GPUs; **OpenMP**: Has GPU support
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Pro

- Portability
  - Other compiler? No problem! To it, it's a serial program
  - Different target architectures from same code
- Easy to program

Con

- Only few compilers
- Not all the raw power available
- A little harder to debug

GPU Programming with Directives

The power of… two.

OpenMP Standard for multithread programming on CPU, GPU since 4.0, better since 4.5

```
#pragma omp target map(tofrom:y), map(to:x)
#pragma omp teams num_teams(10) num_threads(10)
#pragma omp distribute
for (   ) {
    #pragma omp parallel for
    for (   ) {
    // …
    }
}
```

OpenACC Similar to OpenMP, but more specifically for GPUs

For C/C++ and Fortran

OpenACC

Code example

```c
void saxpy_acc(int n, float a, float * x, float * y) {
  #pragma acc kernels
  for (int i = 0; i < n; i++)
    y[i] = a * x[i] + y[i];
}

int a = 42;
int n = 10;
float x[n], y[n];
// fill x, y

saxpy_acc(n, a, x, y);
```

OpenACC

Code example

```
void saxpy_acc(int n, float a, float * x, float * y) {
  #pragma acc parallel loop copy(y) copyin(x)
  for (int i = 0; i < n; i++)
    y[i] = a * x[i] + y[i];
}

int a = 42;
int n = 10;
float x[n], y[n];
// fill x, y

saxpy_acc(n, a, x, y);
```

Programming GPUs

Thrust

Thrust

Iterators! Iterators everywhere! 🚀

- $\frac{\text{Thrust}}{\text{CUDA}} = \frac{\text{STL}}{\text{C++}}$
- Template library
- *A precursor to a GPU-accelerated pSTL?*
- Based on iterators
- Data-parallel primitives (`scan()`, `sort()`, `reduce()`, ...)
- Fully compatible with plain CUDA C (comes with CUDA Toolkit)
- Great with `[](){}` lambdas!

→ `http://thrust.github.io/`
`http://docs.nvidia.com/cuda/thrust/`

Thrust

Code example

```
int a = 42;
int n = 10;
thrust::host_vector<float> x(n), y(n);
// fill x, y

thrust::device_vector d_x = x, d_y = y;
thrust::transform(d_x.begin(), d_x.end(), d_y.begin(), d_y.begin(), [=]
↪  __device__ (auto x, auto y) {return a*x+y;});
// or:
using namespace thrust::placeholders;
thrust::transform(d_x.begin(), d_x.end(), d_y.begin(), d_y.begin(), a * _1 +
↪  _2);

x = d_x;
```


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Thrust Task

TASK

Let's sort some randomness

- Location of code: `01-Basics/exercises/tasks/03-Thrust`
- Look at `Instructions.ipynb` for instructions
  1. Sort random numbers with Thrust on CPU and GPU
  2. Build with `make`
     Reset environment to original; call `source setup.sh` or re-login!
  3. Run with `make run`
- Check Thrust documentation for details on `thrust::sort()`

Summary of Acceleration Possibilities

Application

Libraries ↔ Directives ↔ Programming Languages

Drop-in Acceleration

Easy Acceleration

Flexible Acceleration

Programming GPUs

CUDA C/C++

CUDA SAXPY

With runtime-managed data transfers

```
__global__ void saxpy_cuda(int n, float a, float * x, float * y) {
  int i = blockIdx.x * blockDim.x + threadIdx.x;
  if (i < n)
    y[i] = a * x[i] + y[i];
}

int a = 42;
int n = 10;
float x[n], y[n];
// fill x, y
cudaMallocManaged(&x, n * sizeof(float));
cudaMallocManaged(&y, n * sizeof(float));

saxpy_cuda<<<2, 5>>>(n, a, x, y);

cudaDeviceSynchronize();
```

CUDA’s Parallel Model

In software: Threads, Blocks

- Methods to exploit parallelism:

CUDA’s Parallel Model

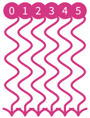
In software: Threads, Blocks

- Methods to exploit parallelism:
  - Thread

CUDA’s Parallel Model

In software: Threads, Blocks

- Methods to exploit parallelism:
    - Threads



CUDA's Parallel Model

In software: Threads, Blocks

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CUDA’s Parallel Model

In software: Threads, Blocks

- Methods to exploit parallelism:
  - Threads → Block
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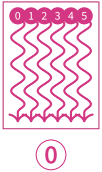

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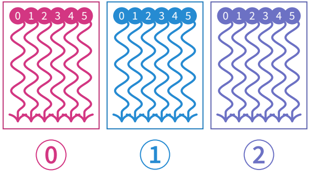
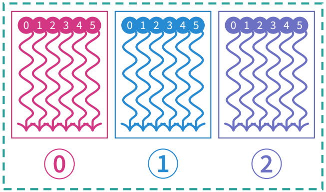


CUDA’s Parallel Model

In software: Threads, Blocks

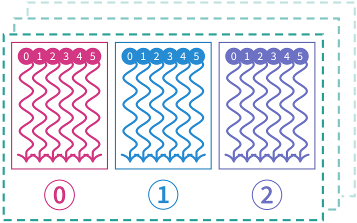
- Methods to exploit parallelism:
  - Threads → Block
  - Blocks → Grid



CUDA’s Parallel Model

In software: Threads, Blocks

- Methods to exploit parallelism:
  - Threads → Block
  - Blocks → Grid
  - Threads & blocks in 3D



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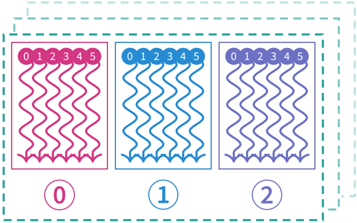

- Parallel function: **kernel**
  - `__global__ kernel(int a, float * b) { }`
  - Access own ID by global variables `threadIdx.x`, `blockIdx.y`, …
- Execution entity: **threads**
  - Lightweight → fast switching!
  - 1000s threads execute simultaneously → order non-deterministic!

Kernel Functions

- Kernel: Parallel GPU function
    - Executed by each thread
    - In parallel
    - Called from host or device

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Kernel Functions

- Kernel: Parallel GPU function
  - Executed by each thread
  - In parallel
  - Called from host or device
- All threads execute same code; but can take different paths in program flow (some penalty)
- Info about thread: local, global IDs

```
int currentThreadId = threadIdx.x;
float x = input[currentThreadId];
output[currentThreadId] = x*x;
```

Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops

```
void scale(float scale, float * in, float * out, int N) {
    for (int i = 0; i < N; i++)
        out[i] = scale * in[i];
}
```

Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops

```
void scale(float scale, float * in, float * out, int N) {
    for (
        int i = 0;
        i < N;
        i++
    )
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```

Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index

```
void scale(float scale, float * in, float * out, int N) {
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Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index | Extract Termination Condition

```
void scale(float scale, float * in, float * out, int N) {
    int i = 0;
    for ( ;
          ;
          i++
    )
        if (i < N)
            out[i] = scale * in[i];
}
```

Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index | Extract Termination Condition | Remove for

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Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index | Extract Termination Condition | Remove for | Add global

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__global__ void scale(float scale, float * in, float * out, int N) {
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Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index | Extract Termination Condition | Remove for | Add global | Replace i by threadIdx.x

```
__global__ void scale(float scale, float * in, float * out, int N) {
    int i = threadIdx.x;




        if (i < N)
            out[i] = scale * in[i];
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```


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Kernel Conversion

Recipe for C Function → CUDA Kernel

Identify Loops | Extract Index | Extract Termination Condition | Remove `for` | Add `global`

Replace `i` by `threadIdx.x` | … including block configuration

```
__global__ void scale(float scale, float * in, float * out, int N) {
    int i = threadIdx.x + blockIdx.x * blockDim.x;




        if (i < N)
            out[i] = scale * in[i];
}
```

Kernel Conversion

Summary

- C function with explicit loop

```
void scale(float scale, float * in, float * out, int N) {
    for (int i = 0; i < N; i++)
        out[i] = scale * in[i];
}
```

- CUDA kernel with implicit loop

```
__global__ void scale(float scale, float * in, float * out, int N) {
    int i = threadIdx.x + blockIdx.x * blockDim.x;
    if (i < N)
        out[i] = scale * in[i];
}
```

Kernel Launch

```
kernel<<<int gridDim, int blockDim>>>(...)
```

- Parallel threads of kernel launched with *triple-chevron syntax*
- Total number of threads, divided into
  - Number of blocks on the grid (`gridDim`)
  - Number of threads per block (`blockDim`)

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- Example:

```
int nThreads = 32;
scale<<<N/nThreads, nThreads>>>(23, in, out, N)
```

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- Example:

```
int nThreads = 32;
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```

- Possibility for too many threads; include termination condition into kernel!

Full Kernel Launch

For Reference

```
kernel<<<dim3 gD, dim3 bD, size_t shared, cudaStream_t stream>>>(...)
```

- 2 additional, optional parameters

Full Kernel Launch

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kernel<<<dim3 gD, dim3 bD, size_t shared, cudaStream_t stream>>>(...)
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`shared` Dynamic **shared memory**

- Small GPU memory space; share data in block (high bandwidth)
- Shared memory: allocate statically (compile time) or dynamically (run time)
- `size_t shared`: bytes of shared memory allocated per block (in addition to static shared memory)

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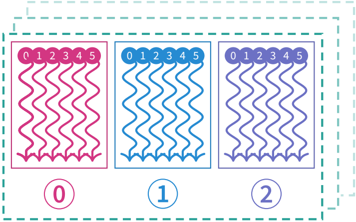
`stream` Associated **CUDA stream**

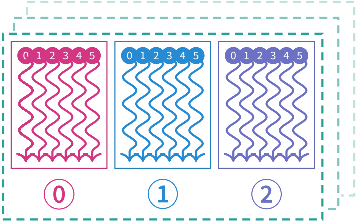
- CUDA streams enable different channels of communication with GPU
- Can overlap in some cases (communication, computation)
- `cudaStream_t stream`: ID of stream to use for this kernel launch

Grid Dimensions

- Threads & blocks in 3D



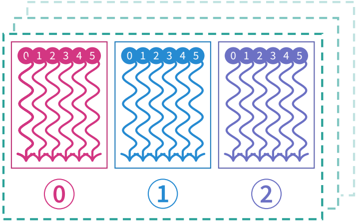
Grid Dimensions



- Threads & blocks in 3D
- Create 3D configurations with `struct dim3`

```
dim3 blockOrGridDim(size_t dimX, size_t dimY, size_t dimZ)
```

Grid Dimensions



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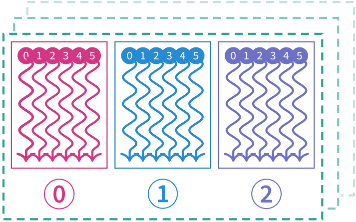
dim3 blockOrGridDim(size_t dimX, size_t dimY, size_t dimZ)
```

- Example:

```
dim3 blockDim(32, 32);
dim3 gridDim = {1000, 100};
```

Grid Dimensions



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```

- Example:

```
dim3 blockDim(32, 32);
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```

- Kernel call with `dim3`

```
kernel<<<dim3 gridDim, dim3 blockDim>>>(...)
```

Grid Sizes

- Block and grid sizes are hardware-dependent

Grid Sizes

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- For JSC GPUs: Tesla V100, A100

Block
- $\vec{N}_{\text{Thread}} \leq (1024_{\text{x}}, 1024_{\text{y}}, 64_{\text{z}})$
- $|\vec{N}_{\text{Thread}}| = N_{\text{Thread}} \leq 1024$

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Grid
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- Find out yourself: `deviceQuery` example from CUDA Samples

Grid Sizes

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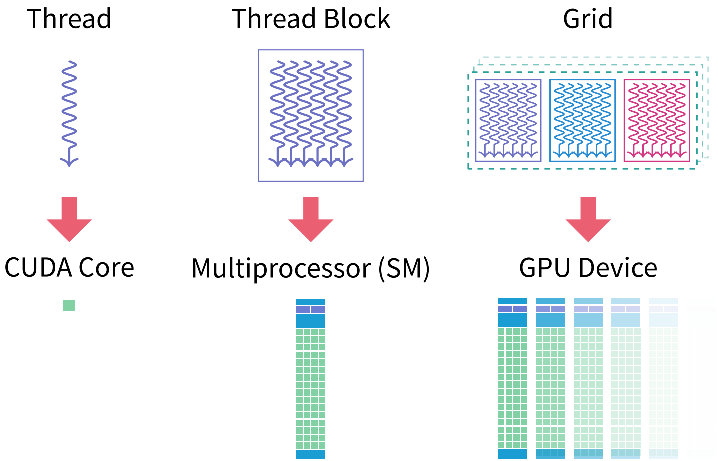
  Block
  - $\vec{N}_{\text{Thread}} \leq (1024_x, 1024_y, 64_z)$
  - $|\vec{N}_{\text{Thread}}| = N_{\text{Thread}} \leq 1024$

  Grid
  - $\vec{N}_{\text{Blocks}} \leq (2147483647_x, 65535_y, 65535_z) = (2^{31}, 2^{16}, 2^{16}) - \vec{1}$
- Find out yourself: `deviceQuery` example from CUDA Samples
- Workflow: Chose 128 or 256 as block dim; calculate grid dim from problem size

```
int Nx = 1000, Ny = 1000;
dim3 blockDim(16, 16);
int gx = (Nx % blockDim.x == 0)  Nx / blockDim.x : Nx / blockDim.x + 1;
int gy = (Ny % blockDim.y == 0)  Ny / blockDim.y : Ny / blockDim.y + 1;
dim3 gridDim(gx, gy);
kernel<<<gridDim, blockDim>>>();
```

Hardware Threads

Mapping Software Threads to Hardware



Memory Management

With Automated Transfers

- Allocate memory to be used on GPU or CPU

```
cudaMallocManaged(T** ptr, size_t nBytes)
```

- Data is copied to GPU or to CPU automatically *(managed)*

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```
float * a;
int N = 2048;
cudaMallocManaged(&a, N * sizeof(float));
```

Memory Management

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- Allocate memory to be used on GPU or CPU

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```

- Data is copied to GPU or to CPU automatically *(managed)*
- Example:

```
float * a;
int N = 2048;
cudaMallocManaged(&a, N * sizeof(float));
```

- Free device memory

```
cudaFree(void* ptr)
```

Memory Management

With Manual Transfers

- Allocate memory to be used on GPU

```
cudaMalloc(T** ptr, size_t nBytes)
```

Memory Management

With Manual Transfers

- Allocate memory to be used on GPU

```
cudaMalloc(T** ptr, size_t nBytes)
```

- Copy data between host ↔ device

```
cudaMemcpy(void* dst, void* src, size_t nByte, enum cudaMemcpyKind dir)
```

Memory Management

With Manual Transfers

- Allocate memory to be used on GPU

```
cudaMalloc(T** ptr, size_t nBytes)
```

- Copy data between host $\leftrightarrow$ device

```
cudaMemcpy(void* dst, void* src, size_t nByte, enum cudaMemcpyKind dir)
```

- Example:

```
float * a, * a_d;
int N = 2048;
// fill a
cudaMalloc(&a_d, N * sizeof(float));
cudaMemcpy(a_d, a,   N * sizeof(float), cudaMemcpyHostToDevice);
kernel<<<1,1>>>(a_d, N);
cudaMemcpy(a   , a_d, N * sizeof(float), cudaMemcpyDeviceToHost);
```

Task: Scale Vector

TASK

Work on an Array of Data

- Location of code: `01-Basics/exercises/tasks/04-Scale-Vector`
- Look at `Instructions.ipynb` for instructions
  1. Implement the whole CUDA flow (allocation, kernel configuration, kernel launch)
  2. Build with `make`
  3. Run with `make run`
- Additional task: Look at the version with explicit transfers (`_et`)

Task: Jacobi

TASK

Implement Manual Memory Handling

- Location of code:
  `01-Basics/exercises/tasks/05-Jacobi-Explicit-Transfers`
- Look at `Instructions.ipynb` for instructions
  1. Port the application from Unified Memory to manual memory handling
  2. Build with `make`
  3. Run with `make run`

Unified Memory

Overview

- Everything started with manual data management
- First Unified Memory since CUDA 6.0
- Better Unified Memory better since CUDA 8.0
- Now: Unified Memory great default, explicit memory only a possible optimization

Manual Memory vs. Unified Memory

```
void sortfile(FILE *fp, int N) {
    char *data;
    char *data_d;

    data = (char *)malloc(N);
    cudaMalloc(&data_d, N);

    fread(data, 1, N, fp);

    cudaMemcpy(data_d, data, N, cudaMemcpyHostToDevice);
    kernel<<<...>>>(data, N);

    cudaMemcpy(data, data_d, N, cudaMemcpyDeviceToHost);
    host_func(data)
    cudaFree(data_d); free(data);
}
```

```
void sortfile(FILE *fp, int N) {
    char *data;


    cudaMallocManaged(&data, N);


    fread(data, 1, N, fp);


    kernel<<<...>>>(data, N);
    cudaDeviceSynchronize();

    host_func(data);
    cudaFree(data);
}
```

Implementation Details

Under the hood

```
cudaMallocManaged(&ptr, ...);
```

```
*ptr = 1;
```

```
kernel<<<...>>>(ptr);
```

Implementation Details

Under the hood

```
cudaMallocManaged(&ptr, ...);
```
← Empty! No pages anywhere yet (like `malloc()`)

```
*ptr = 1;
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```
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Implementation Details

Under the hood

`cudaMallocManaged(&ptr, ...);` ← Empty! No pages anywhere yet (like `malloc()`)

`*ptr = 1;` ← CPU page fault: data allocates on CPU

```
kernel<<<...>>>(ptr);
```

Implementation Details

Under the hood

```
cudaMallocManaged(&ptr, ...);
```
← Empty! No pages anywhere yet (like `malloc()`)

```
*ptr = 1;
```
← CPU page fault: data allocates on CPU

```
kernel<<<...>>>(ptr);
```
← GPU page fault: data migrates to GPU

Implementation Details

Under the hood

```
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```
*ptr = 1;
```
← CPU page fault: data allocates on CPU

```
kernel<<<...>>>(ptr);
```
← GPU page fault: data migrates to GPU

- Pages populate on **first touch**
- Pages migrate on-demand
- GPU memory over-subscription possible
- Concurrent access from CPU and GPU to memory (page-level)

Performance Analysis

Comparing `scale_vector_um` (Unified Memory) and `scale_vector` (manual copy) for 20 480 `float` elements.

UM

```
Time(%)  Total Time (ns)  Name
-------  ---------------  ---------------------------------
  100.0          463,286  scale(float, float*, float*, int)
```

Manual

```
Time(%)  Total Time (ns)  Name
-------  ---------------  ---------------------------------
  100.0            4,792  scale(float, float*, float*, int)
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UM

```
Time(%)  Total Time (ns)  Name
-------  ---------------  ---------------------------------
  100.0          463,286  scale(float, float*, float*, int)
```

100× *slower?!*

What's going wrong here?

Manual

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Time(%)  Total Time (ns)  Name
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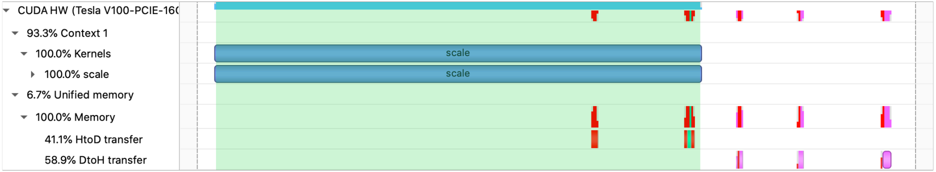

Manual

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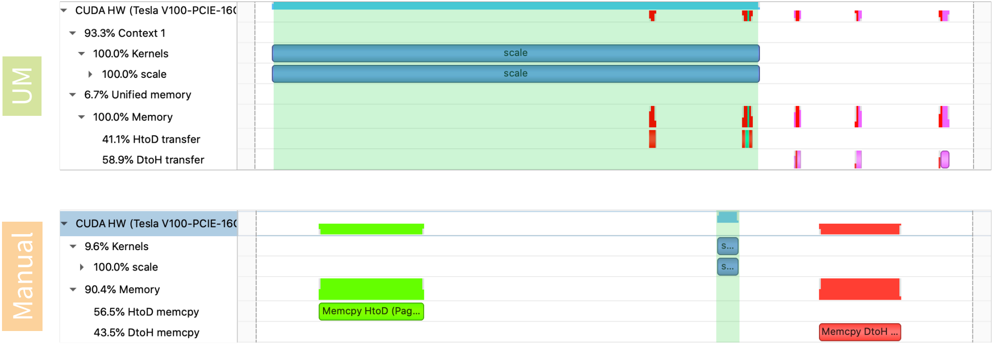

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Comparing UM and Explicit Transfers

UM: Kernel is launched, data is needed by kernel, data migrates host→device
$\Rightarrow$ Run time of kernel **incorporates** time for data transfers

Explicit: Data will be needed by kernel – data migrates host→device **before** kernel launch
$\Rightarrow$ Run time of **kernel** without any transfers

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- UM more convenient
- Total run time of whole program does not principally change
  Except: Fault handling costs $\mathcal{O}(10\,\mu\text{s})$*, stalls execution*
- But data transfers sometimes sorted to kernel launch

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- UM more convenient
- Total run time of whole program does not principally change
  Except: Fault handling costs $\mathcal{O}(10\,\mu s)$, stalls execution
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$\Rightarrow$ Improve UM behavior with performance hints!

Performance Hints for UM

New API routines

API calls to augment data location knowledge of runtime

- `cudaMemPrefetchAsync(data, length, device, stream)`
  Prefetches data to `device` (on `stream`) asynchronously

Performance Hints for UM

New API routines

API calls to augment data location knowledge of runtime

- `cudaMemPrefetchAsync(data, length, device, stream)`
  Prefetches data to `device` (on `stream`) asynchronously
- `cudaMemAdvise(data, length, advice, device)`
  Advise about usage of given data, `advice`:

Performance Hints for UM

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API calls to augment data location knowledge of runtime

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  - `cudaMemAdviseSetAccessedBy`: Data is accessed by *this* device; will pre-map data to avoid page fault
- Use `cudaCpuDeviceId` for `device` CPU, or use `cudaGetDevice()` as usual to retrieve current GPU device id (default: 0)

Hints in Code

```
void sortfile(FILE *fp, int N) {
    char *data;
    // ...
    cudaMallocManaged(&data, N);

    fread(data, 1, N, fp);


    cudaMemPrefetchAsync(data, N, device);
    kernel<<<...>>>(data, N);
    cudaDeviceSynchronize();

    host_func(data);
    cudaFree(data); }
```

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```

Prefetch data to avoid expensive GPU page faults

Hints in Code

```
void sortfile(FILE *fp, int N) {
    char *data;
    // ...
    cudaMallocManaged(&data, N);

    fread(data, 1, N, fp);

    cudaMemAdvise(data, N, cudaMemAdviseSetReadMostly, device);
    cudaMemPrefetchAsync(data, N, device);
    kernel<<<...>>>(data, N);
    cudaDeviceSynchronize();

    host_func(data);
    cudaFree(data); }
```

Read-only copy of data is created on GPU during prefetch
→ CPU and GPU reads will not fault

Prefetch data to avoid expensive GPU page faults

Tuning `scale_vector_um`

TASK

Express data movement

- Location of code: `01-Basics/exercises/tasks/06-Scale-Vector-Hints/`
- Look at `Instructions.ipynb` for instructions
  1. Task: Advise CUDA runtime that data should be migrated to GPU before kernel call
  2. Build with `make`
  3. Run with `make run`
  4. Glimpse at profile with `make profile`
- See also CUDA C programming guide (L.3.) for details on data performance tunig

Conclusions

- GPUs achieve performance by specialized hardware
- Acceleration can be done by different means
- Libraries are the easiest
- Thrust, OpenACC can give first entry point
- Full power with CUDA
- Threads, Blocks to expose parallelism for a kernel
- Several API routines exist
- Unified Memory productive, possibly with hints

Conclusions

- GPUs achieve performance by specialized hardware
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Thank you for your attention!

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Appendix

Glossary I

AMD Manufacturer of CPUs and GPUs. 3, 4, 5, 6, 7, 8, 9

Ampere GPU architecture from NVIDIA (announced 2019). 13, 14, 15

API A programmatic interface to software by well-defined functions. Short for application programming interface. 186

ATI Canada-based GPUs manufacturing company; bought by AMD in 2006. 3, 4, 5, 6, 7, 8, 9

CUDA Computing platform for GPUs from NVIDIA. Provides, among others, CUDA C/C++. 2, 3, 4, 5, 6, 7, 8, 9, 94, 103, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 135, 136, 137, 142, 143, 144, 145, 146, 154, 179, 180, 181, 185

JSC Jülich Supercomputing Centre, the supercomputing institute of Forschungszentrum Jülich, Germany. 185

Glossary II

JURECA A multi-purpose supercomputer at JSC. 15

JUWELS Jülich's new supercomputer, the successor of JUQUEEN. 12, 13, 14

NVIDIA US technology company creating GPUs. 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15, 58, 59, 60, 184, 185, 186, 187

NVLink NVIDIA's communication protocol connecting CPU $\leftrightarrow$ GPU and GPU $\leftrightarrow$ GPU with high bandwidth. 187

OpenACC Directive-based programming, primarily for many-core machines. 94, 96, 97, 98, 99, 100, 101, 180, 181

OpenCL The *Open Computing Language*. Framework for writing code for heterogeneous architectures (CPU, GPU, DSP, FPGA). The alternative to CUDA. 3, 4, 5, 6, 7, 8, 9, 94

Glossary III

OpenGL The *Open Graphics Library*, an API for rendering graphics across different hardware architectures. 3, 4, 5, 6, 7, 8, 9

OpenMP Directive-based programming, primarily for multi-threaded machines. 94, 96, 97, 98, 99

SAXPY Single-precision $A \times X + Y$. A simple code example of scaling a vector and adding an offset. 69, 108

Tesla The GPU product line for general purpose computing computing of NVIDIA. 12, 142, 143, 144, 145, 146

Thrust A parallel algorithms library for (among others) GPUs. See `https://thrust.github.io/`. 94, 103, 105, 180, 181

Glossary IV

V100 A large GPU with the Volta architecture from NVIDIA. It employs NVLink 2 as its interconnect and has fast *HBM2* memory. Additionally, it features *Tensorcores* for Deep Learning and Independent Thread Scheduling. 142, 143, 144, 145, 146

Volta GPU architecture from NVIDIA (announced 2017). 187

CPU Central Processing Unit. 12, 15, 20, 21, 22, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 69, 99, 105, 148, 149, 150, 158, 159, 160, 161, 162, 170, 171, 172, 173, 174, 175, 178, 184, 185

Glossary V

GPU Graphics Processing Unit. 2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 41, 42, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 64, 65, 66, 68, 72, 73, 74, 75, 76, 77, 88, 95, 96, 97, 98, 99, 102, 105, 107, 118, 119, 120, 135, 136, 137, 142, 143, 144, 145, 146, 148, 149, 150, 151, 152, 153, 158, 159, 160, 161, 162, 170, 171, 172, 173, 174, 175, 177, 178, 179, 180, 181, 184, 185, 186, 187

SIMD Single Instruction, Multiple Data. 51, 52, 53, 54, 55, 56, 57, 58, 59, 60

SIMT Single Instruction, Multiple Threads. 23, 24, 25, 38, 39, 41, 42, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60

SM Streaming Multiprocessor. 51, 52, 53, 54, 55, 56, 57, 58, 59, 60

SMT Simultaneous Multithreading. 51, 52, 53, 54, 55, 56, 57, 58, 59, 60

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