Tailoring potentials by simulation-aided design of gate layouts for spin-qubit applications

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Gate layouts of spin-qubit devices are commonly adapted from previous successful devices. As qubit numbers and device complexity increase, modeling new device layouts and optimizing for yield and performance become necessary. The simulation tools used in the advanced semiconductor industry need to be adapted for smaller structure sizes and electron numbers. Here, we present a general approach to electrostatically modeling new spin-qubit-device layouts, considering gate voltages, heterostructures, doping, reservoirs, and an applied source-drain bias. We identify key challenges in spin-qubit-device design: validating the impact on quantum-dot parameters, considering cross-coupling among gates and reservoirs, and ensuring robustness of the design to fabrication limits. We select a demanding target potential to investigate and optimize examples of gate layouts under these challenges. We verify our model by fabricating two simulated designs and indirectly probing the potential landscape through transport measurements.

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I. INTRODUCTION

Demonstrator devices for electron-spin qubits have been shown to work with high manipulation [1–9] and readout [9–12] fidelities and indicate a possible path to scaling to a quantum computer [13–21]. The gate layouts of most demonstrator devices are closely related to or copies of previous devices used by a research group or are copies of published layouts. Their functionality has been mostly tested as completed devices, and therefore only a few iterations have been made due to the relatively slow feedback cycle. Scaling up to larger qubit numbers requires optimized and new device layouts. As devices become more complex, testing of many device generations is not sufficient to achieve high yield and robustness to material variations. To this end, simulations are needed to predict functionalities and, finally, to strengthen the feedback cycle from device measurement to fabrication. Simulation tools are extensively used for high-complexity devices throughout the advanced semiconductor industry, for example technology computer-aided design (TCAD), which is used in the design of transistors, photodetectors, and miniature solar cells [22–24].

In contrast to these applications, spin-qubit devices require accuracy of single-electron control, include tunnel barriers, and are mostly based on smaller designs. Simulations of these devices require additional quantum mechanical constraints. Adaptions of TCAD software allowing quantum mechanical restrictions have been implemented, with a focus on optimizing qubit distances for manipulation and tunnel couplings [25]. There are simulation-based micromagnet designs optimized for fast and precise spin manipulation by use of electric dipolar spin resonance [8,26,27]. The coupling to electron reservoirs has been calculated by simulating the induced potential in a two-dimensional electron gas (2DEG) and approximating the Hamiltonian [28,29]. A detailed comparison with experimentally applied voltages has been presented only for gate pinchoffs [30]. These modeling efforts were based on ideal device layouts. However, the consideration of process constraints promises higher functionality and device yields. For that purpose, fabricational variations such as line-edge roughness on the order of a few nanometers [31] and the limitations of patterning with electron beam lithography at nonvertical angles need to be considered [32]. Here, we present a general approach to electrostatic modeling of a target potential, taking into account the gate structure,

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doping, reservoirs, and applied bias. We consider the influence of fabricational variability to optimize the design for stability and a small number of device iterations. For a particular target potential chosen as an example, implementations for both undoped and doped heterostructures, as well as depletion- and accumulation-mode designs, are designed. For two different heterostructure implementations, the simulated functionality is verified experimentally.

II. SIMULATION APPROACH

A. Design challenges

Our design approach is aimed at solving key challenges in spin-qubit-device design for arbitrary target potentials. Such potentials can be derived from targeting one or more quantum-dot (QD) parameters, e.g., tunnel couplings and capacitive couplings to gates and reservoirs, crosstalk of gates, or control of the chemical potential in QDs. After defining the potential, we first design a gate structure that yields the desired result. The simulation then allows the desired influence of the gate structure on the quantum-dot parameters to be validated and optimized if necessary. Therefore, we must be able to predict the shape and influence of multilayer gate patterns on the target potential, taking the properties of the underlying heterostructure into account. Finally, we need to investigate and optimize the robustness of the device to fabricational limitations that result in metal-gate roughness and potentially imperfect gate placement. This ensures the functionality of the device during the transition from the idealized design phase to the final fabricated sample.

B. Target potential

Our approach can be used to implement any target potential. To illustrate its possible application, we apply it to an example of a target potential.To exemplify the possible application, we discuss one specific potential to highlight the studied parameters. For this example, the aim is to form a QD that has similar tunnel couplings to the source and drain reservoirs, but a significantly larger capacitive coupling to the source than to the drain reservoir [Fig. 1(a)]. We implement this configuration by forming a QD potential with a sharp tunnel barrier to the source reservoir and the drain reservoir, with an added potential section between the seconddrain-side barrier and the drain reservoir. The potential in this added section, referred to as the slide, slowly decreases the potential to the chemical potential of the drain reservoir over a distance of several hundreds of nanometers [Fig. 1(b)]. We choose this specific example because it is particularly demanding in terms of the design challenges stated in Sec. II A. The ratio of the capacitive couplings to the source and drain represents a clearly defined quality value of the potential realization,

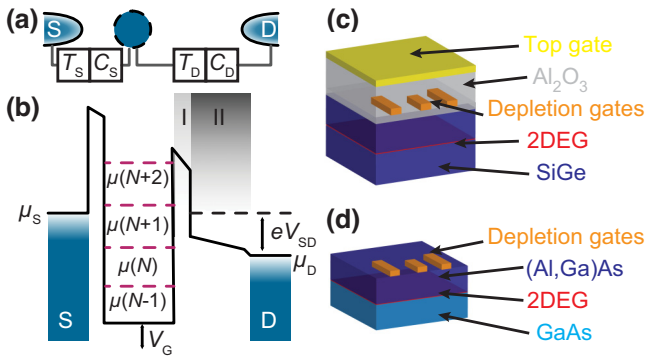

FIG. 1. Parameter settings. (a) Targeted coupling of a QD (blue) to source (S) and drain (D) reservoirs. The tunnel couplings are identical, i.e., $T_S = T_D$, and the capacitive coupling of the dot to the drain is significantly smaller than that to the source, i.e., $C_D \ll C_S$. (b) Schematic potential matching the requirements in (a). The tunnel coupling and the capacitive decoupling are defined by the potentials in sections I and II, respectively. (c),(d) Parameterization of simulation input for Si/SiGe and GaAs/(Al, Ga)As heterostructures, respectively.

which can be optimized via simulations. The piecewise defined potential profiles for the QD, barriers, and slide provide complex transition areas. These are no longer intuitive and require a detailed study of the cross-couplings. This is further complicated by the fact that the location of the reservoirs can change as a function of the bias V_{SD}. The long gates required to form the slide potential provide an interesting scenario in which to benchmark the effects of line-edge roughness and sample fabrication accuracy on the designed potential landscape.

This specific potential is studied as a QD charge sensor with enhanced performance [12]. A double quantum dot (DQD) is added next to it, which can host a spin qubit or qubits. The capacitive coupling between the QD of the sensor and the DQD must be high for good charge sensitivity.

III. GATE LAYOUTS

To highlight the versatility of our simulation approach regarding the heterostructure and charge accumulation, we choose three different realizations, including both a doped and an undoped heterostructure, as well as a depletion- and an accumulation-mode design. A depletion-mode design requires a filled 2DEG [1,3,33–40] and depletes the QD regions to the few-electron regime, and has been studied for both doped and undoped heterostructures. In the latter case, the lack of doping of the 2DEG is compensated by a global top gate, to which a positive voltage is applied in order to accumulate charge carriers in the 2DEG. Therefore, on the one hand the gate voltage applied to this global top gate determines the accumulation in the electron reservoir, but on the other hand it influences the

potential in the QD region. This lack of tuning flexibility is often problematic. The problem is solved by use of an accumulation-mode layout: this is a device with multiple patterned gate layers, in which positive and negative voltages for accumulation and depletion are chosen within the layers [2,41–45].

We build a finite-element model of a doped GaAs/(Al, Ga)As and an undoped Si/SiGe heterostructure, with simplified layer stacks in regard to the permittivities of the different materials [Figs. 1(c) and 1(d)], as the basis of the electrostatic simulations. For the GaAs/(Al, Ga)As devices, the depletion gate layer is added directly on top of the heterostructure as metal surfaces. The Si/SiGe devices include an oxide layer underneath the depletion gate layer and between the metal gate layers. For the multigate-layer accumulation design, oxide layers and metal gate layers are alternated. The quantum wells are implemented as a two-dimensional layer within which charges can be accumulated according to the Thomas-Fermi approximation (see Appendix A) [46,47]. We perform the electrostatic simulation using the finite-element solver COMSOL Multiphysics (the simulation parameters are given in Appendix B) and determine the tunnel barriers by use of the Wentzel-Kramers-Brillouin (WKB) approximation.

We realize the potential for three different boundary conditions: (I) a doped GaAs/(Al, Ga)As heterostructure, (II) an undoped Si/SiGe heterostructure with a global top gate, and (III) an undoped Si/SiGe heterostructure with an accumulation-mode design. Next to the sensor, a DQD is formed in the QW by properly shaped metal gates. The gate layouts are designed in an iterative process using a performance predictor to evaluate and improve the layout. For this, we choose the capacitive coupling C_D of the drain reservoir to the sensor QD. This coupling not only is critical to the functionality behind the target potential but also can be determined through measurements, which we use to validate our simulation results. C_D can be extracted from the simulations by varying the bias V_{SD} applied between the reservoirs and extracting the lever arm of one reservoir on the QD potential (see Appendix D). Differently from the notation in Ref. [48], we set the source reservoir to ground and apply a positive voltage to the drain reservoir. Simulations of other target potentials may require an adjusted predictor, with possibilities being the use of calculated and measured tunnel couplings or relative lever arms of different gates, among other things.

For the GaAs/(Al, Ga)As implementation [I, Fig. 2(a)], the target potential is formed by three additional gates added to the sensor design [marked in red in Fig. 2(a)],

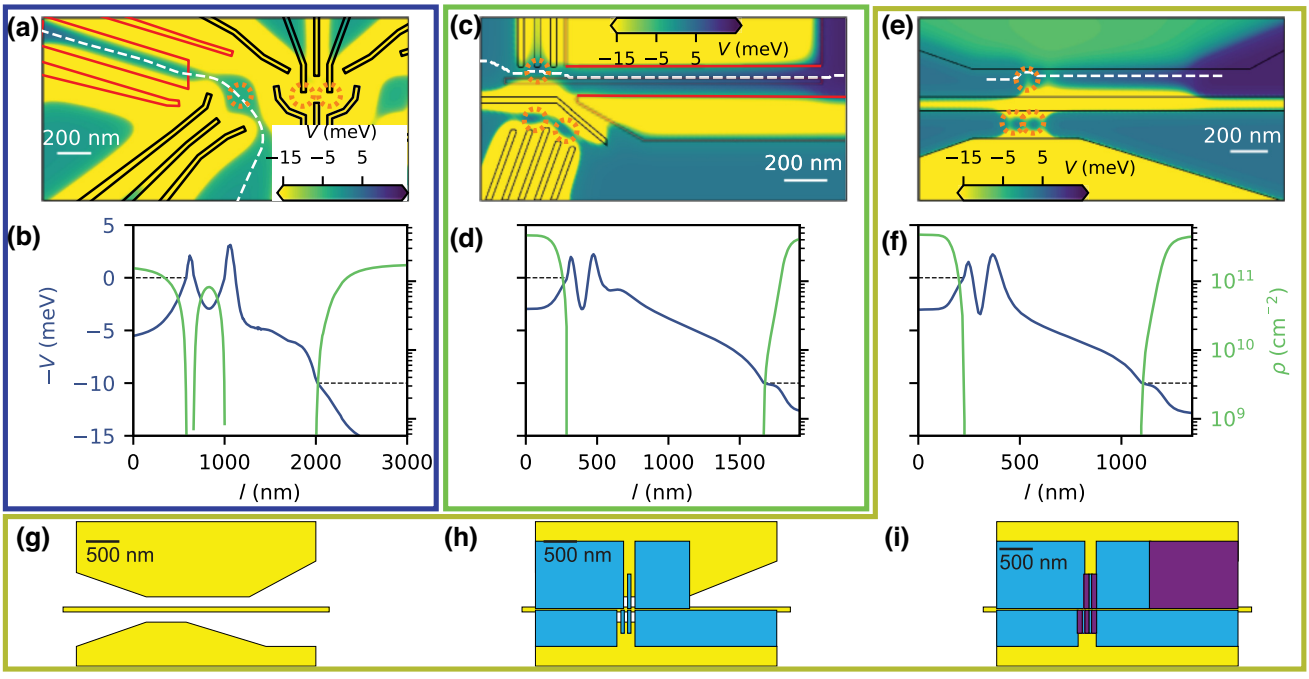

FIG. 2. Modeled electrostatic potential. (a) Potential realization for a doped GaAs/(Al, Ga)As heterostructure. The gate structure (black) and the pathline section used for visualization (white) are indicated, as well as the sensor QD and DQD regions (dashed orange lines). (b) Line section of potential V (blue) and charge-carrier density ρ (green) along the line section for the realization in (a). The source and drain levels are indicated (black dashed lines). (c) Potential realization for an undoped Si/SiGe heterostructure with a global top gate. (d) Line section of potential and charge-carrier density along the pathline section used for visualization for the realization in (c). (e) Potential realization for a closed-gate design in an undoped Si/SiGe heterostructure with the first gate layer (black). (g)–(i) Stacking of layers 1 (yellow), 2 (blue), and 3 (purple) in closed-gate design.

the angle and shape of which are adjusted in the simulation. In the slide region, the potential is reduced to remain below the electrochemical potential of the QD, so as not to reduce the tunnel coupling. As the motion of an electron from the source to the drain is not trivially accessible, Dijkstra's algorithm (see Appendix C) is used to determine line sections from the source to the drain, defined by minimizing a cost function combining the semiclassical Wentzel-Kramers-Brillouin approximation and a path of lowest potential. We evaluate the potentials along these line sections and use them for a more intuitive visualization [Fig. 2(b)]. The charge density shows that, due to the applied bias $V_{SD} = 10$ mV, the 2DEG in the slide region is depleted.

One Si/SiGe implementation [II, Fig. 2(c)] uses a gate on top of the slide and two side gates [marked red in Fig. 2(c)], similarly to the previous case. All three gates are set to positive voltages. The edges of the two side gates (highlighted in red) have a small angle α between them to ensure a widening potential. The line section of the potential through the sensor and the corresponding charge density show the target slide potential, where the slide is depleted of charge carriers according to the negligibly small charge density ρ [Fig. 2(d)].

The second Si/SiGe implementation uses an angle in the confinement gates and a separate accumulation gate in the slide region to define the potential [III, Figs. 2(e) and 2(f)], as shown in the gate structure separated into metal layers [Figs. 2(g)–2(i)]. These simulations allow us to optimize the gate layout without fabricating each design, while adhering to the fabricational limitations. For each realization, we are able to judge the feasibility of tuning the voltages applied to each layout to generate the target potential. Especially, regions with nontrivial cross-coupling from individual gates (mainly nonorthogonal gate structures) can be studied and optimized to fit a specific potential. Therefore, problems such as unrealistic fine tuning of specific gates being required can be avoided.

IV. BENCHMARK SIMULATIONS BY EXPERIMENTS

A. Capacitive coupling to sensor QD

After modeling these very different design layouts, it is indispensable to confirm our simulation methods. To verify our simulations, we fabricate and test the last design iteration. While the potential is the obvious parameter extracted from the simulations, direct probing of the shape of the potential over the entire device is hardly possible. Instead, we limit ourselves to benchmarking the behavior of the defined predictor, as indirect probing. On the experimental side, measuring a QD formed in the target potential in transport (see Fig. 1) leads to strongly tilted Coulomb diamonds [12], from which C_D can be measured. A large and continuously declining slide region decouples the drain reservoir. This decoupling leads to a large slope m of the resonance point between the dot and the drain, while the slope of the dot-source resonance point (m_+) remains nearly constant.

We correlate the slope m with the capacitive coupling C_D between the drain reservoir and the QD, via the asymmetry η of the coupling to the source and drain reservoirs:

$$\eta = \left| \frac{dV_{SD}/dV_{PS}|_{\mu_{QD}=\mu_D}}{dV_{SD}/dV_{PS}|_{\mu_{QD}=\mu_S}} \right| = \left| \frac{m}{m_+} \right| = \frac{C_{PS}}{C_D} \frac{C_\Sigma - C_D}{C_{PS}} = \frac{C_\Sigma}{C_D} - 1, \quad (1)$$

where V_{PS} is the voltage applied to the QD plunger PS, and C_{PS} and C_Σ are the capacitive coupling of the gate PS and the total capacitive coupling of all gates, respectively. To probe the potential, we vary the applied gate voltages in the slide region and extract the slopes of the Coulomb diamonds measured for various voltage configurations. For the casetype II implementation, Si/SiGe with a global accumulation gate, we measure this experimental dependence.

A device similar to the one tested is depicted in Fig. 3(a). The voltage of the marked gate SR is adapted to change the potential of the sensor region and control the coupling to the drain reservoir, while the gate PS and the bias applied between the Ohmic contacts V_{SD} are used to measure the diamonds. For larger values of V_{SR}, the standard Coulomb diamonds [Fig. 3(b)] are measured, and the dot-drain-resonance slope m of the diamonds is extracted. The tilt of the diamonds is enhanced when the voltage applied to the gate SR is decreased. A steep slope m is observed for a very low voltage V_{SR} [Fig. 3(c)]. Comparing m for different slide configurations reveals a systematic decrease in m as a function of a decreasing voltage applied to SR [Fig. 3(d)]. This corresponds to the formation of a slide region after the drain-side barrier, which is elongated as lower SR values narrow the path to the drain contact. The data match the trend predicted by the simulation but exhibit a variance in the required voltage range. This deviation aligns with the typical order of magnitude observed in Si/SiGe structures across different samples, measurement protocols, or cooldowns. This is consistent with the fact that the device layout is optimized for $\eta = 200$ by the simulation. Note that larger asymmetries parameterized by η are possible according to the simulation, but are of limited use as the corresponding tuning of the plunger voltage applied to the gate PS needs to be as accurate as $\Delta V_{PS} = 0.5$ mV to use the QD as a sensor. The maximum value obtained experimentally during a separate measurement on a second sample is $\eta = 85$. The discrepancy between the simulation and experiments can be attributed to imperfect gate structures or to defects, as both require an adjustment of

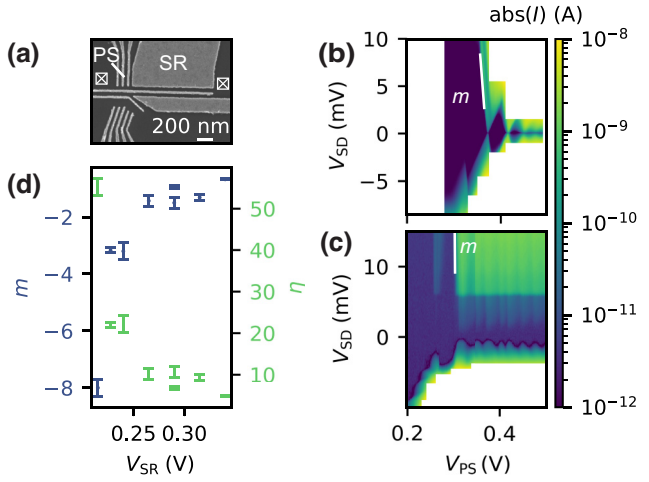

FIG. 3. Experimental variation of the slide region. (a) Scanning electron micrograph (SEM) of an identical device with slide gate (SR), plunger (PS), and sensor-dot Ohmic contacts (crosses) marked. (b),(c) Coulomb diamonds with slope m shown for $V_{SR} = 0.35$ V and $V_{SR} = 0.24$ V, respectively. (d) Coulomb-diamond slope (blue) and η (green) as a function of slide-gate voltage.

the applied voltages, which shortens the length of the slide region.

Via this indirect probe, we can measure a few aspects of the potential, such as verifying the tunnel barriers and the formation of a tunable slide region. Even without a general or global potential probe, we can verify the assumptions of our simulations.

B. Influence of reservoir bias

Not only a description of the influence of the gate layer, but also a good description of the impact of the electron reservoirs and the applied bias V_{SD} between the source and the drain reservoir of the sensor are essential for accurately modeling the potential landscape. The extent of the reservoirs determines the reach of the screening effects of accumulated electrons. A change in V_{SD} has a large influence on the overall potential landscape and changes the size of the reservoirs. For complex gate layouts and complex electrostatic landscapes of the bias V_{SD}, the extent of the reservoirs is nontrivial and can be predicted only by simulations.

To study the influence of the bias V_{SD}, we use as an example a device similar to the type I implementation [Fig. 2(a)], a doped GaAs/(Al, Ga)As device, which is optimized for larger bias values. A device identical to the one measured and simulated is depicted in Fig. 4(a). For this layout, simulations with varying bias voltages V_{SD} are performed without changing the gate voltages in between [Fig. 4(b)]. The bias V_{SD} is applied asymmetrically, meaning that only one reservoir potential is shifted. We extract the coupling asymmetry η from simulations for various bias points. The simulation results indicate a pronounced rise in η as the bias voltage increases. This trend can be intuitively explained by considering the length of the slide region, which expands with the applied V_{SD}. The boundaries of the reservoir can be identified from the charge-carrier density.

We experimentally verify this simulation of the impact of the bias by comparing it with the measured Coulomb diamonds of the device. As discussed for Fig. 3, the extracted capacitive coupling C_D is used as a probe of the shape of the potential. For large bias voltages V_{SD}, the Coulomb diamonds tilt even for a QD, which has no added slide potential [see Fig. 4(c)]. This indicates suppression of C_D. We call this type of single-electron transistor (SET), which does not employ a slide potential, a symmetrically coupled QD. Here, the asymmetry arises due to a large bias V_{SD} applied only to one of the two reservoirs. We repeat the simulations shown in Fig. 4(b) for the symmetrically coupled case. Here, we notice a comparable trend of increasing coupling asymmetry η with higher bias voltages. However, it is important to note that this increase is notably smaller than in the case of an asymmetrically coupled QD. As this device is based on a doped heterostructure, measuring the device with no voltage applied to the gate DB5 allows it to be used as a symmetrically coupled QD. We extract the slope m of the Coulomb diamonds as a function of the bias V_{SD}. The absolute value of the slope increases with the applied bias V_{SD}.

An asymmetrically coupled QD can be formed when the slide region is depleted by the voltage applied to the gate DB5, forming a potential as intended in the simulations [see Fig. 1(b)]. Then, steeper diamond slopes are observed [Fig. 4(d)]. With an added slide region in the potential, the increase of the absolute value of the slope m with increasing bias V_{SD} is significantly larger, as expected from the simulations, where the slide length and therefore the capacitive coupling of the drain reservoir to the QD depend strongly on the value of V_{SD} applied [inset of Fig. 4(d)]. The experimentally observed larger tilt of the Coulomb diamonds [Fig. 4(c) versus 4(d)] is correctly predicted by our simulation.

C. Fabricational variability

A significant benefit of simulating different layouts is the possibility of finding a robust design with regard to fabricational influences and imperfections. Therefore, we analyze the stability of the simulated gate layouts with regard to the spatial resolution limit of the nanolithography of the metal gates. As an example of the geometry of a type II device [see Fig. 2(c)], we first study the impact of the line-edge roughness of a patterned gate structure. The edges of the metallic gates of an example device are identified by applying shape recognition to a scanning electron micrograph [Fig. 5(a)]. The observed realistic line-edge roughness is

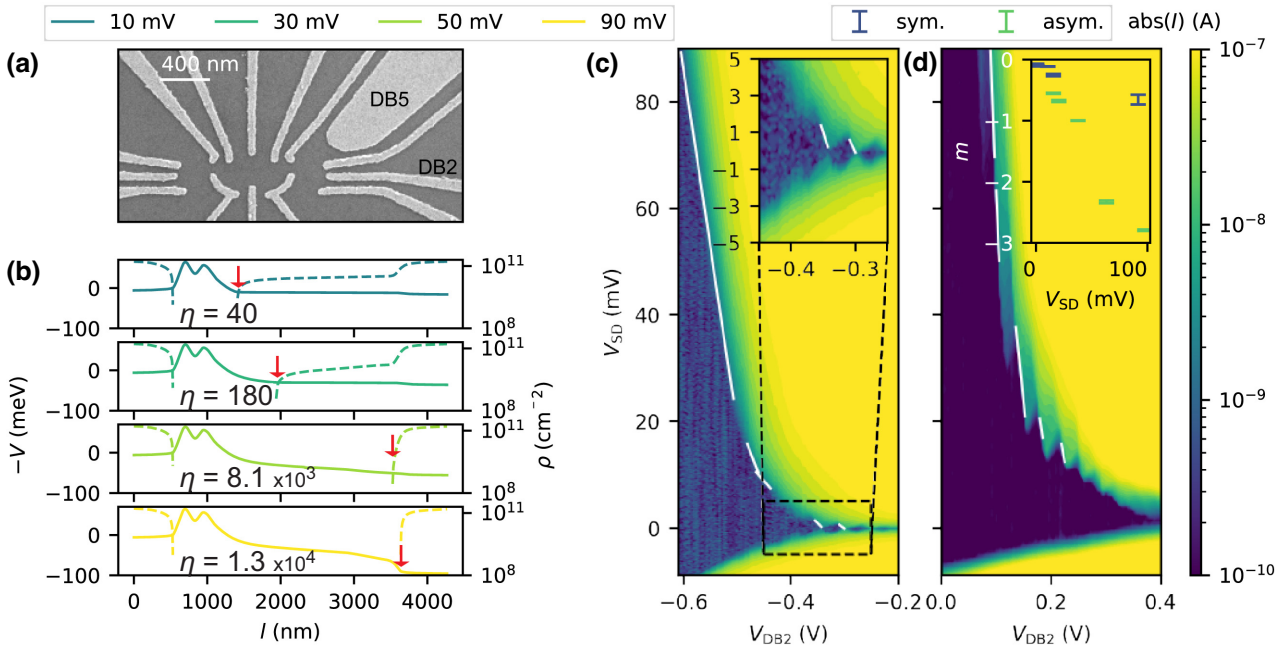

FIG. 4. Influence of bias. (a) SEM of an identical device with slide gate (DB5) and sensor plunger (DB2) marked. (b) Simulation of influence of bias on the potential formed. When only the bias voltage is increased, the slide length of the induced potential V (solid lines) increases. Accordingly, the charge density ρ (dashed lines) extends into the slide region, depending on the applied bias. The beginning of the drain reservoir is marked with red arrows. (c) Coulomb diamonds of a symmetrically coupled QD operation with an asymmetrically applied bias voltage. The slopes (white lines) of the Coulomb diamonds are extracted from the dependence on the applied bias. A current level of 1.5 nA is used as a threshold. For clarity, the low-bias regime is depicted as an inset. To realize the symmetric coupling of the reservoirs to the QD operation, the slide-forming gate voltage V_{DB5} is set to zero. (d) Coulomb diamonds of an asymmetrically coupled QD operation with $V_{\mathrm{DB5}} = -0.31$ V. For the same current threshold $I = 1.5$ nA, the slopes m (white lines) are extracted. The extracted m for both operation modes is depicted in the inset as a function of the applied bias.

fed back to our finite-element device model to predict its impact on the shape of the target potential. The calculated potential along the pathline section used for visualization predicts a slide potential with multiple ripples after the voltages applied are finely tuned when a realistic line-edge roughness is used, in contrast to case for perfect gate edges [Fig. 5(b)]. Although the general potential is obtained, we note that a slide region shorter than that for the ideal gate layout is likely to occur, as the voltages are tuned to form only one QD with two sharp barriers. We obtain $\eta = 165$, compared with $\eta = 200$ for the ideal layout.

Note that, in general, it is even not required to fabricate an example device. A simple variation of the shape of the metal gates in the simulation is sufficient to study the robustness to fabrication imperfections. In addition to line-edge roughness [49], limitations on accurate alignment in nanolithography [50] can be explored by simulation. Nonorthogonal and, especially, small-angle gate structures are not fabricated accurately when one relies on electron beam lithography [32,51]. To quantify the impact on the generated potential, we implement small changes in angles of the gates in our finite-element model. As an example of this angle variation, the position of the corner of the gate labeled SR is varied along the y axis. This results in variations of the opening angle of the gap between the gates in the slide region [the bright blue dot in Fig. 5(a)]. For a displacement of a few nanometers, our potential simulation predicts that the potential slide can be reduced to half of its original length or that a flat potential region might occur [yellow and blue lines, respectively, in Fig. 5(c)]. In the first case, a significantly lower asymmetry η would be obtained experimentally, causing a decrease in sensor gain [12]. In the second case, the sensor current might be blocked, since the disorder in the potential [see Fig. 5(b)] changes the flat potential region into a series of disordered QDs and may possibly block the current through the sensor region.

Tuning the voltages applied to specific gates can partially improve the shape of the potential. Also, this tunability can be predicted by our device model: For the case of a −10-nm displacement, the tunability of the slide with respect to the voltage V_{SR} is shown in the inset of Fig. 5(c). Tuning the voltage predominantly alters the height of the potential within the slide region and therefore has a small influence on the linear slope of the slide. Our discussions show that gate layouts, which are unreliable with respect to fabrication imperfections, can be studied, and the impact of these imperfections can be eliminated by simulation.

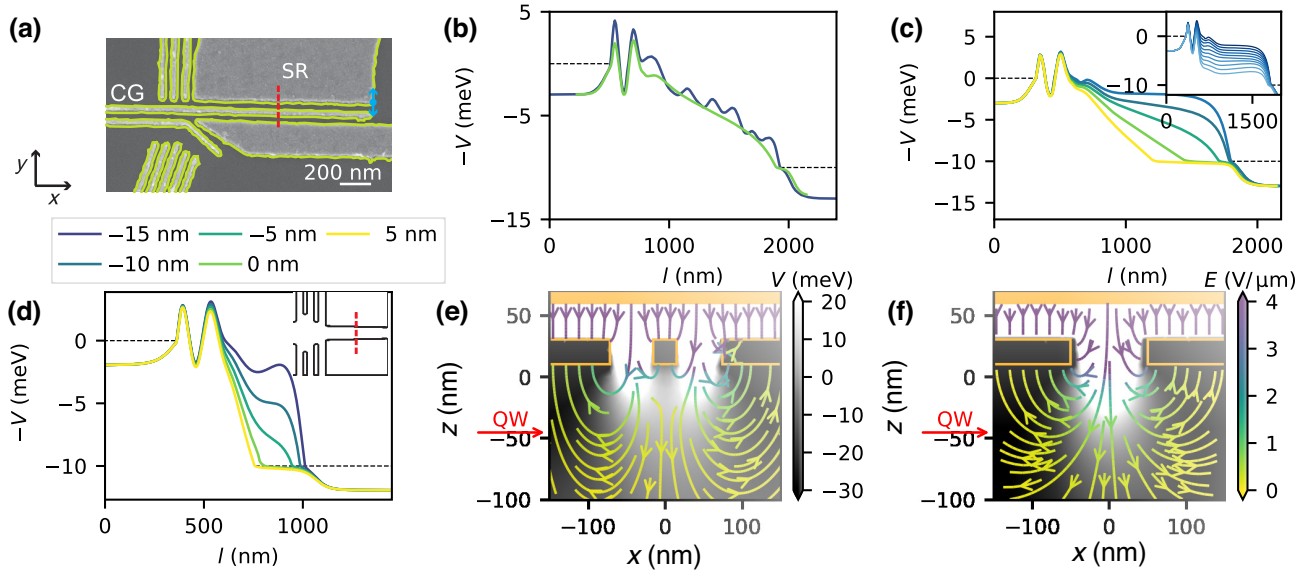

FIG. 5. Robustness of potential. (a) SEM of an identical device. The edges of the fabricated gates (yellow) are extracted by image processing. (b) Potential along line section using the gate edges in (a) of a fabricated device (blue) and optimal gate edges (green). (c) Influence of slide angle on line-section potential. The slide angle is varied by changing the y position of the endpoint of the slide [blue dot in (a)]. The inset shows compensation by tuning of the slide voltage for $\Delta y = -10$ nm. Starting from the top, $\Delta V_{\mathrm{SR},i} = (i-1) \times 10$ mV. (d) Influence of slide angle for a simpler device (layout in inset). (e) Cross section of slide potential and electrical field perpendicular to the path at the position marked in red in (a). The gate edges are marked in orange, and the quantum well (red arrow) is placed at $z = -45$ nm. (f) Cross section of slide potential and electrical field perpendicular to the path in the simple device at the position marked in red in the inset of (d).

We conclude with a final example of simulation-supported gate design, which motivated our choice to use a thin metal gate in the type II device [labeled CG in Fig. 5(a)]. For this purpose, we compare this with a summarized and simplified Si/SiGe device layout [inset of Fig. 5(d)] for a sensor without a capacitively coupled DQD. Similarly to the type II device, we include a global accumulation gate in our device model. The simplification to a symmetric single dot without a DQD nearby allows us to reduce the input parameters. Electrostatic simulation of the variation of the angle of the slide-forming gates [see Fig. 5(c)] reveals a larger influence on the shape of the slide potential [Fig. 5(d)]: a second unintentional potential minimum emerges in the pathline section used for visualization.

The larger influence of variations in the simple device than in the type II device [Fig. 2(c)] can be understood from our simulations as well, by extracting and studying the electric field gradients at the quantum well [Figs. 5(e) and 5(f)]. For the type II device, the simulated potential forms a single minimum at the height of the quantum well [grayscale in Fig. 5(e), where a small center gate is included]. However, the electric field is mainly defined by the gates patterned on the depletion-gate layer, while the influence of the accumulation gate is blocked by the central gate along the current path [color-scaled arrows in Fig. 5(e)]. For the simple device without a central thin gate, the influence of the global accumulation gate dominates [Fig. 5(f)]. Both the electric field (color-scaled arrows) and the potential (grayscale) depend strongly on the global accumulation gate. For both devices, the gates in the depletion-gate layer are tuned to have similar voltages so as to be less sensitive to variations. Thus, we conclude that the thin long gate in the type II device layout better screens the effect of the top gate, which has a larger potential difference compared with the difference between the slide gates within the depletion layer. For any design that is aimed at, consideration of the generated electric fields is useful, as they indicate layout positions that are most impacted by small variations. As it is not possible to fully avoid fabricational fluctuations, reducing the generated electric fields improves the robustness and leads to a higher yield.

V. CONCLUSIONS AND OUTLOOK

We describe a general approach to electrostatic modeling of spin-qubit devices. Our model includes descriptions of the heterostructure, gate layers, reservoirs, and applied bias and can be applied to accumulation- or depletion-type heterostructures. We show gate design by device simulation for an example of a target-potential shape, which necessitates the development of a complex gate structure and an in-depth investigation of cross-couplings among

gates and reservoirs. Additionally, the desired potential shape in our study requires precise control over large distances, making the potential highly sensitive to fabrication limitations such as line-edge roughness and the accuracy of gate placement. We experimentally benchmark our simulation by probing the predicted gate-voltage dependences of the current through the device. By simulating our device layout, we are able to predict the properties of and successfully operate first-generation devices [12]. We include a study to make the gate layout robust to unavoidable fabrication imperfections. With our general finite-element modeling of qubit devices, the electrostatic potential landscape can be predicted and the gate layout optimized without the need for resource-costly fabrication iterations.

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APPENDIX A: THOMAS-FERMI APPROXIMATION

The 2DEG is implemented in the simulation as a two-dimensional plane, throughout which the charge density ρ is determined using the Thomas-Fermi approximation (TFA),

$$n_{\mathrm{el}}(\mathbf{x}) = \int D(E) f\left([[E + eV(\mathbf{x})] - \mu]/k_{\mathrm{B}}T\right) dE. \quad \text{(A1)}$$

In the case of SiGe, the valley degeneracy leads to a partially defined electron density

$$n_{\mathrm{el}}(\mathbf{x}) = \begin{cases} \dfrac{2m^*}{\pi\hbar^2}, & E_{\mathrm{F}} + E_{\mathrm{VS}} < eV(\mathbf{x}), \\ \dfrac{m^*}{\pi\hbar^2}, & E_{\mathrm{F}} < eV(\mathbf{x}) < E_{\mathrm{F}} + E_{\mathrm{VS}}, \\ 0 & eV(\mathbf{x}) < E_{\mathrm{F}}, \end{cases} \quad \text{(A2)}$$

where E_{F} corresponds to the Fermi energy, E_{VS} to the valley-splitting energy, and $V(\mathbf{x})$ to the potential. Since $\rho(V) = en_{\mathrm{el}}(V)$ and $V = V(\rho)$, ρ and V have to be solved for self-consistently. To include the applied bias, V_{SD} is added to $V(\mathbf{x})$ where applicable. The boundaries of the regions are determined by the maxima of the tunnel barriers, where the charge density ρ is equal to zero.

As the TFA is most accurate for large electron numbers, the QD regions need to be considered carefully. For the SiGe simulations, the charge density is set to zero in the QD regions delimited by the tunnel barriers. For the GaAs simulations, the charge density is measured by use of the TFA in the QD region also.

APPENDIX B: SIMULATION PARAMETERS

The parameters used to model the Si/SiGe and (Al, Ga)As/GaAs implementations are listed in Table I. Both the (Al, Ga)As/GaAs and the Si/SiGe implementation use a fine mesh in the 2DEG region and, specifically, the QD regions, as well as a limited maximum element size to accurately describe the effect of the small gates.

APPENDIX C: DIJKSTRA'S ALGORITHM FOR DETERMINATION OF LINE SECTIONS

As the simulated potential channel has no inherent symmetry, *Dijkstra's algorithm* is used to calculate a well-defined path for a line section through the two-dimensional

TABLE I. COMSOL simulation parameters.

Description	Variable	Si/SiGe	(Al, Ga)As/GaAs
Effective electron mass	m^*	$0.19m_e^*$	$0.067m_e^*$
Valley splitting	E_{VS}	70 μeV	
Fermi energy	E_{F}	555 meV	6.5 meV
Permittivity of heterostructure	ϵ_r	13	13
Permittivity of oxide	$\epsilon_{\mathrm{oxide}}$	11.3	
Gate height	h_{gate}	20 nm	30 nm
Oxide height	h_{oxide}	10 nm	
Minimum element size (ES)	d_{min}	5 nm	1 nm
Maximum ES	d_{max}	75 nm	150 nm
Minimum 2DEG ES	$d_{\mathrm{min,2DEG}}$	1 nm	1 nm
Maximum 2DEG ES	$d_{\mathrm{max,2DEG}}$	15 nm	15 nm
Depth of 2DEG	z_{2DEG}	45 nm	90 nm

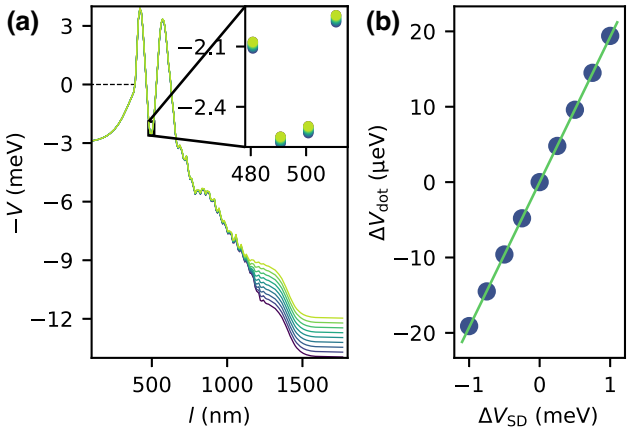

FIG. 6. Determination of the gate lever arm α_D by simulation. (a) Potential along line sections for various bias voltages V_{SD}. (b) Change in potential minimum ΔV_{dot}, obtained from an interpolation in the QD region of the 2D data for the line sections of the potential in (a), as a function of the change in bias voltage ΔV_{SD}. The data points are linearly fitted to obtain the slope α_D (green).

(2D) potential landscape. This algorithm calculates the cheapest path between two nodes in a graph, where the nodes are defined as the mesh points used in the simulation. The cost function C between nodes is defined as

$$C = \mathrm{Re}\left(\sqrt{E_F - eV(\mathbf{x})}\right) - \epsilon eV(\mathbf{x}), \tag{C1}$$

where the first part ($\sqrt{E_F - eV(\mathbf{x})}$) is based on a semiclassical (WKB) approximation, and the second part ($eV(\mathbf{x})$) is based on a classical path of lowest potential. The WKB approximation is thereby used to determine the path through the barriers. Only the real part of the square root is therefore of interest, and constants are neglected. The dynamically calculated prefactor ϵ is chosen to be small, so that the cost function is completely dominated by the WKB contribution and the potential has an influence only outside the barrier zones.

The calculated path supports visualization of the relevant potential region. While the well-defined cost function allows a comparison between different devices, it does not represent the quantum mechanical behavior of an electron.

APPENDIX D: EXTRACTION OF CAPACITANCE FROM SIMULATION

The coupling asymmetry η depends on the capacitance ratio $C_\Sigma C_D^{-1}$. The potential of the dot depends linearly on the voltage applied to the drain reservoir V_{SD}, with a factor $\alpha_D = -C_D C_\Sigma^{-1}$. This is extracted from the simulations by varying V_{SD} and monitoring the potential minimum V_0. η is then given by

$$\eta = |\frac{C_\Sigma}{C_D} - 1| = \frac{1}{\alpha_D} + 1. \tag{D1}$$

This is realized by running the simulation for a specific design nine times with a varying $V_{SD} = -10$ mV + [−1 mV, −0.75 mV, −0.5 mV, −0.25 mV, 0 mV, +0.25 mV, +0.5 mV, +0.75 mV, +1 mV]. The potential minimum is determined for each simulation by placing an ellipse around the dot and evaluating the potential at each mesh point inside it. As the potential is evaluated only at the points of the discrete mesh, the element density is set accordingly, to ensure a high enough resolution to cover possible shifts in the spatial position of the potential minimum. The potential minima so obtained are then plotted against V_{SD} and fitted to obtain α_D, as shown in Fig. 6.

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