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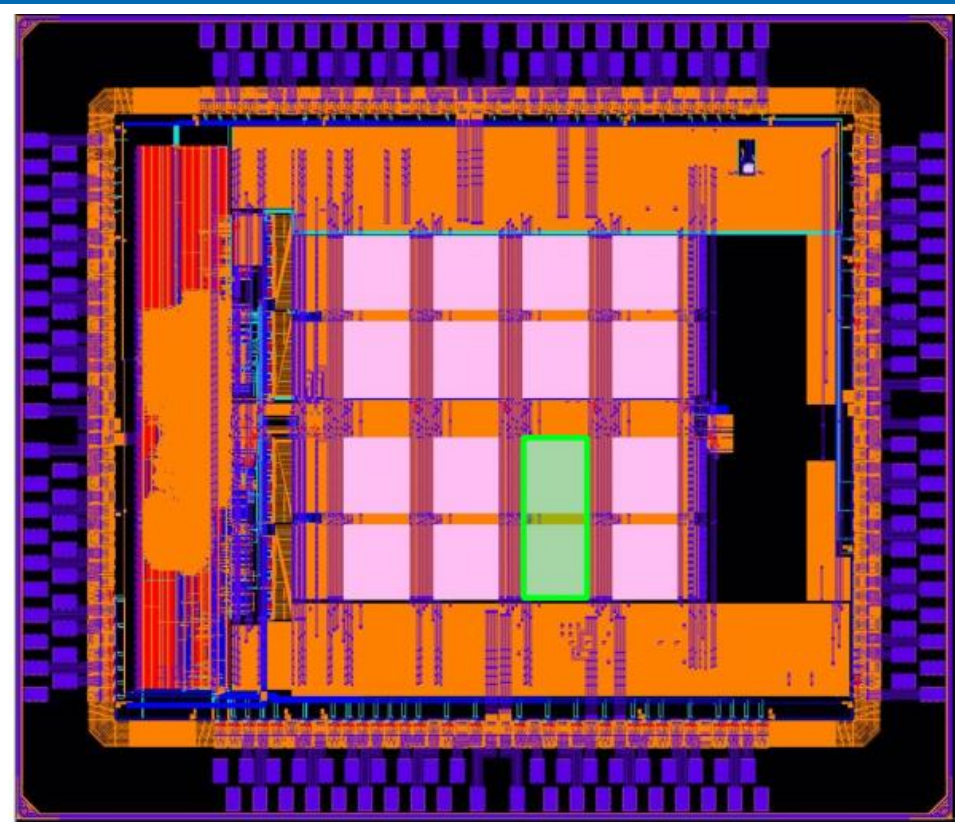
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Physics-based Modeling and Experimental Characterization of Endurance in Filamentary VCM ReRAM [1]

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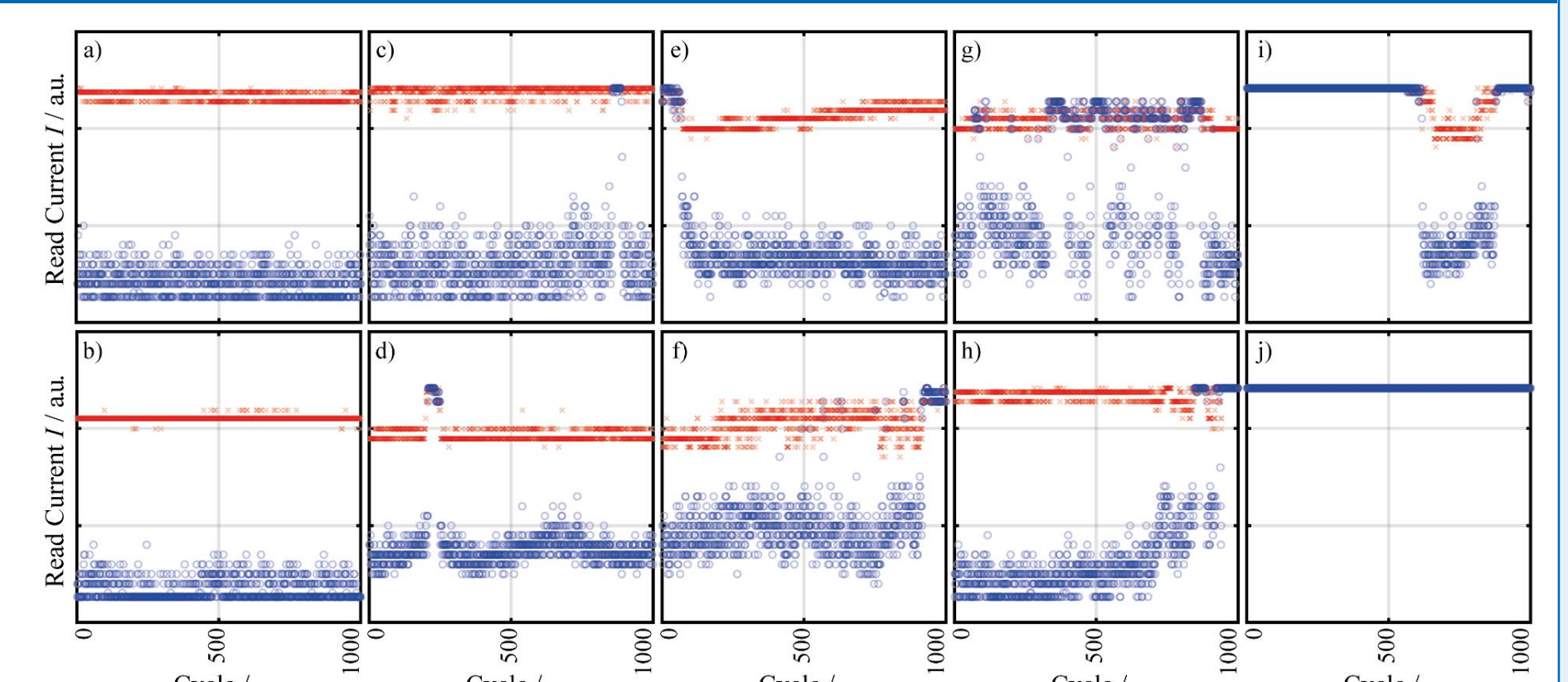
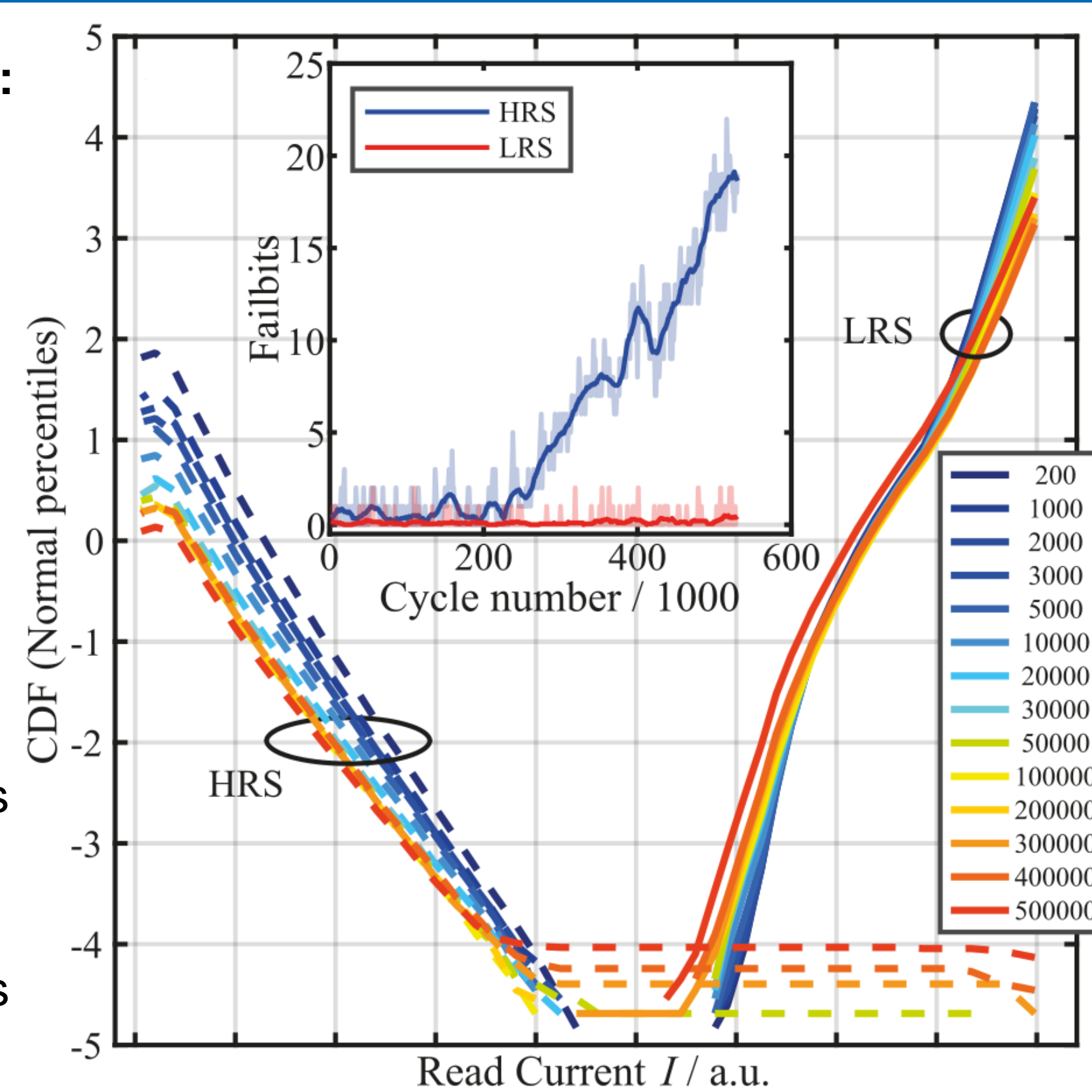
Motivation

**Industrially fabricated test-chip:**

- 16 Mbit VCM-type ReRAM
- BEOL integrated
- 1T1T configuration
- 28nm CMOS technology
- 2 Mbit (green block) cycled

Experimental Endurance characterization:

- Switching via program-verify algorithm [2]
- 500k switching cycles performed for 2 Mbit
- Great endurance – cumulative HRS and LRS distributions are very stable
- Few ppm fail-bits in HRS at high cycle numbers (>250k)
- Single bits fail to RESET – total number of fail-bits increases linearly

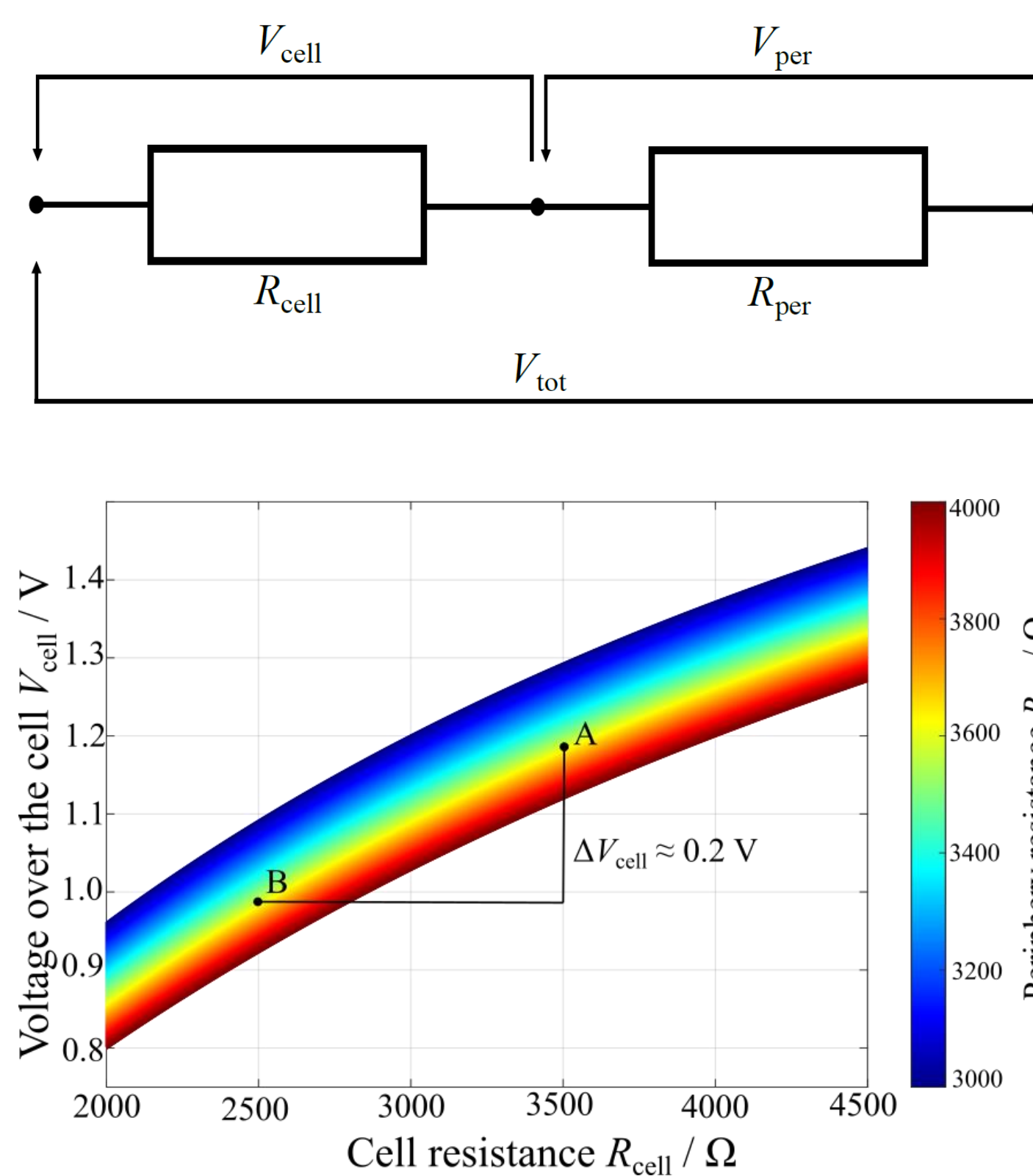
**Selected traces of single bits:**

- HRS (blue), LRS (red) over 1000 switching cycles
- a)/b): Reference bits with no observed failure
- c)-j): Bits with single fail events (c)) increasing to permanent failure during the 1000 cycles in j)
- Fail-bits can occur spontaneously or gradually
- Fail-bits are not permanent and can be recovered
- Fail-bits typically show high LRS current

Phenomenological Model

Simple explanation for the origin of the RESET failure:

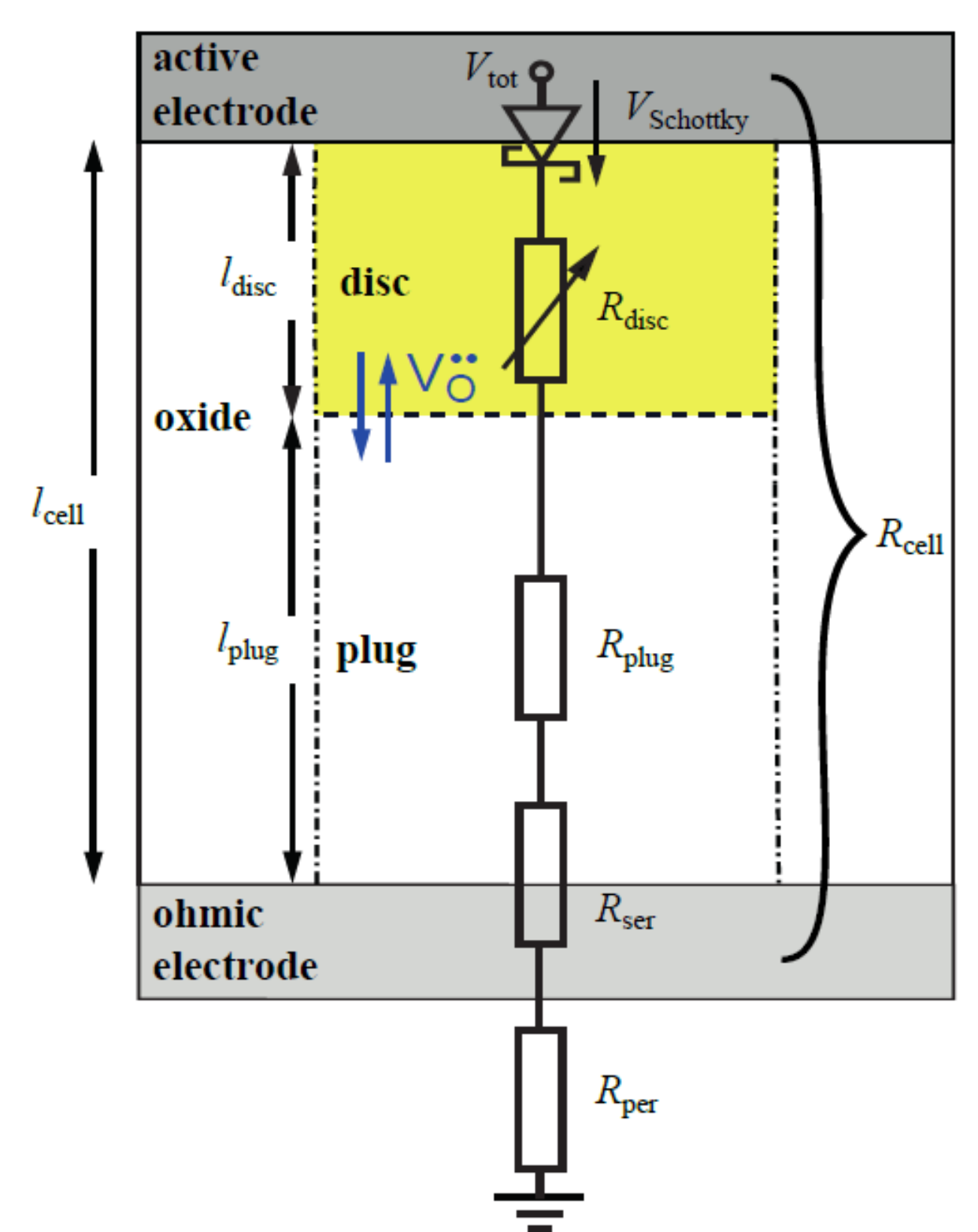
- Transistor, line resistances, etc. summed up to periphery resistance
- Voltage divider
- $V_{cell} = V_{tot} \frac{R_{cell}}{R_{cell} + R_{per}}$
- External voltage constant
- Periphery resistance can vary from device to device
- Cell resistance varies from device to device and from cycle to cycle
- “Unlucky” combination of high periphery resistance and low cell resistance leads to too low voltage dropping over the cell
- RESET time strongly dependent on the cell voltage [3]



1D KMC Simulation Model

Simulation of huge statistics: Adaption of KMC methods to compact model:

- Based on JART VCM 1.0 model [4]
- Kirchhoff's law: $V_{tot} = V_{Schottky} + I \times \sum_i R_i$
- $R_{disc,plug} = \frac{l_{disc,plug}}{A \times Z V_0 \times e N_{disc,plug} \mu_{no}} \exp\left(\frac{\Delta E_{ac}}{k_B T}\right)$
- $T = (V_{disc} + V_{plug}) \times I \times R_{th,eff} + T_0$
- Ion movement calculated via Mott-Gurney law and KMC methods [5]:
- V_0 jump from plug to disc or vice versa: $R^{f,r} = v_0 \times \exp\left(-\frac{\Delta W_{f,r}}{k_B T}\right)$
- Weighted, random process selection
- Time update: $t_{jump} = \frac{\ln(rand)}{R^{f,r}}$



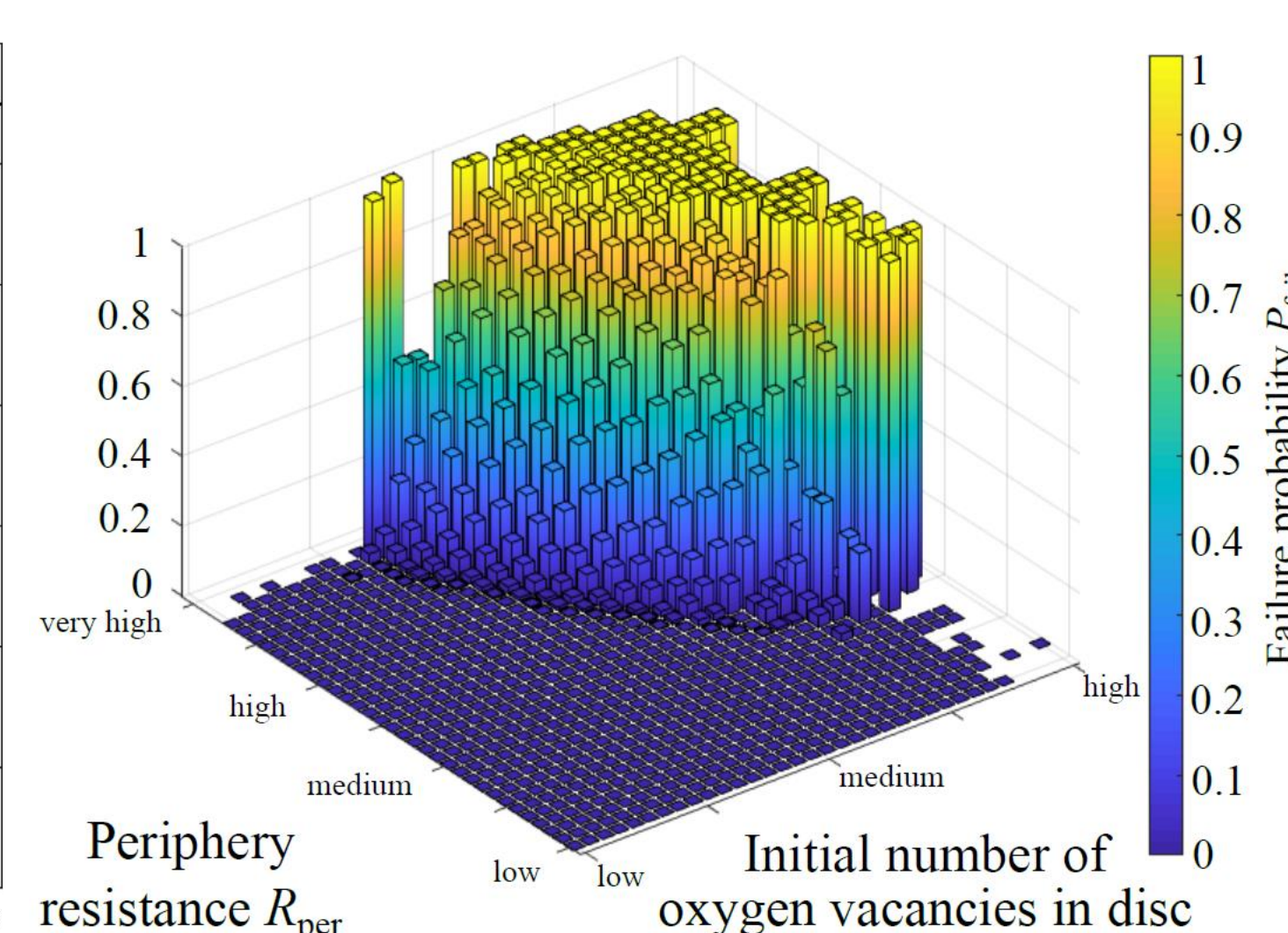
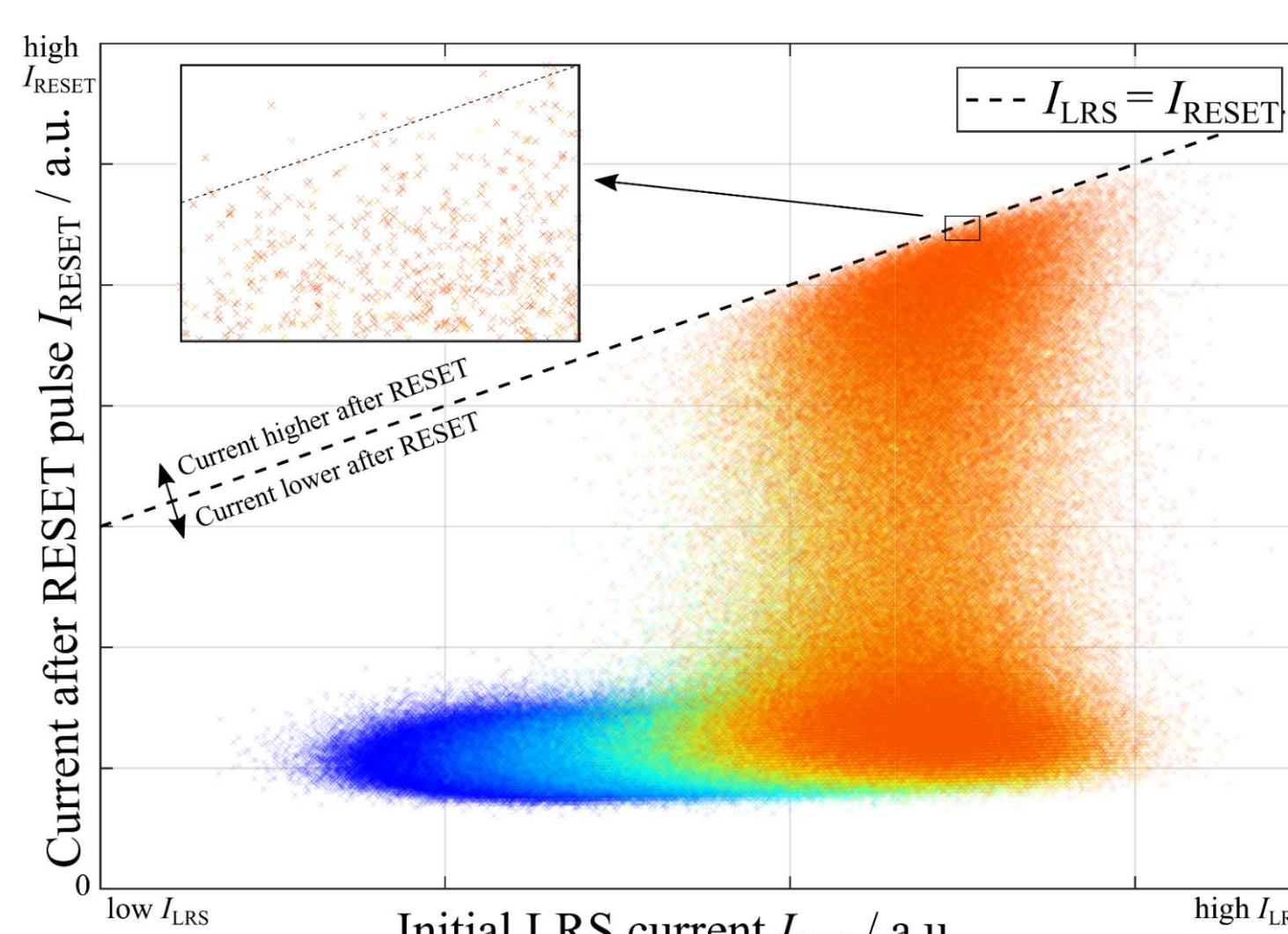
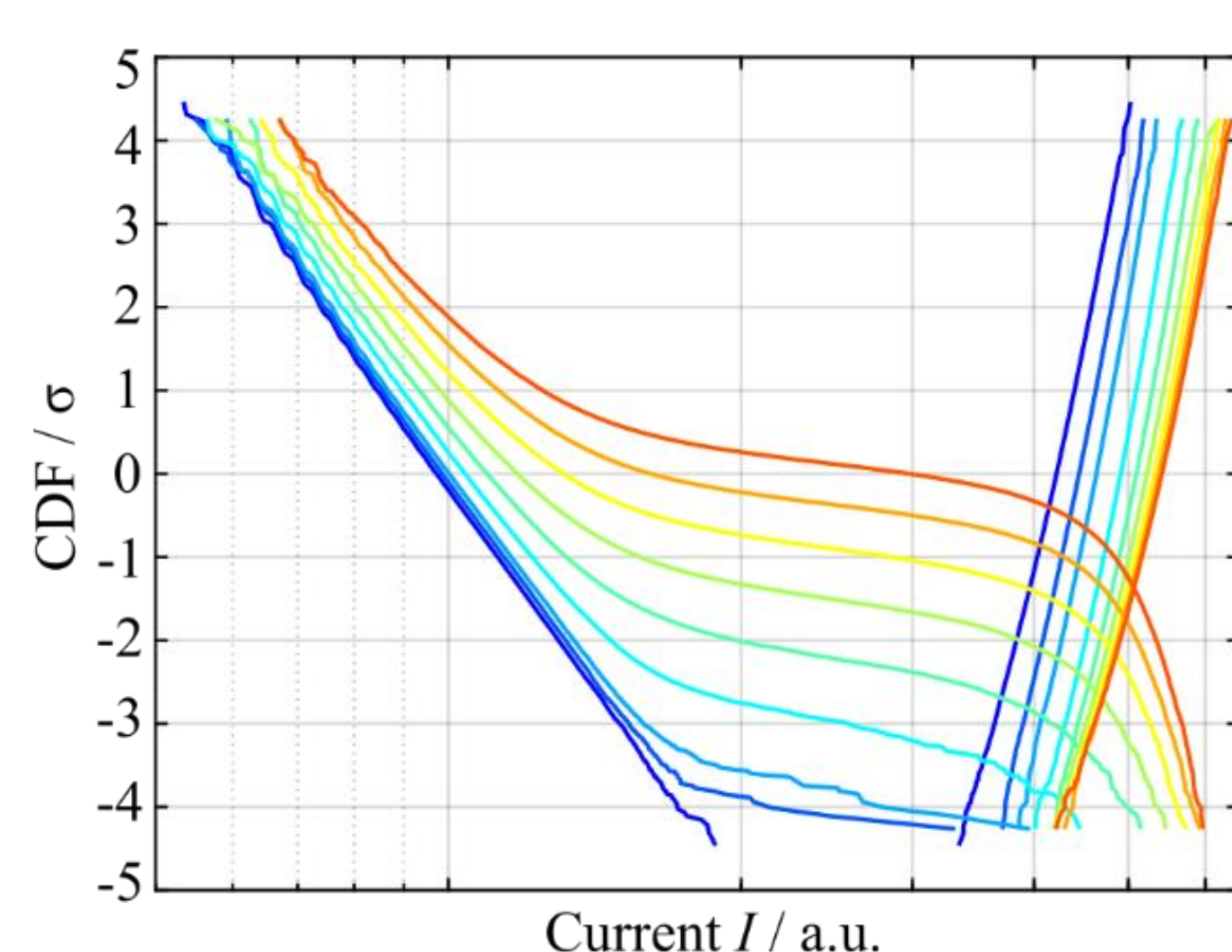
Simulation Results

Simulation of RESET pulse:

- Modeling of LRS distribution with number of oxygen vacancies in the disc and plug, and periphery resistance as parameters with variability
- Normal RESET from LRS to HRS (dark blue)
- Increasing number of oxygen vacancies in the disc for initial LRS
- Lower cell resistance
- RESET failure occurs where cells are only partly (green) or not (red) switched to HRS

Deep investigation of fail-bits:

- Comparison of read current before and after RESET
- RESET failure correlates with initial LRS current: Cells with high LRS current are more prone to failure, cell with low LRS current switch faultless
- In the zoom-in, even cells with higher current after RESET can be found
- Deep look at properties of cells that did not switch to HRS during RESET
- Failure probability in dependence of the periphery resistance and the number of oxygen vacancies in the disc (correlated to cell resistance)
- Combination of high periphery resistance and low cell resistance leads to RESET failure
- Underlines predictions from simple phenomenological model



References

- [1] N. Kopperberg *et al.*, "Endurance of 2 Mbit Based BEOL Integrated ReRAM," in *IEEE Access*, vol. 10, pp. 122696-122705, 2022, doi: 10.1109/ACCESS.2022.3223657.
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- [5] S. Menzel *et al.*, "Statistical modeling of electrochemical metallization memory cells," 2014 IEEE 6th International Memory Workshop (IMW), Taipei, Taiwan, 2014, pp. 1-4, doi: 10.1109/IMW.2014.6849360.