DESIGN AND CRYOGENIC CHARACTERIZATION OF INTEGRATED CIRCUITS FOR QUANTUM COMPUTING

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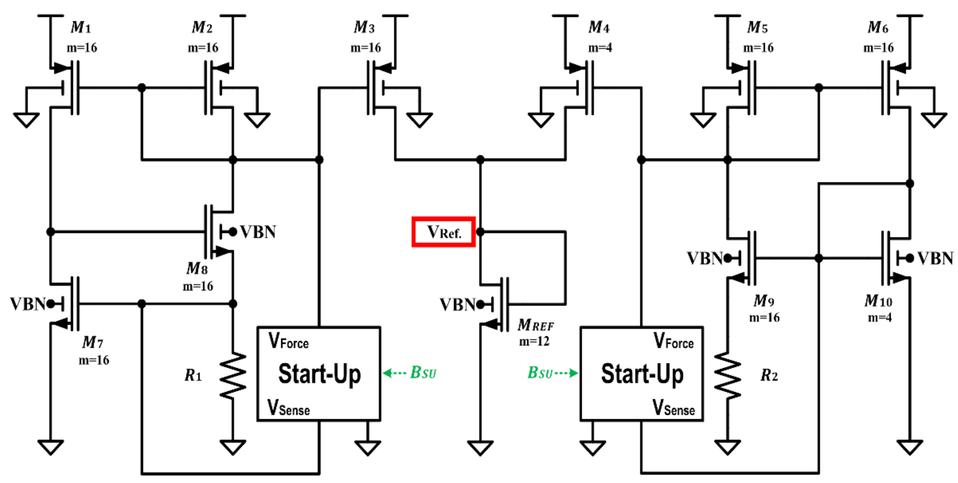

Fig. 1: Cryogenic voltage reference based on cryogenic Vth saturation phenomenon.

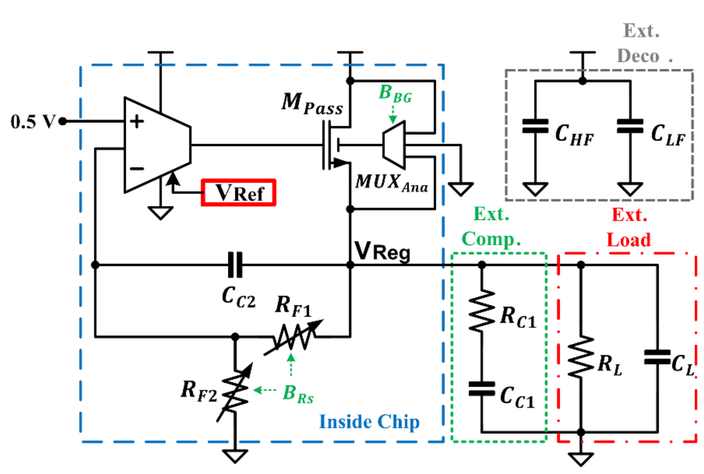

Fig. 2: Cryogenic voltage regulator, with its components integrated on chip and external elements.

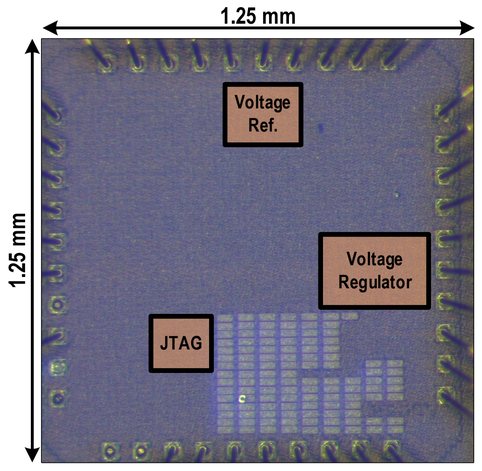

Fig. 3: Micrograph of a prototype IC manufactured in a commercial 22 nm FDSOI Technology.

1. MOTIVATION

- High performance Integrated Circuits (ICs) are a fundamental part of future Quantum Computers (QCs) [1].
- The ICs of QCs need regulated, stable and noise free supply voltages [2].
- Supply voltage lines in dilution fridges are prone to voltage ripple noise due to pulse tube vibrations, ground loops induce noise and dynamic load currents [3], [4].
- Cryogenic ICs for in situ voltage regulation can provide a clean voltage supply for the ICs of QCs.
- A voltage reference and a voltage regulator are presented as building blocks for cryogenic voltage regulation.
- The investigated circuits were developed in 22 nm FDSOI technology and tested from 6 K to 300 K.

2. INTEGRATED CIRCUITS DESCRIPTION

- The voltage reference circuit (Fig. 1) uses the cryogenic Vth saturation phenomenon as working principle.
- The circuit is composed of current sources that bias a diode connected NMOS device to yield the output reference voltage (VRef).
- VRef is a temperature stable quantity used in analog signal processing.
- The voltage regulator (Fig. 2) employs an NMOS pass element whose back-gate terminal connection can be shifted by an analog multiplexer via a JTAG interface.
- Back-gate shifting allows the NMOS pass element Vth reduction for power optimization at cryogenic temperatures.
- The output regulated voltage (VReg) can energize other cryogenic circuits with a stable power signal.
- The voltage reference, the voltage regulator and the JTAG interface are included in a prototype IC (Fig. 3) manufactured in a commercial 22 nm FDSOI technology.

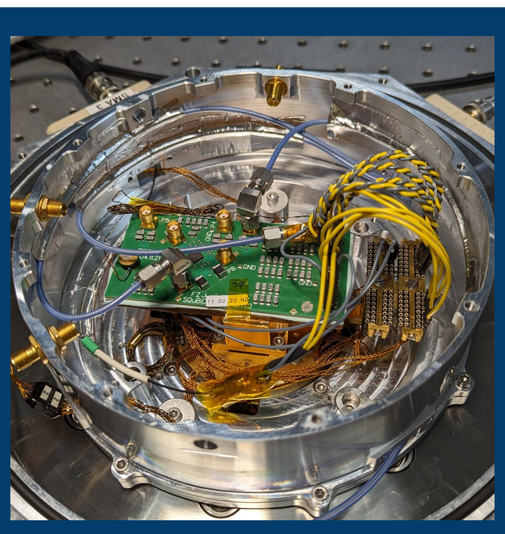

Fig. 4: Experimental setup: PCB with prototype IC, mounted onto the cryostat cold head (Gifford-McMahon cryocooler).

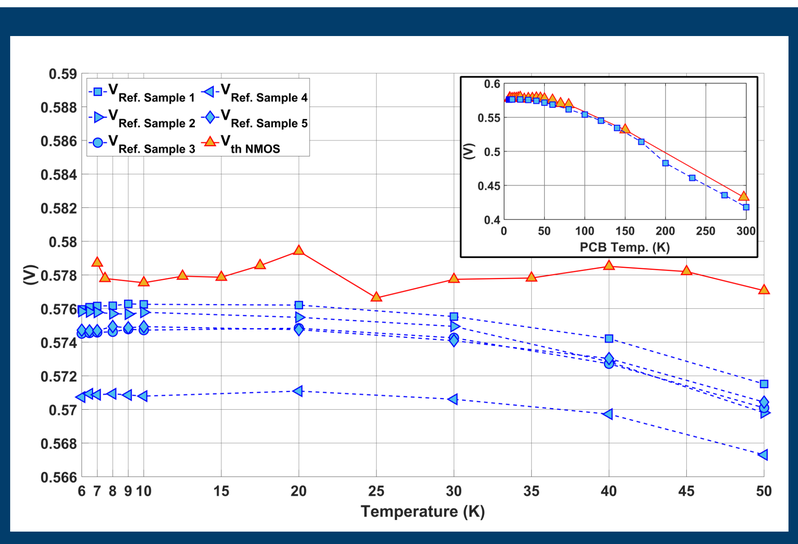

Fig. 5: Measured output from voltage reference over the temperature range of interest (6 K to 50 K), with VSup = 1.25 V and VBG = 0 V; results correspond to 5 sample chips. Extracted Vth from I/O NMOS (W = 1 µm, L = 0.32 µm) is added for comparison. Inset displays sample 1 data over a wider temperature range (6 K to 300 K).

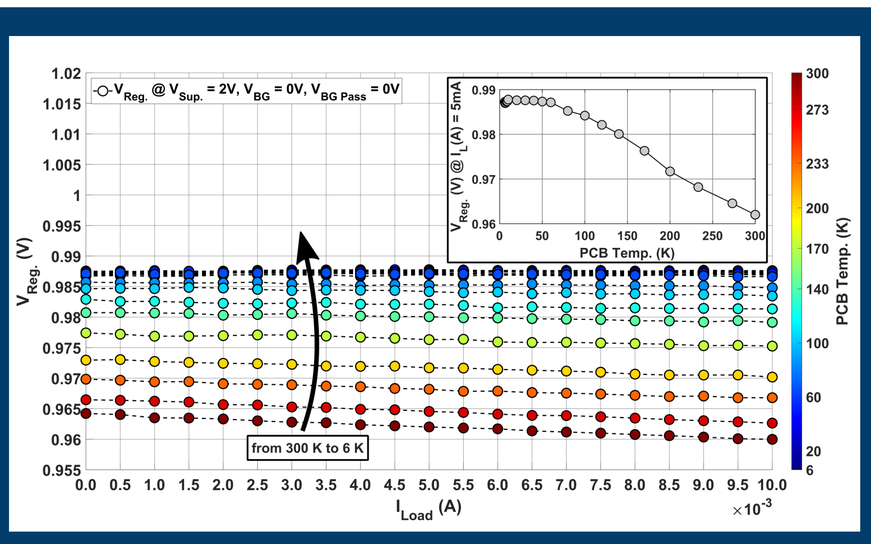

Fig. 6: Measured regulator output voltage (VReg) in relation to ILoad and temperature, at VIN Ref = 0.5 V, RF1 = RF2 , VBG = 0 V and VSup = 2 V. Inset displays VReg for ILoad = 5 mA over temperature (from 6 K to 300 K).

3. EXPERIMENTAL RESULTS

- A prototype IC is mounted over the cryostat cold head (Gifford-McMahon cryocooler) via a PCB specially designed for good thermal coupling (Fig. 4).
- Fig. 5 shows the response from the voltage reference circuit, with a temperature coefficient of 300 ppm/K, over the 6 K to 50 K range.
- Fig. 6 shows the voltage regulator response, with load regulation of 22 mV/A at 6 K.
- The studied circuits served as exploration vehicles to gain inside into the design and electrical characterization of cryogenic ICs [5], [6].

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