

POWER INTEGRITY CHALLENGES IN LARGE SCALE QUANTUM COMPUTERS AND SOLUTIONS

IEEE Workshop on Quantum Computing: Devices, Cryogenic Electronics and Packaging
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25.10.2023 | A. R. CABRERA-GALICIA, ZEA-2

OVERVIEW

- Motivation
- Power Integrity Challenges for Cryogenic ICs
- Proposed Solution: Cryogenic Voltage Regulation
- Application Case: Voltage References for DAC
- Conclusions

MOTIVATION

Brief summary

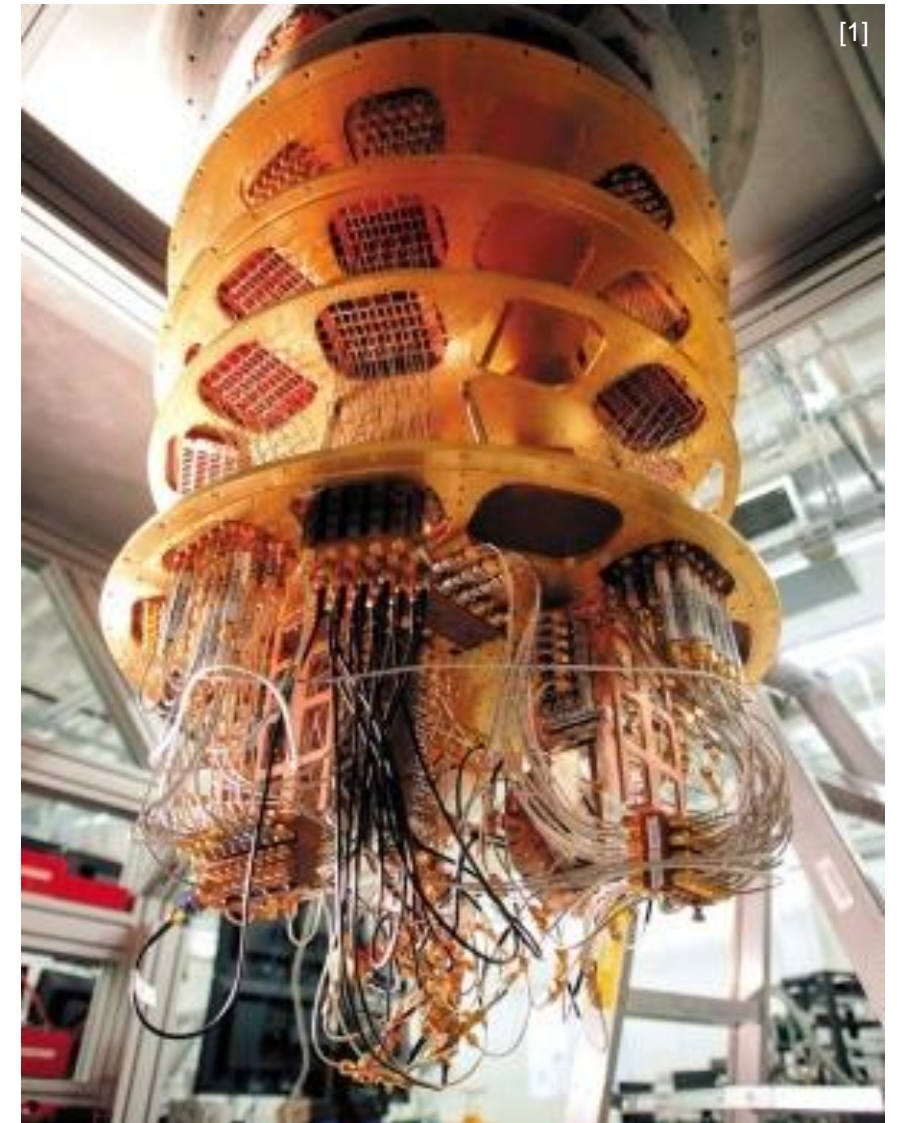
- Quantum computing will speed up solution finding in drug design, cryptography, optimization.
- Universal quantum computers needs 10^6 to 10^9 physical qubit, due to non-idealities ^[1].
- Current RT approaches are not fully scalable ^{[2],[3]}.

Local cryo-electronics
with system integration view is needed!

Regulated and stable supply voltage in situ is required for optimum operation.

[1] Mohseni, Masoud, et al. "Commercialize quantum technologies in five years." *Nature* 543.7644 (2017): 171-174.
[2] Charbon, Edoardo, et al. "Cryogenic CMOS circuits and systems: Challenges and opportunities in designing the electronic interface for quantum processors." *IEEE Microwave Magazine* 22.1 (2020): 60-78.
[3] Degenhardt, C., et al. "Systems engineering of cryogenic CMOS electronics for scalable quantum computers." *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019.

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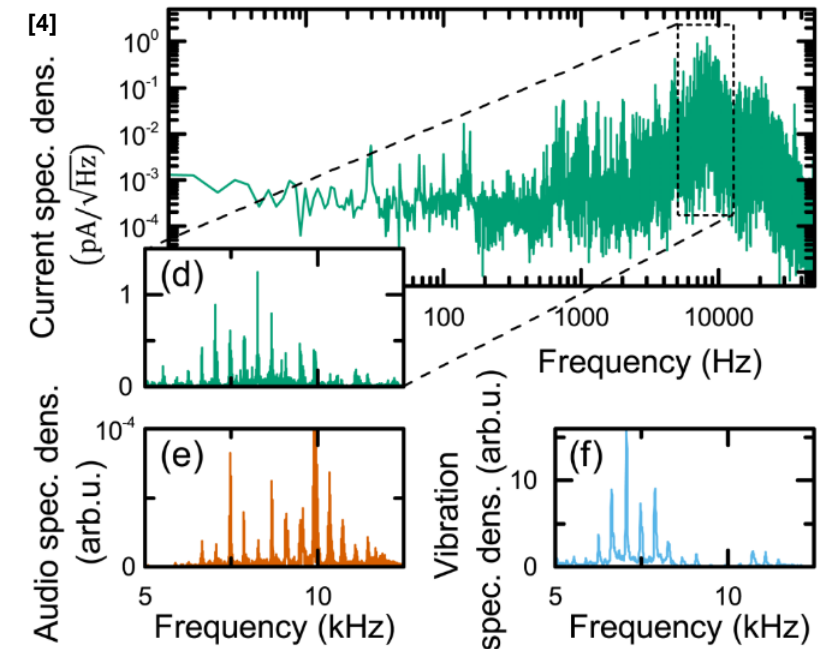
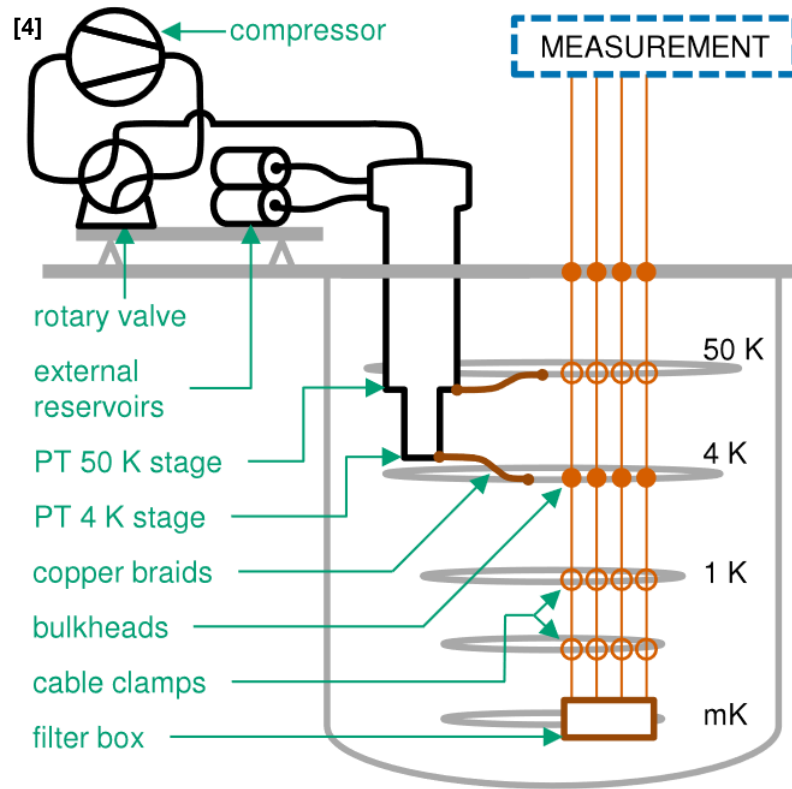


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POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Vibration-induced electrical noise



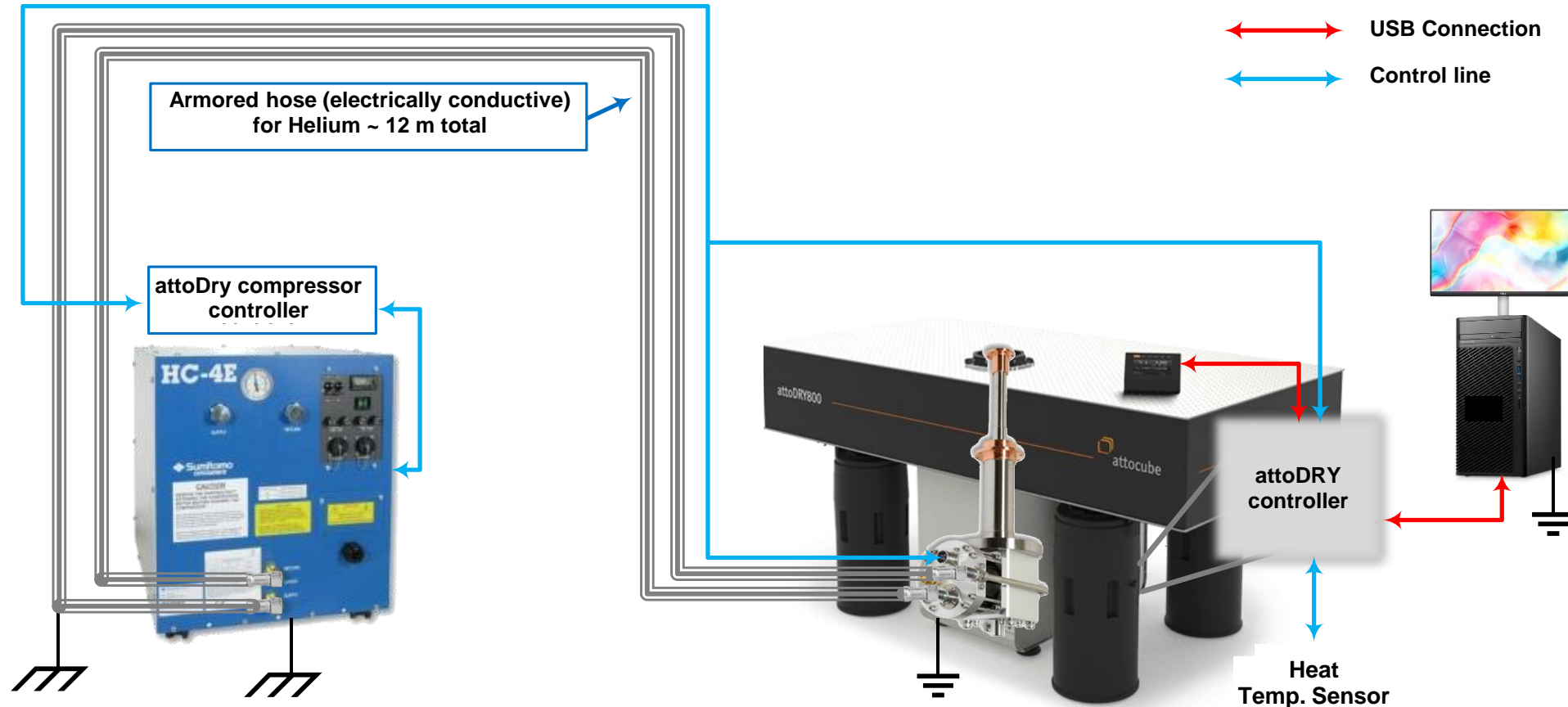
Cryocooler (e. g. pulse tube) in dilution fridge produces vibrations [4],[5].

[4] Kalra, Rachpon, et al. "Vibration-induced electrical noise in a cryogen-free dilution refrigerator: Characterization, mitigation, and impact on qubit coherence." *Review of Scientific Instruments* 87.7 (2016).

[5] Lake Shore Cryoelectronics, "Pulse tube cryocoolers vs Gifford-McMahon cryocoolers," <https://www.lakeshore.com/products/product-detail/janis/pulse-tube-cryocoolers-vs.-gifford-mcmahon-cryocoolers>.

POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Ground loop in Gifford-McMahon cryocooler (attoDRY800)



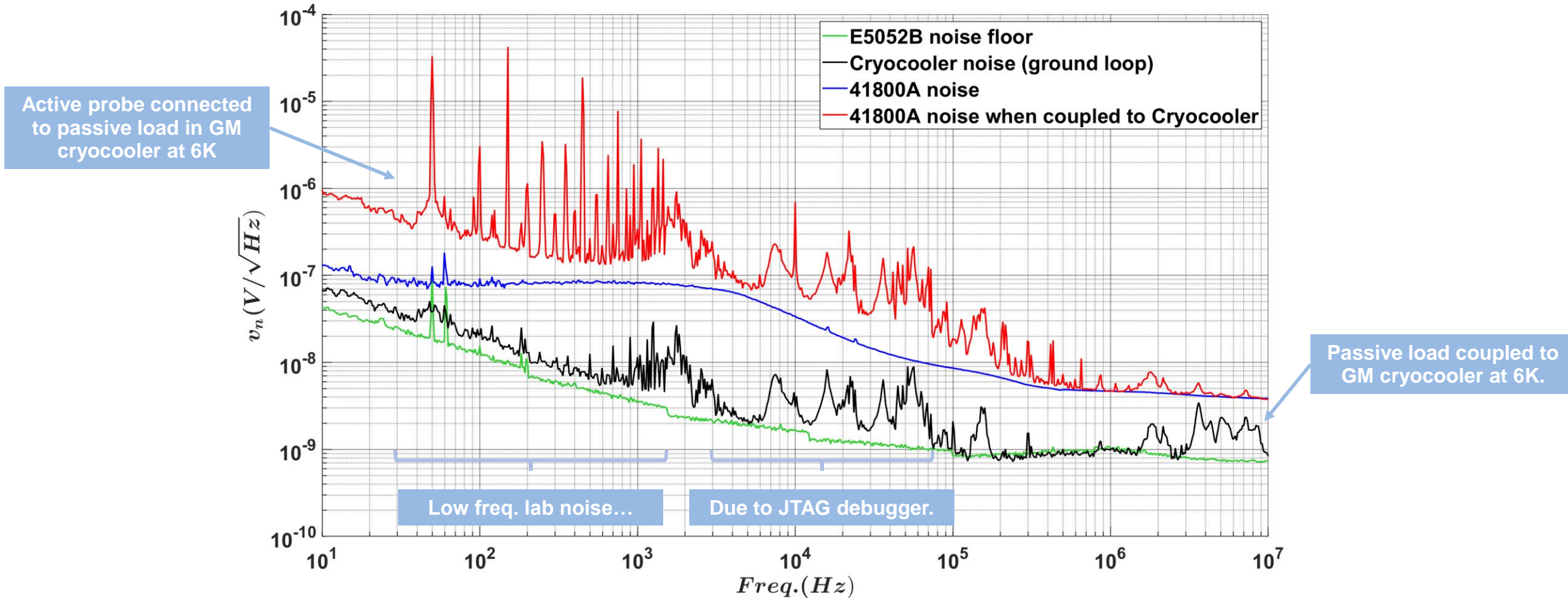
[6] Ott, Henry W. *Electromagnetic compatibility engineering*. John Wiley & Sons, 2011.

[7] Sumitomo Heavy Industries, Ltd., <https://www.shicryogenics.com/>

[8] attocube systems AG, <https://www.attocube.com/en>

POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Ground loop impact on active probe (41800A) as example



POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Power distribution for cryogenic ICs

- Complex ICs for Quantum Computing need local power distribution networks due to:

- Limited connections between Cryo. stage and RT.
- Different power domains needed; Analog, Digital, Mixed Signal.
- No commercial DC-DC converters for Cryo. ($4\text{K} \leq \text{Temp.} \leq 7\text{K}$) [9], [10]



[9] Homulle, Harald, et al. "Design techniques for a stable operation of cryogenic field-programmable gate arrays." *Review of Scientific Instruments* 89.1 (2018): 014703.

[10] H. Homulle and E. Charbon, "Cryogenic low-dropout voltage regulators for stable low-temperature electronics," *Cryogenics*, vol. 95, 2018.

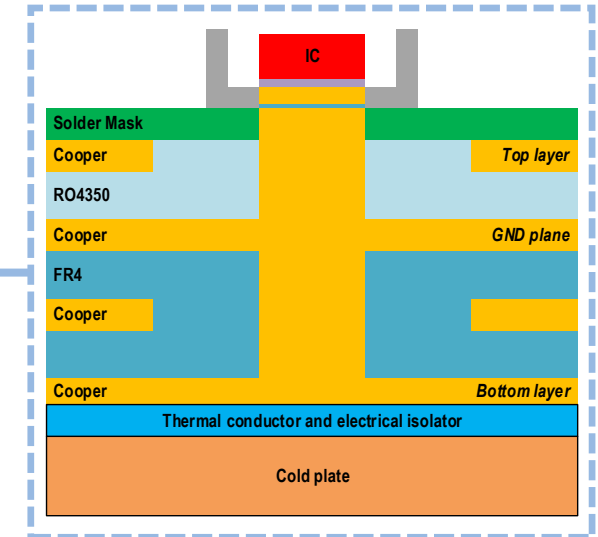
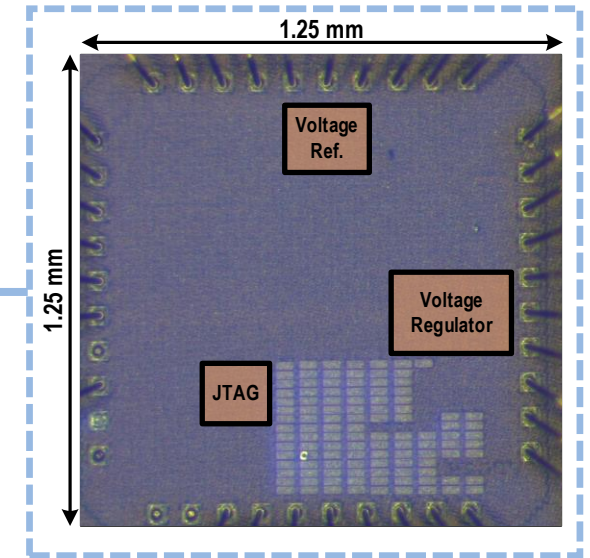
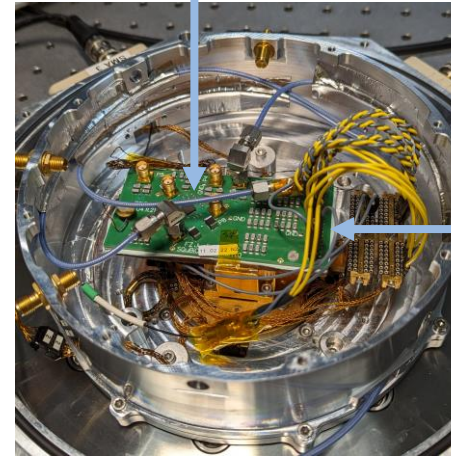
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- **Proposed Solution: Cryogenic Voltage Regulation**
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CRYOGENIC VOLTAGE REGULATION

Prototype

- IC (22 nm FDSOI): Voltage Ref., Voltage Reg. and JTAG interface^[11].
- PCB for good cryocooler – IC thermal coupling.
- Thermal pad to break ground loop.
- Test temps.: [300 K, 6 K].



[11] A. R. Cabrera-Galicia *et al.*, "A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology," to be published in 2023 IEEE 19th Asia Pacific Conference on Circuits and Systems (APCCAS), 2023.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

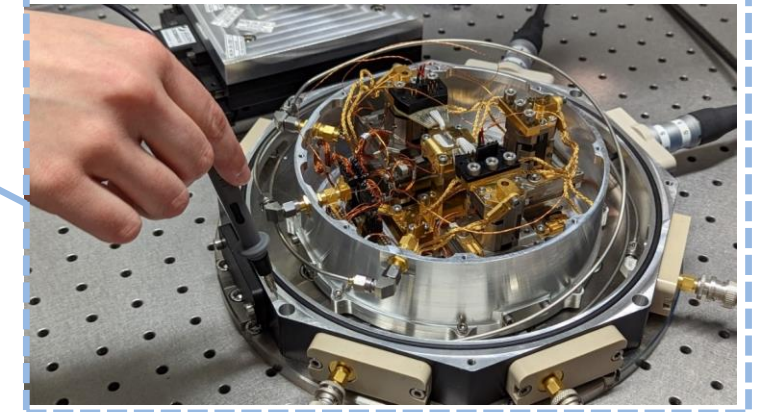
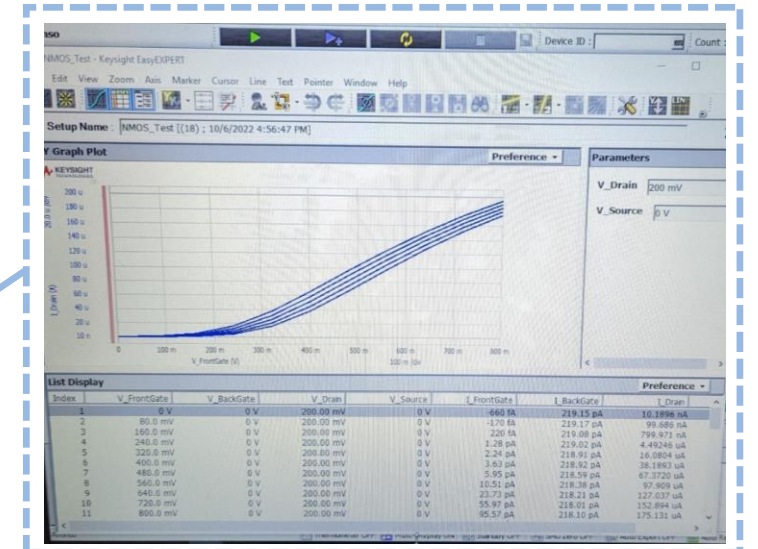
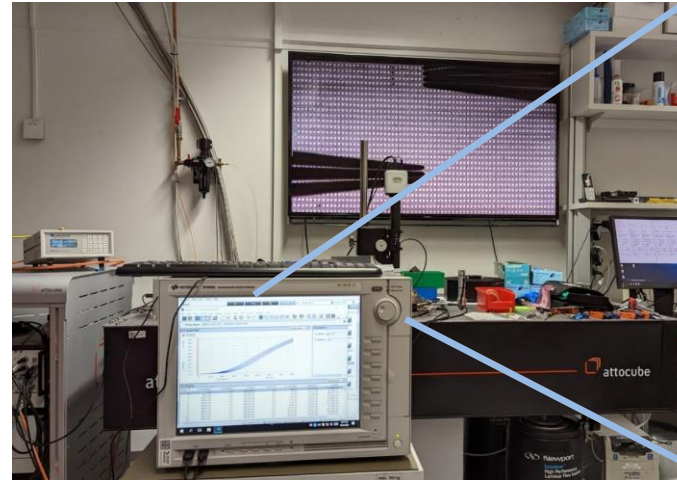
Cryogenic electrical characterization of 22 nm FDSOI

- **Setup:**

- Gifford-McMahon cryocooler (attoDRY800); 7K with needle probing station.
- Semiconductor device analyzer (B1500A).

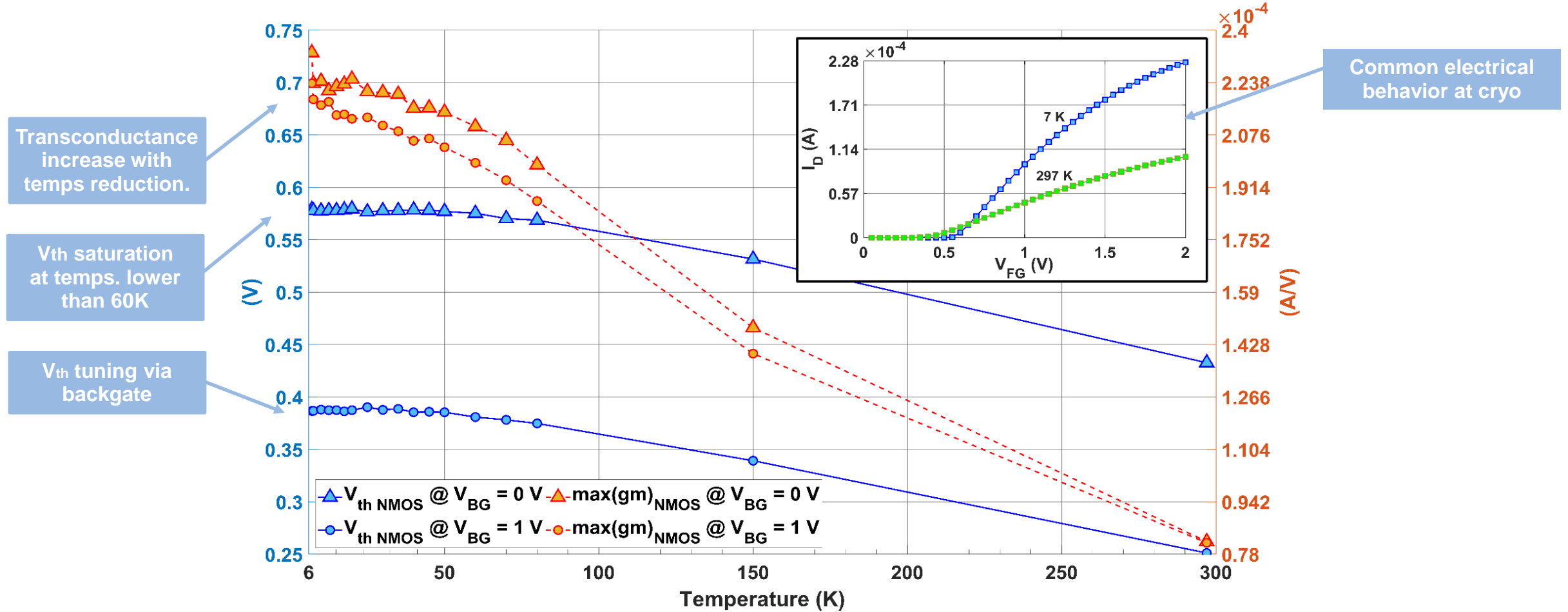
- **Objective:**

to develop a cryogenic simulation model for 22 nm FDSOI;
QSolid collaborative project ^[12]



CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

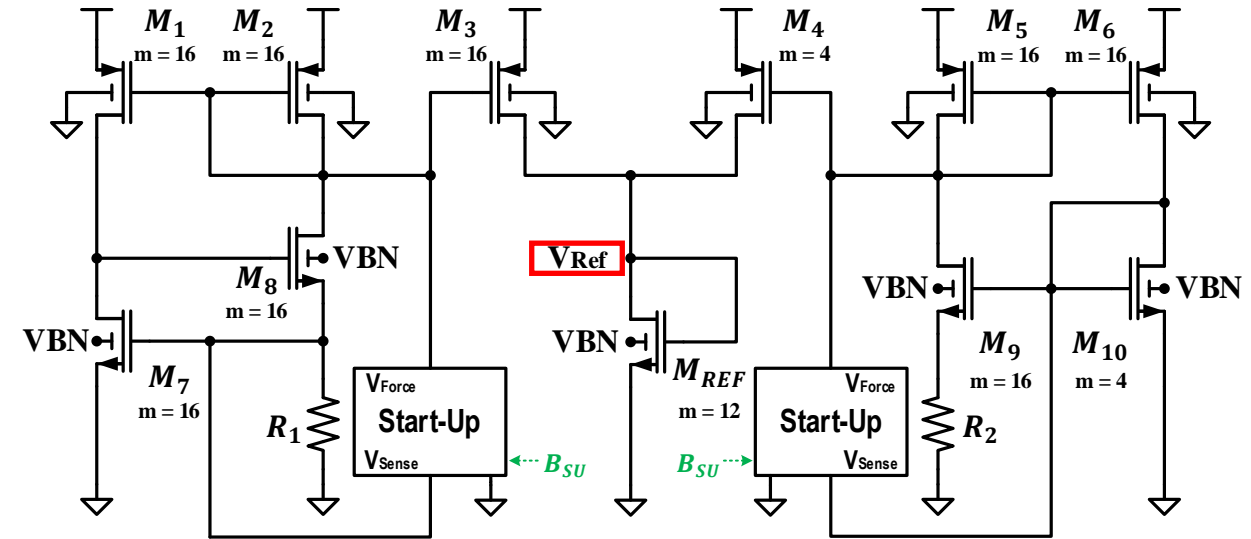
Cryogenic electrical characterization of 22 nm FDSOI



CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

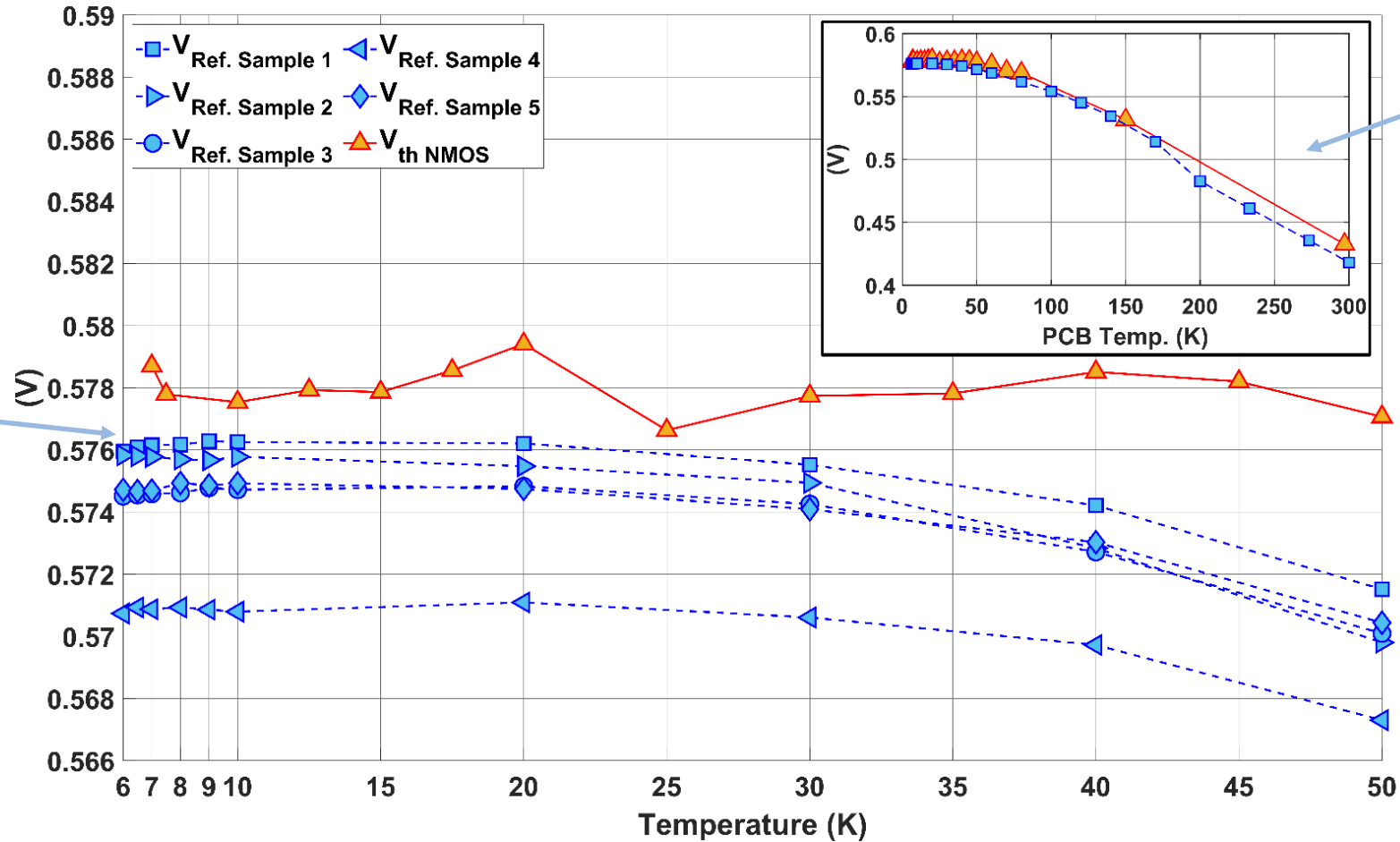
Voltage reference

- Cryogenic V_{th} saturation as working principle.
- The circuit saturates M_{REF} while in V_{th} saturation temperature region.
- Simple and without post-fabrication correction.



CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

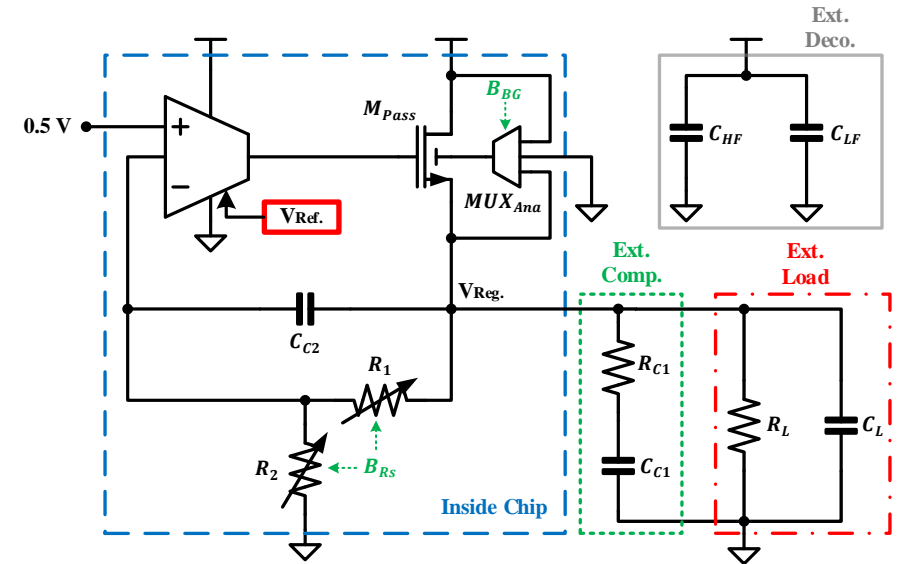
Voltage reference cryogenic test



CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator

- NMOS pass element (M_{Pass}); better PSRR than PMOS [14].
- M_{Pass} V_{th} reduction via backgate for low $V_{Sup.}$ requirement.
- $V_{Reg.}$ tuning via feedback modification with JTAG.
- Cryogenic-stable RC compensation network [10].

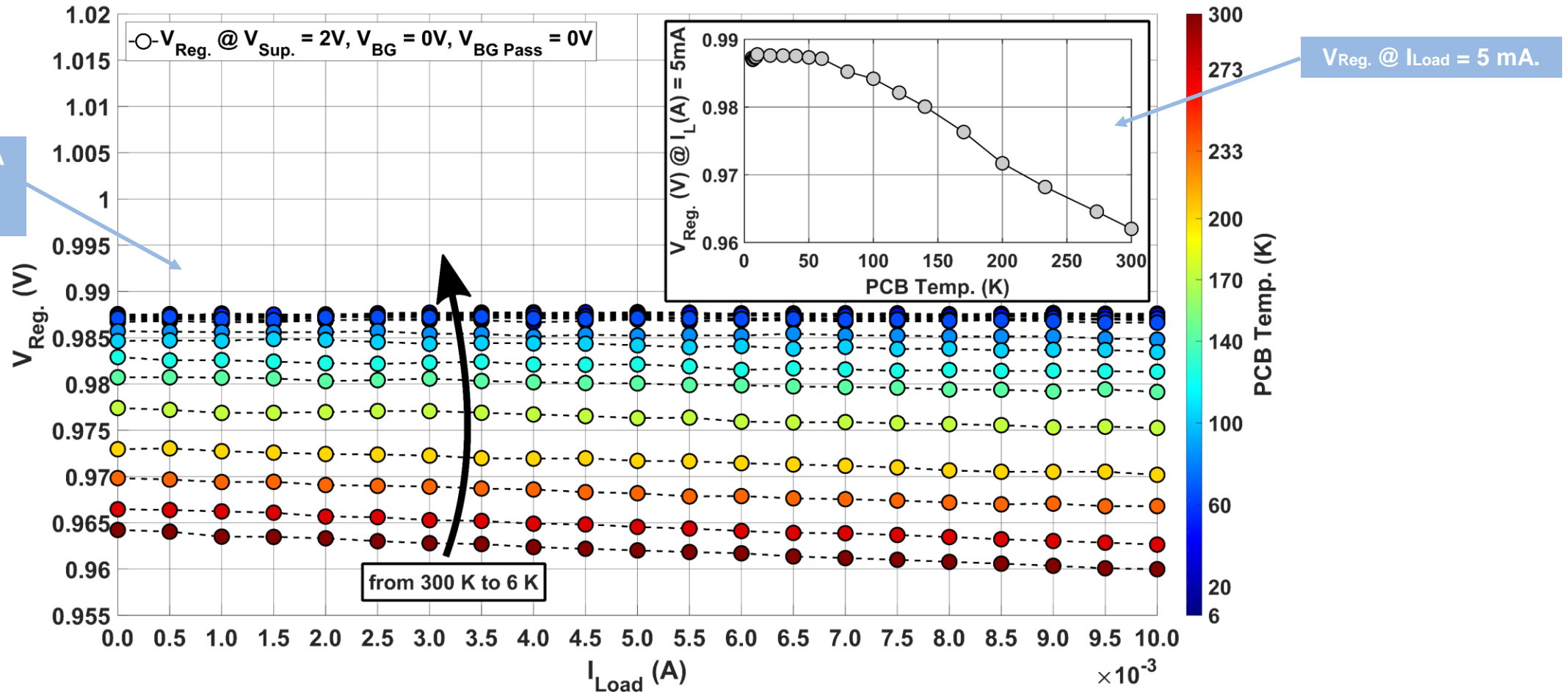


[10] H. Homulle and E. Charbon, "Cryogenic low-dropout voltage regulators for stable low-temperature electronics," Cryogenics, vol. 95, 2018.

[14] B. Razavi, "The low dropout regulator [a circuit for all seasons]," IEEE Solid-State Circuits Magazine, vol. 11, no. 2, 2019.

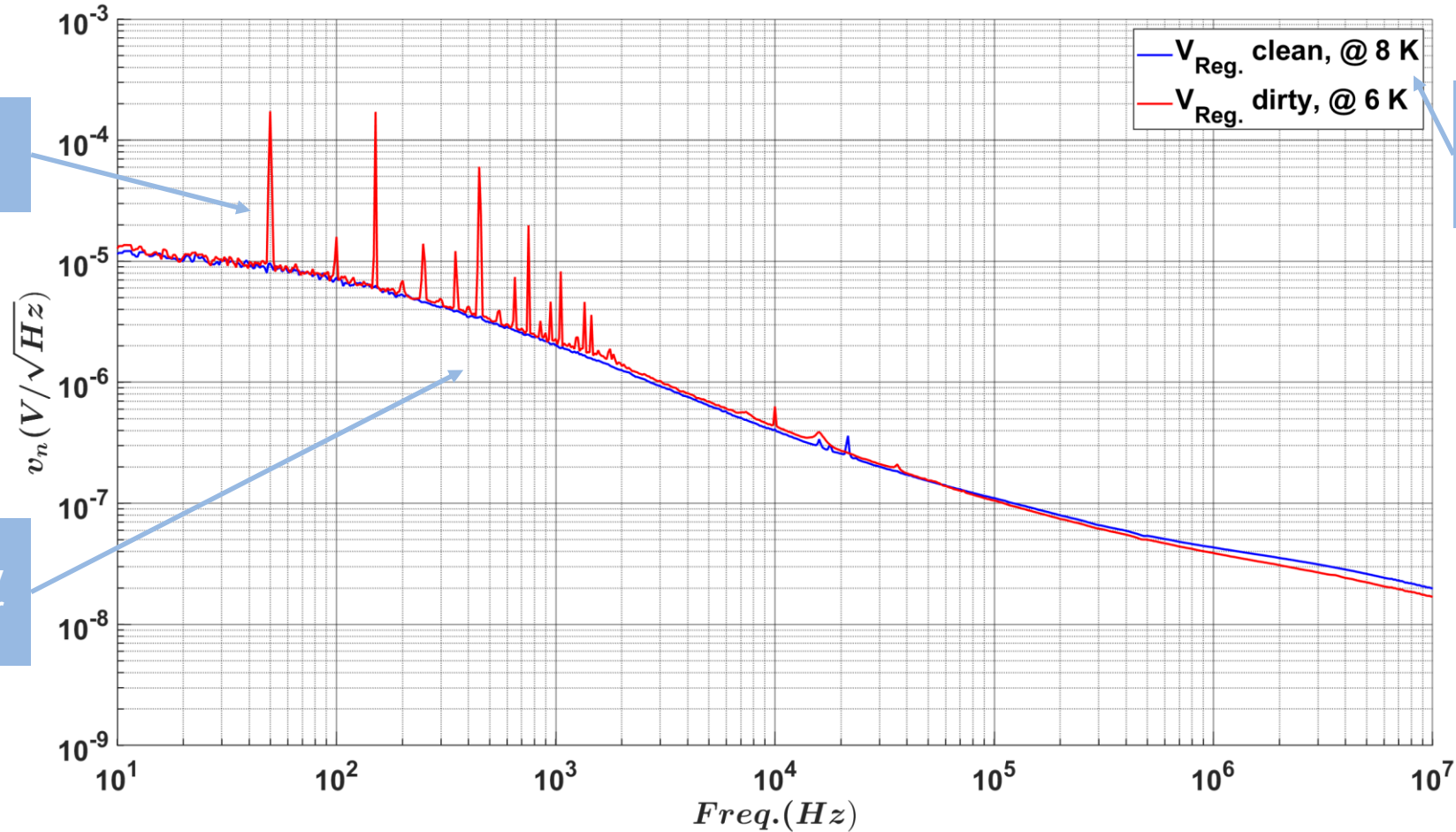
CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator cryogenic test; load regulation



CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator cryogenic test; noise spectral density



Ground loop noise is coupled to regulator output via cold plate.

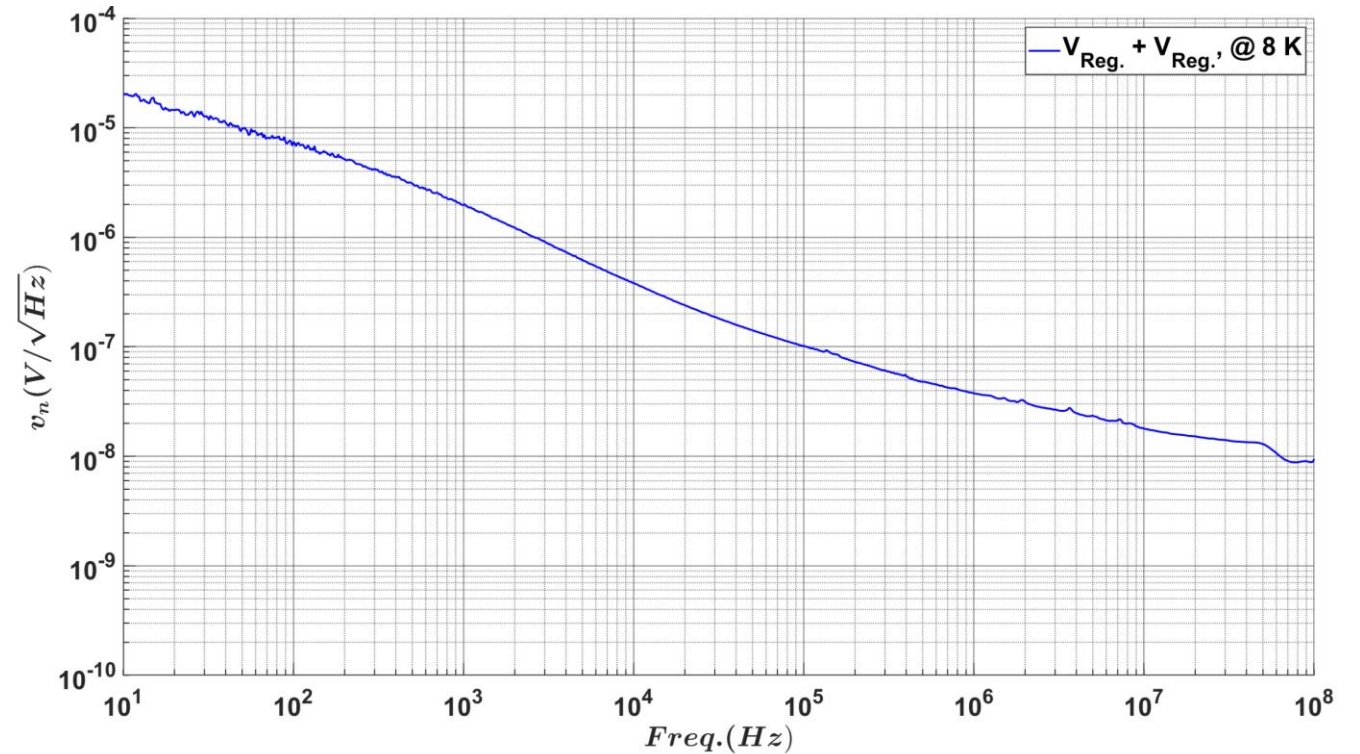
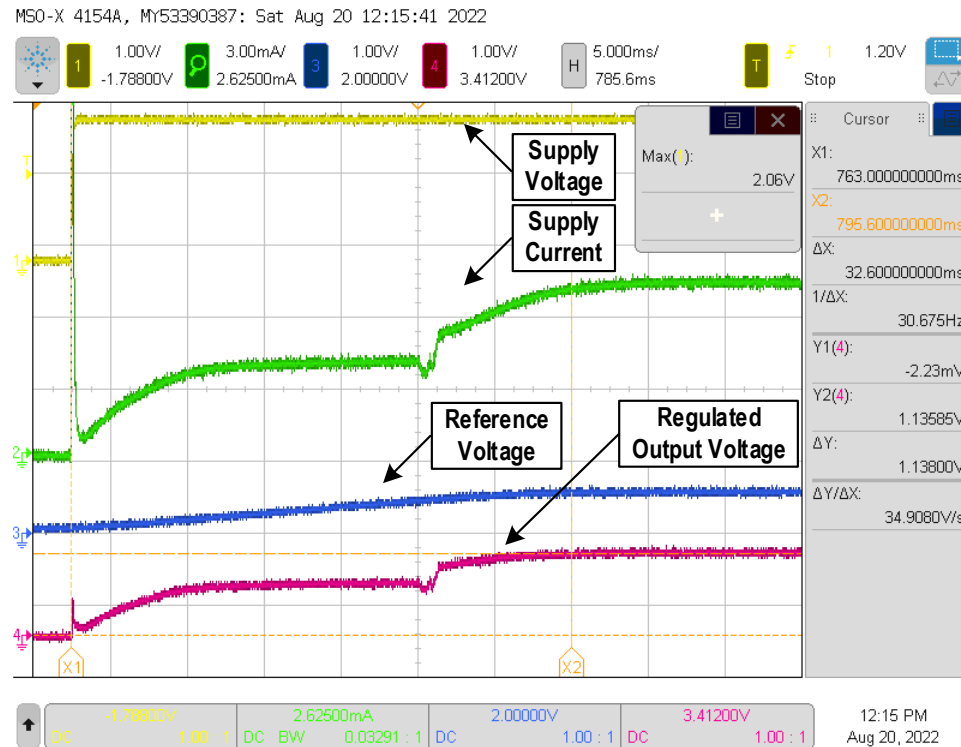
Ground loop noise is removed by electrically detaching the regulator from the cold plate.

Higher temp. due to thermal pad and imperfect thermalization of cables; improvement on progress.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

$V_{\text{Ref.}} + V_{\text{Reg.}}$ cryogenic test

Transient response and spectral noise density measured at cryo.



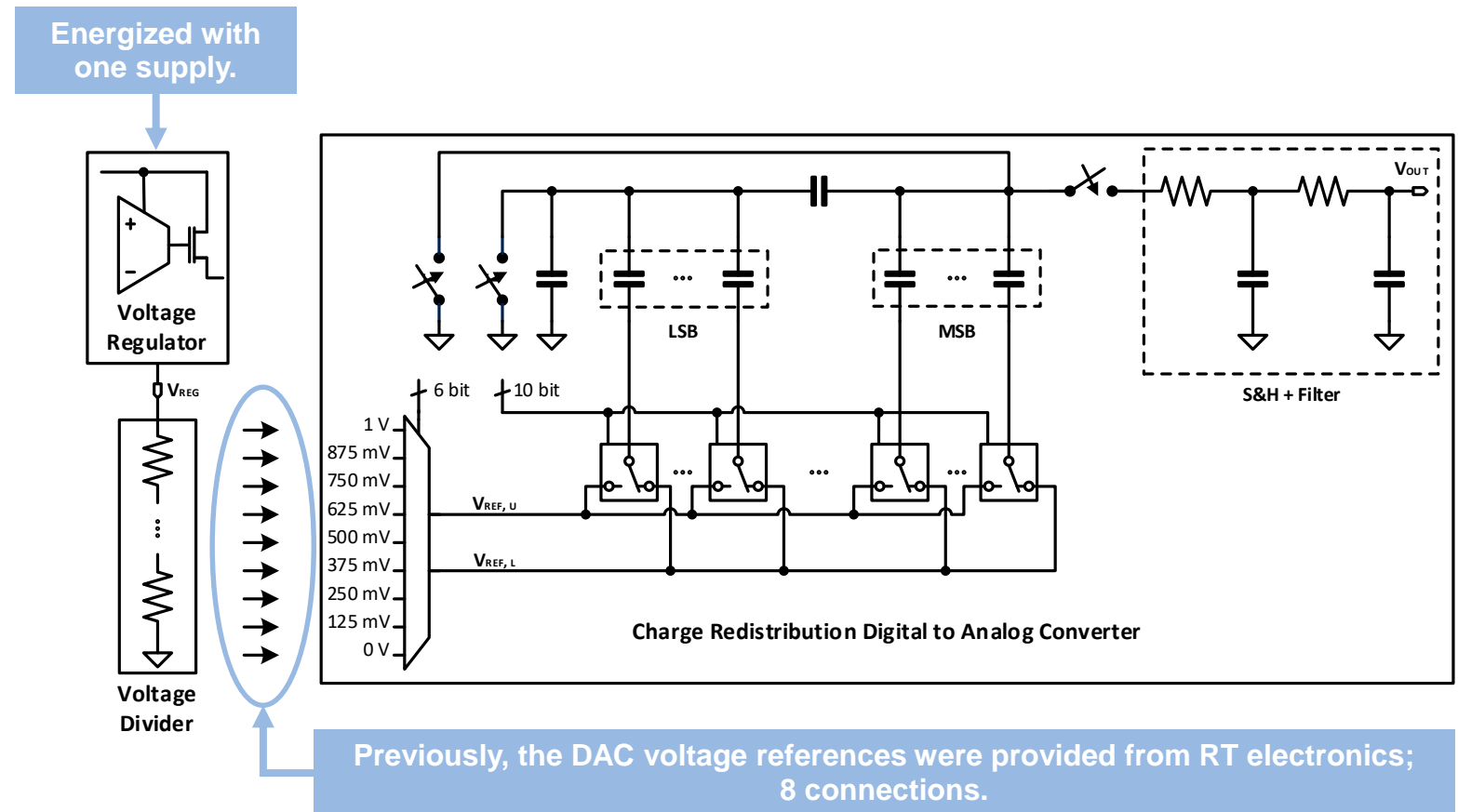
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APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{\text{Reg.}}$ + DAC at cryogenic temperatures

- **Objective:**
to showcase the operation of multiple ICs on Cryo.
- DAC (65 nm CMOS) [12]
 $V_{\text{Reg.}}$ (22 nm FDSOI).

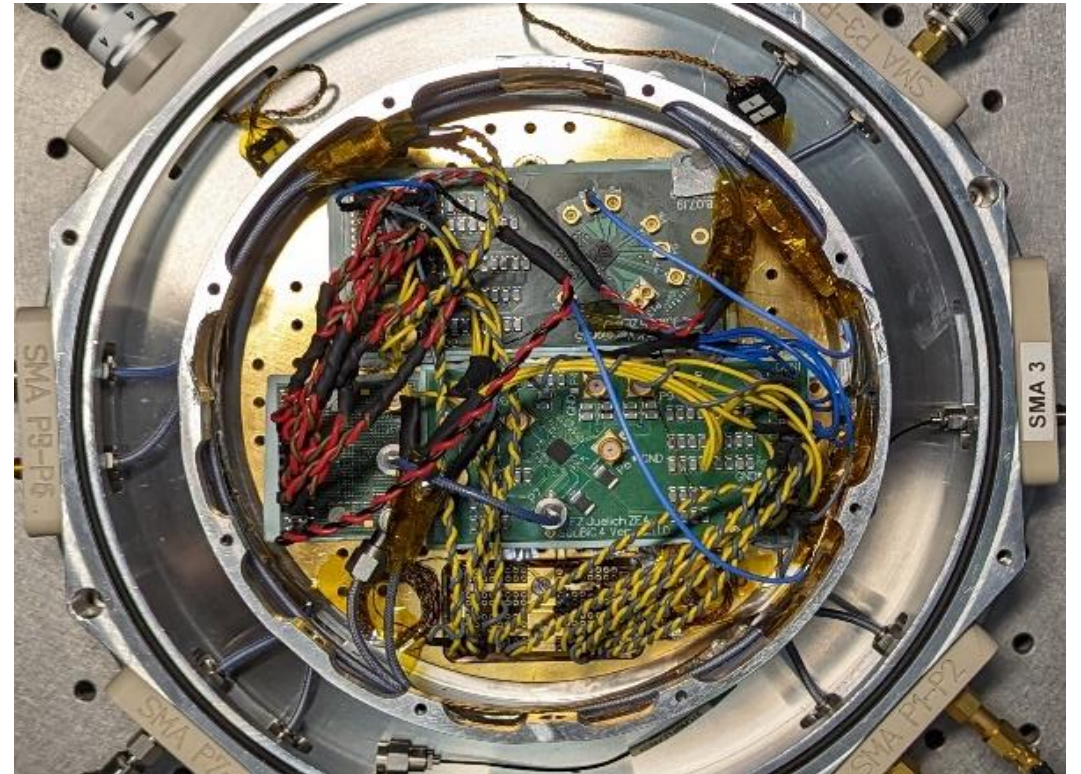
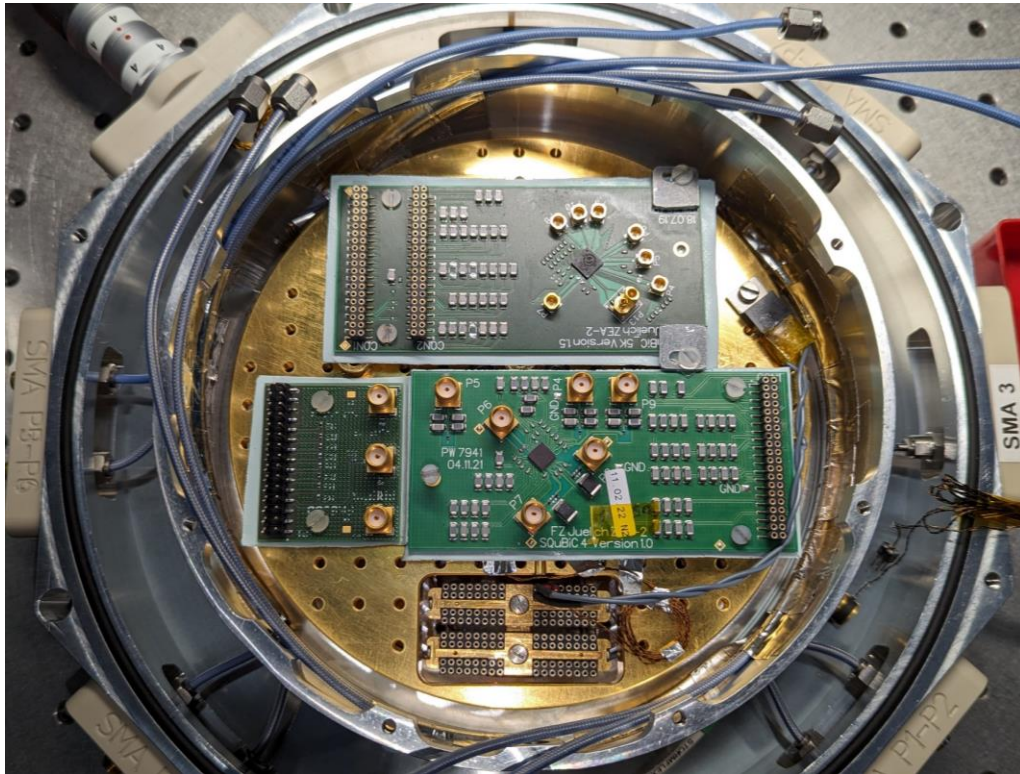


[15] Vliex, Patrick, et al. "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications." *IEEE solid-state circuits letters* 3 (2020): 218-221.

APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{\text{Reg.}}$ + DAC at cryogenic temperatures

First trial: quick and dirty!



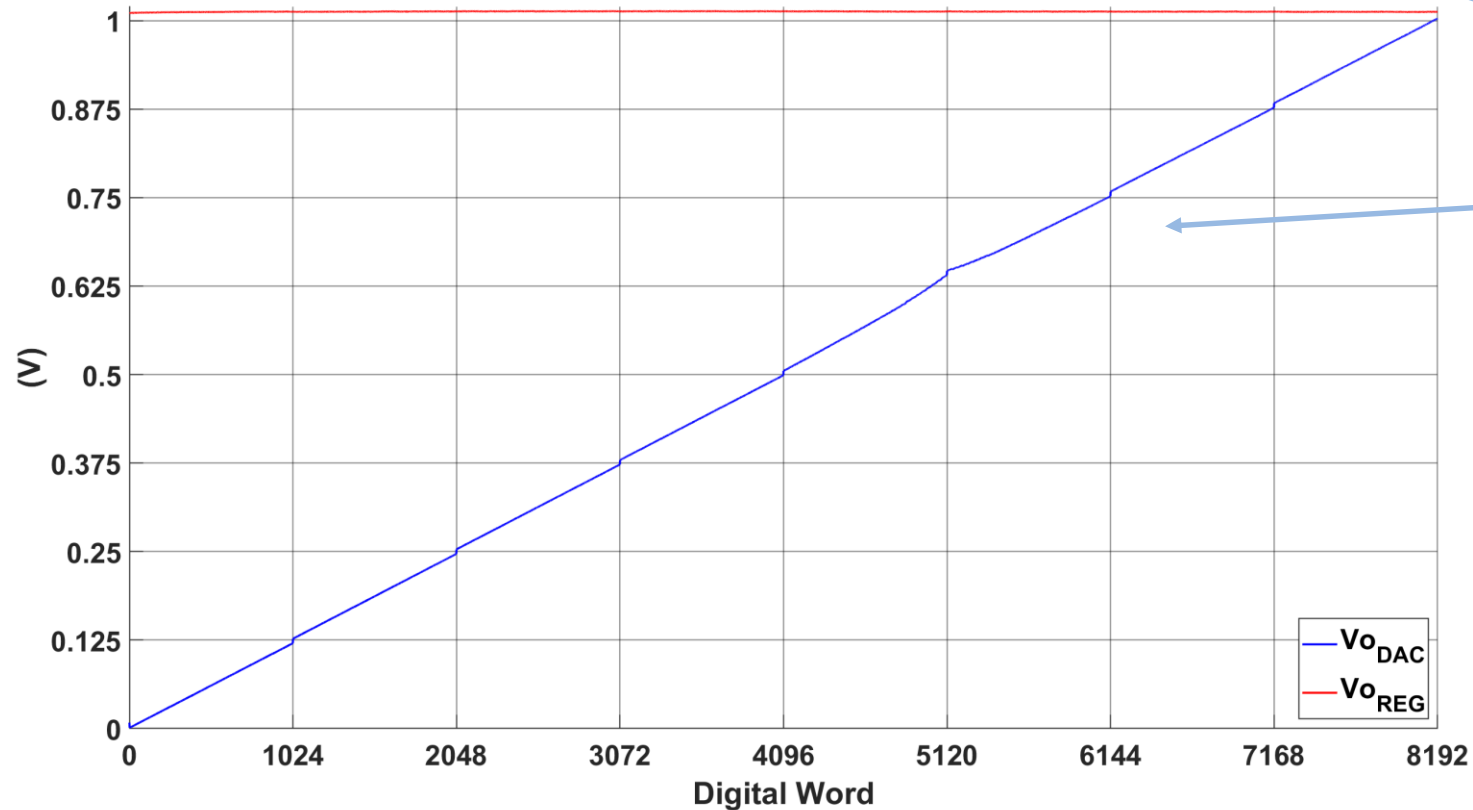
APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{\text{Reg.}}$ + DAC at cryogenic temperatures

PCB temp. is 11 K;
optimization on
cryocooler cabling is
needed.

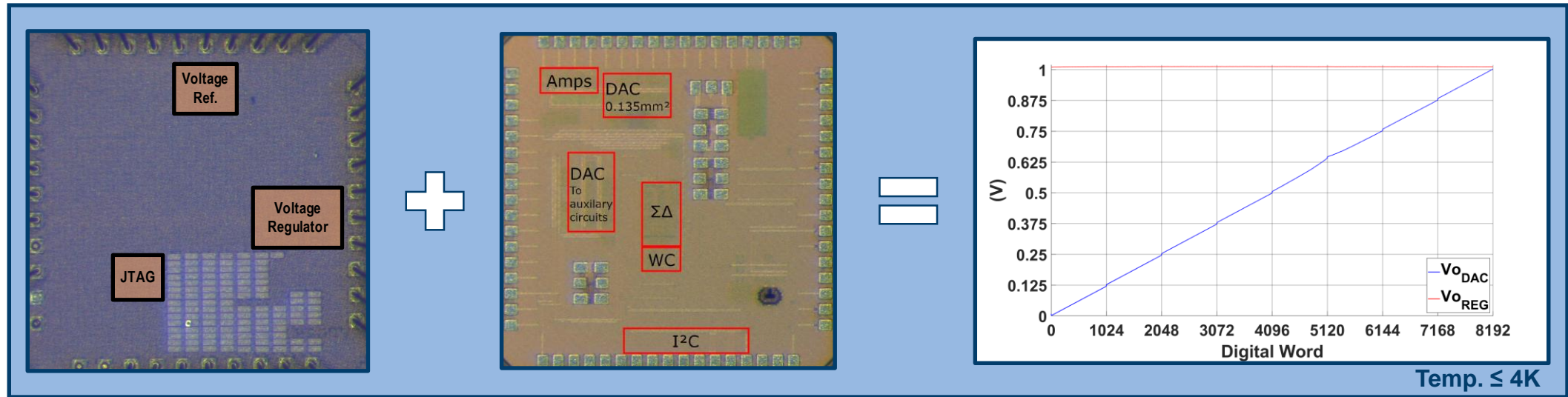
Dedicated PCB for
both ICs will improve
the area and
connections.

Work on progress;
first results.



CONCLUSIONS

- Cryogenic ICs need local power distribution network.
- Dilution refrigerators challenges: vibration induced noise, ground loops, limited connections.
- ICs and physical setups are the solution to the challenges.



THANKS FOR YOUR ATTENTION

ZEA-2



**André
Zambanini**



**Carsten
Degenhardt**



**Christian
Grewing**



**Stefan
van Waasen**



**Arun
Ashok**



**Andre
Kruth**



**Dennis
Nielinger**



**Patrick
Vliex**



**Alfonso Rafael
Cabrera Galicia**



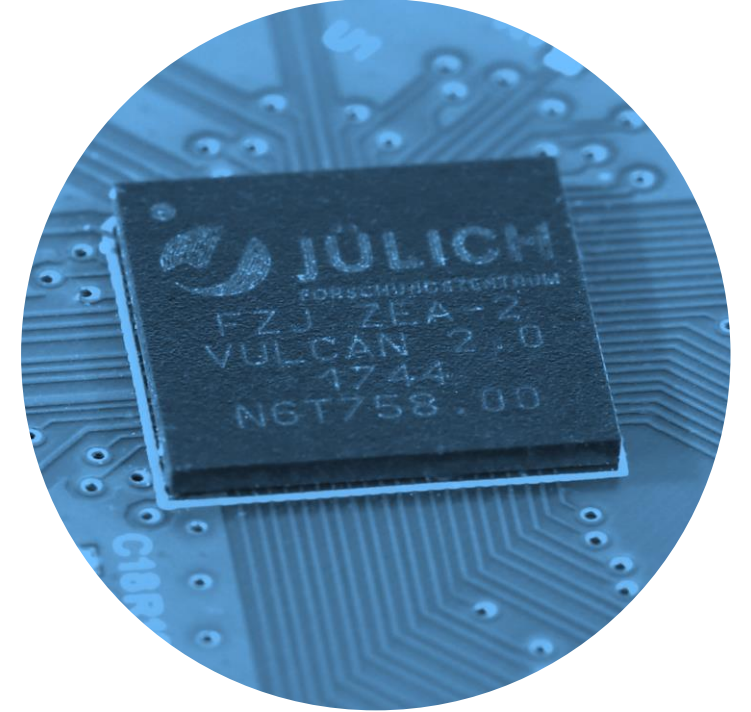
**Lea
Schreckenberg**



**Phanish
Chava**



**Swasthik
B. S. Bhat**



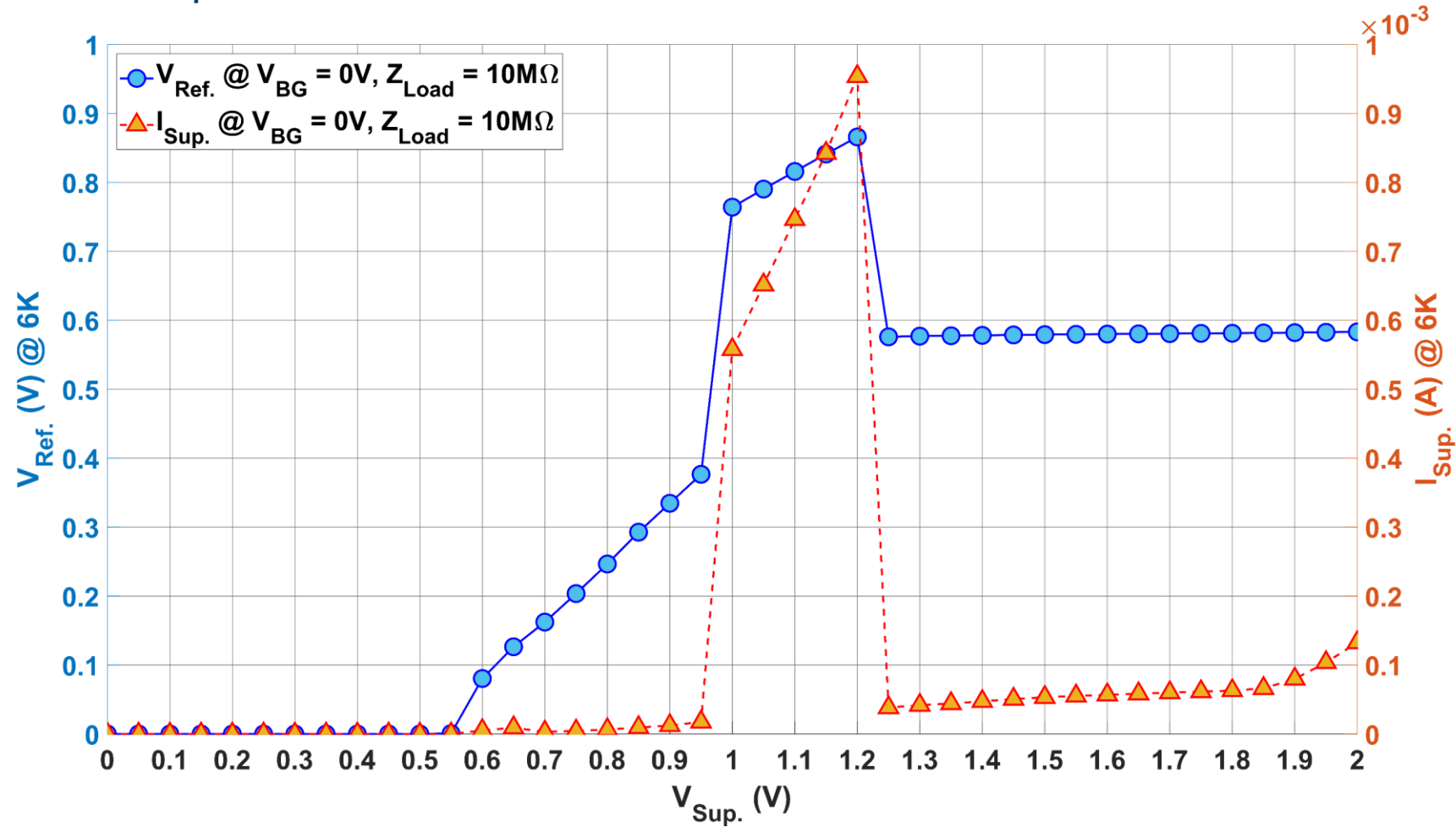
IC Development Team

REFERENCES

- [1] Mohseni, Masoud, et al. "Commercialize quantum technologies in five years." *Nature* 543.7644 (2017): 171-174.
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- [6] Ott, Henry W. *Electromagnetic compatibility engineering*. John Wiley & Sons, 2011.
- [7] Sumitomo Heavy Industries, Ltd., <https://www.shicryogenics.com/>
- [8] attocube systems AG, <https://www.attocube.com/en>
- [9] Homulle, Harald, et al. "Design techniques for a stable operation of cryogenic field-programmable gate arrays." *Review of Scientific Instruments* 89.1 (2018): 014703.
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- [12] The QSolid consortium, "QSolid, Quantum Computer in the Solid State," <https://www.q-solid.de/> .
- [13] A. R. Cabrera-Galicia *et al.*, "Towards the Development of Cryogenic Integrated Power Management Units," *2022 IEEE 15th Workshop on Low Temperature Electronics (WOLTE)*.
- [14] B. Razavi, "The low dropout regulator [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 11, no. 2, 2019.
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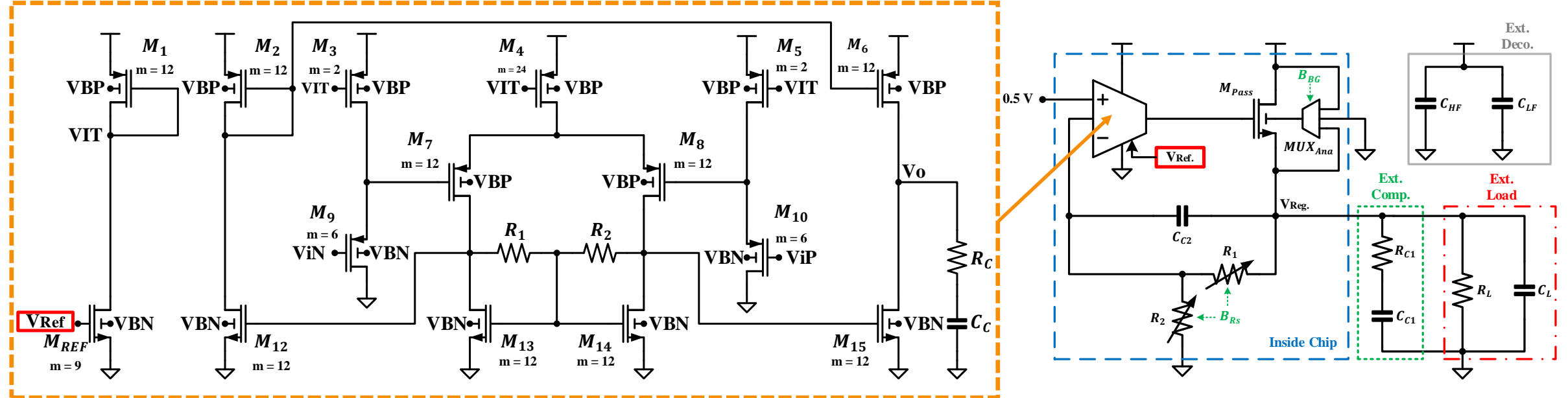
BACKUP

$V_{\text{Ref.}}$ with respect to $V_{\text{Sup.}}$ at 6K



BACKUP

Differential amplifier used by regulator



$$A_{DA} \approx g_{m_{7,8}} \cdot (R_{1,2} \parallel r_{o_{7,8}} \parallel r_{o_{13,14}}) \cdot g_{m_{12,15}} \cdot Z_{out} \quad (1)$$

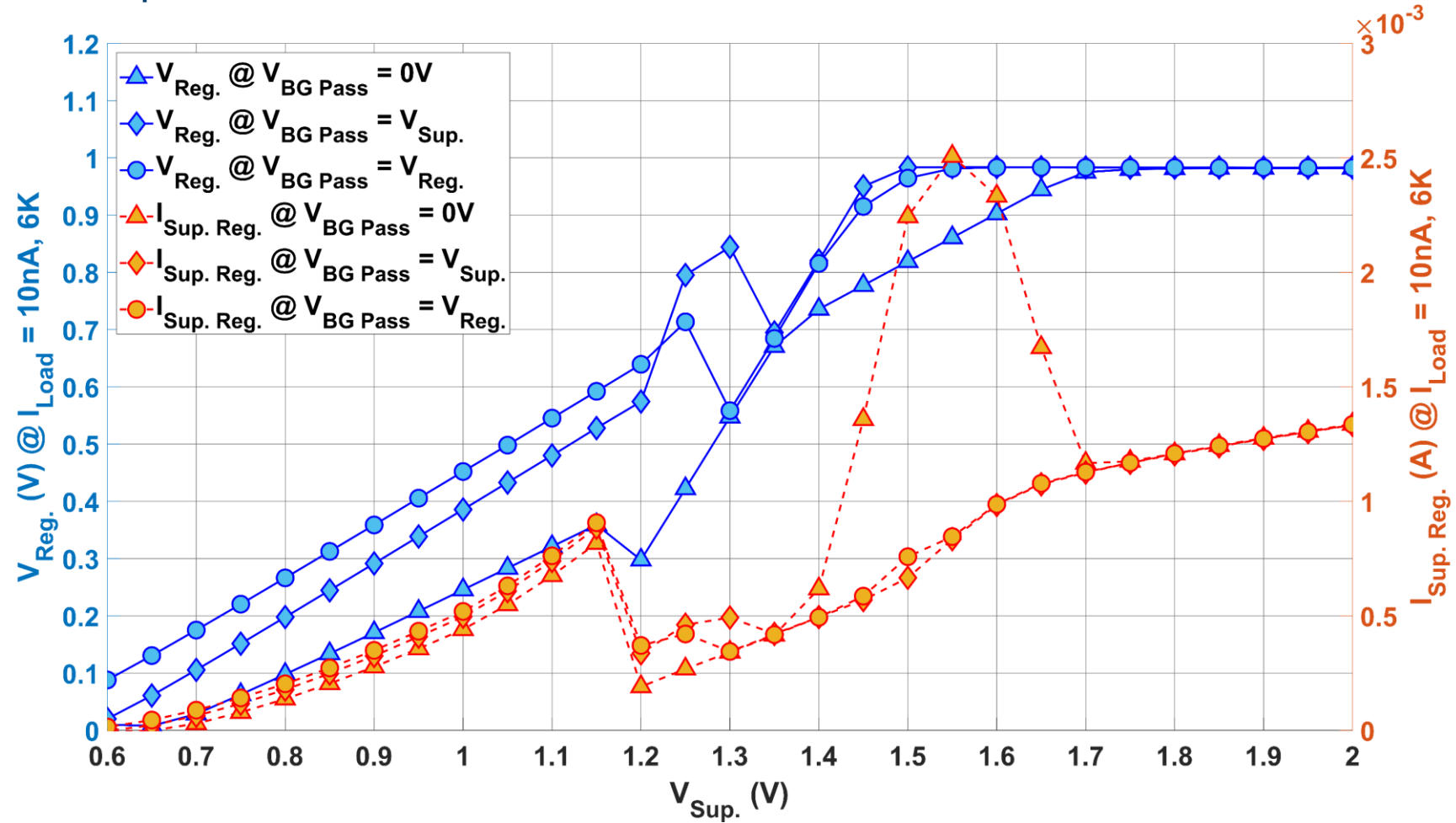
$$A_{LG} \approx A_{DA} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \quad (2)$$

$$LR \approx \frac{1}{g_{m_{M\,Pass}} \cdot A_{LG}} \quad (3)$$

$$PSRR \approx \frac{1}{g_{m_{M\,Pass}} \cdot r_{o_{M\,Pass}} \cdot A_{LG}} \quad (4)$$

BACKUP

$V_{\text{Reg.}}$ with respect to $V_{\text{Sup.}}$ at 6K



BACKUP

$V_{\text{Reg.}}$ PSRR at $V_{\text{Sup.}} = 2\text{V}$ and Temp. = 6K

