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Measurement-Free Fault-Tolerant Quantum Error Correction in Near-Term Devices

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Logical qubits can be protected from decoherence by performing quantum error-correction (QEC) cycles repeatedly. Algorithms for fault-tolerant QEC must be compiled to the specific hardware platform under consideration in order to practically realize a quantum memory that operates for in principle arbitrary long times. All circuit components must be assumed as noisy unless specific assumptions about the form of the noise are made. Modern QEC schemes are challenging to implement experimentally in physical architectures where in-sequence measurements and feed forward of classical information cannot be reliably executed fast enough or even at all. Here we provide a novel scheme to perform QEC cycles without the need of measuring qubits that is fully fault-tolerant with respect to all components used in the circuit. Our scheme can be used for any low-distance CSS code since its only requirement towards the underlying code is a transversal CNOT gate. Similarly to Steane-type EC, we coherently copy errors to a logical auxiliary qubit but then apply a coherent feedback operation from the auxiliary system to the logical data qubit. The logical auxiliary qubit is prepared fault tolerantly without measurements, too. We benchmark logical failure rates of the scheme in comparison to a flag-qubit-based EC cycle. We map out a parameter region where our scheme is feasible and estimate physical error rates necessary to achieve the break-even point of beneficial QEC with our scheme. We outline how our scheme could be implemented in ion traps and with neutral atoms in a tweezer array. For recently demonstrated capabilities of atom shuttling and native multiatom Rydberg gates, we achieve moderate circuit depths and beneficial performance of our scheme while not breaking fault tolerance. These results thereby enable practical fault-tolerant QEC in hardware architectures that do not support midcircuit measurements.

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I. INTRODUCTION

Implementation of quantum error-correction (QEC) routines into inevitably noisy physical hardware is conjectured to be indispensable in order to enable large-scale universal quantum computation [1]. If errors on the quantum register that holds the logical information can be corrected faster than they occur, the threshold theorem guarantees that the computation can be continued for in principle arbitrary long times [2,3]. Fault-tolerant (FT) quantum circuits come with a qubit, gate, or time overhead compared to non-FT circuits but can lead to lower logical failure rates provided the error rates of physical components are below a break-even point [4]. For a QEC code capable of correcting t errors, any possible combination of t Pauli faults on all components [5] of a quantum circuit can never lead to failure of the circuit in order for the protocol to be fully FT.

The ability to perform measurements is considered crucial to perform FT QEC. Several milestones towards error-corrected quantum computation have been achieved using FT circuit designs [6–15]. Repeated QEC cycles were realized in both ion traps [16] and superconducting transmons [17–19]. Recently, it was shown experimentally that increasing the size of the QEC code can suppress the logical failure rate in a surface-code experiment [20]. Neutral-atom platforms are catching up quickly. The preparation of logical states of the Steane, surface, and toric code has been demonstrated in an experiment with mobile atoms in optical tweezers [21]. Proposals for FT quantum computing have been put forward that take into account specific aspects of this physical platform such as enhanced leakage errors [22,23] and first experimental observations were made recently [24,25].

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Although most quantum computing hardware platforms are able to perform measurements of physical qubits, each have their own limitations that hinder straightforward application of QEC. In superconducting transmons, for example, error rates of measurements are typically larger than error rates of physical gates and measurement crosstalk can affect neighboring qubits [20]. In many hardware platforms, measurements are much slower than gate operations, leading to errors on qubits that are idling during measurement and feedback. In trapped-ion and neutral-atom platforms, this problem is exacerbated by the necessity of applying relatively slow laser recooling of ions after qubit detection [26] or laser cooling during detection to avoid atom loss [27]. In trapped ion systems, alternative routes explore using different ion species for sympathetic cooling [28,29] or physical shuttling of ions into dedicated readout zones separated from the rest of the system to avoid heating of a large ion crystal [13,30–32]. In neutral-atom platforms, midcircuit measurements have only recently been demonstrated [33–35]; however, they are still orders of magnitude slower than typical gate times on that platform. Real-time feedback based on measurements remains experimentally challenging but has been demonstrated lately [36,37]. Future experiments that involve in-sequence logic might require technologies such as cavity-enhanced fluorescence imaging [38,39], shuttling of atoms into dedicated readout zones [21], or the use of multiple atom species [40].

Because of these challenges, there has been continuous effort in finding QEC schemes that circumvent the need of measuring individual qubits to obtain information about potential errors while at the same time maintaining fault tolerance. Note that some dissipative element is still needed for QEC to remove entropy from the system; either by the ability to reset qubits or to have a sufficiently large reservoir of fresh qubits [41–43]. Autonomous quantum error-correction protocols make use of engineered dissipation in a non-FT way [44]. In bosonic codes it is common to engineer Lindbladians that have the code states as fixed points [45,46]. Measurement-free EC need not be substantially inferior than conventional QEC in principle [47,48]. A non-FT measurement-free surface-code implementation has been shown in Ref. [49]. Techniques to devise the T gate and the Toffoli gate fault tolerantly without measurements were given in Ref. [50]. In Ref. [51] a different measurement-free FT EC protocol was devised specific to the Bacon-Shor code while extendable to the class of Calderbank-Shor-Steane (CSS) codes. The authors proved a competitive threshold by means of concatenation for the nine-qubit Bacon-Shor code. QEC cycles can be implemented fault tolerantly given additional assumptions about the form of the noise [52,53]. However, devising *practical* measurement-free QEC schemes compatible with the number of qubits and native gate operations available in current quantum computers that incorporate full fault tolerance remains a challenging task.

In this paper we provide a QEC technique without measurements that is fully fault tolerant towards circuit-level depolarizing noise on all circuit locations, inspired by Steane-type EC. We note that now logical qubit operations, i.e., initialization, Clifford gates, and QEC cycles, can be implemented without the need of measurements and real-time feedback. In Sec. II we present our novel measurement-free FT QEC scheme, discuss resource requirements and compare the scheme to conventional flag-qubit-assisted QEC [54–57]. Our scheme needs auxiliary logical qubit states, which can be prepared fault tolerantly without measurements [58,59], as we show in Sec. III. In Sec. IV we provide protocols for practical implementations in state-of-the-art quantum hardware, via (a) decompositions into two-qubit gates, (b) native multiqubit-controlled gates that were proposed for neutral-atom or ion trap architectures and (c) multiqubit Mølmer-Sørensen (MS) gates native to ion-trap quantum processors. Contrary to general folklore, using all these multiqubit operations does not invalidate the FT property of the scheme if used at suitable positions in the QEC circuits. Moreover, we propose a shuttling schedule to implement the proposed scheme in a state-of-the-art neutral-atom quantum processor. We provide conclusions and an outlook on future work in Sec. V.

II. MEASUREMENT-FREE FT QEC CYCLE

Quantum error-correcting codes are based on so-called stabilizer operators, whose eigenvalues must be measured in order to determine and correct for potential errors that might have happened to the logical qubit that is encoded in such a code [60]. Two standard techniques to render QEC fault tolerant are Shor- and Steane-type EC [61,62]. The former verifies that a measured stabilizer expectation value is correct by fault tolerantly encoding the syndrome into the parity of an auxiliary preverified FT GHZ state. The readout procedure must be repeated until a majority vote determines the most likely value in order to protect against single measurement errors. With much fewer qubit and repetition overhead, the flag-qubit paradigm was shown to efficiently realize FT QEC cycles [54–56]. A small number of additional physical flag qubits act as heralds of errors that—with non-FT QEC—would lead to logical failure but can be corrected with flag-FT QEC. Measurement of syndrome and flag qubits is combined with classical processing and feedback conditioned on the in-sequence measurement information and, possibly, additional stabilizer measurements. This technique can be used in any QEC code. Steane-type EC, on the other hand, can be applied to the class of CSS quantum codes [63], which includes the well-known surface code [64,65] and two-dimensional color codes [66–69].

Steane-type EC sequentially corrects one type of Pauli error (first X then Z or vice versa) by mapping faults from the data qubit register to a logical auxiliary qubit in the state $|+\rangle_L$ or $|0\rangle_L$, respectively. It then uses appropriate logical measurements of the logical auxiliary qubits to infer the most likely error on the logical data qubit, which can then be corrected by conditioning the classical recovery operation on the measurement outcome of the logical auxiliary qubit.

We demonstrate that with sufficient qubit and gate overhead the need for measurements in Steane-type EC can be circumvented. In the following we first lay out our scheme for a general distance-3 CSS code and the $[\![7,1,3]\!]$ Steane code [70]—the smallest representative of the family of two-dimensional color codes [66–69]—explicitly. We then discuss resources needed for implementation. Lastly, we demonstrate in which parameter regime we can expect an advantage of the scheme over conventional syndrome-measurement-based QEC.

A. Scheme

We illustrate one measurement-free FT QEC cycle of our protocol with logical building blocks in Fig. 1. It requires three qubit registers: the first holds the logical data qubit formed of n physical qubits, which we aim to correct, in an arbitrary logical state $|\psi\rangle_L$, potentially having suffered from some fault. The second register of equal size is used to initialize a logical auxiliary qubit, analogous to Steane-type EC, in the state $|+\rangle_L$ ($|0\rangle_L$) when correcting $X(Z)$ errors. The third register contains a unencoded physical qubits which are all initialized to $|0\rangle$ ($|+\rangle$) when correcting $X(Z)$ errors. Our goal is to propagate faults, which are potentially present on the logical data qubit, through the circuit while at the same time preserving the logical qubit state during fault-free operation. In order to correct for X errors on the state $|\psi\rangle_L$, a transversal, i.e., bitwise, CNOT gate propagates them to the logical auxiliary qubit first as marked by the yellow block in Fig. 1. For two logical qubits both encoded in the same CSS code, bitwise application of physical CNOT gates between their physical data qubits implements the logical CNOT gate. Transversal gates are naturally fault tolerant since there are no couplings between two qubits of the same block. Thus, a single fault on one logical qubit or a physical CNOT gate can never propagate to an uncorrectable error on any logical qubit. Since $|+\rangle_L$ ($|0\rangle_L$) is the state on the target (control) of the logical CNOT when correcting $X(Z)$ errors, there is no backaction on the control (target) state where we hold $|\psi\rangle_L$. This way, one does not learn about the logical state itself since no expectation values of logical operators are mapped to the logical auxiliary qubit but only individual faults. Note that one cannot use n CNOT gates coupling the ancilla qubits in tensor product states $|0\rangle^{\otimes n}$ or $|+\rangle^{\otimes n}$ to the logical state to read out errors on the code state. Then follows a coherent syndrome mapping S from the second to the third register. The mapping can be done without special treatment to ensure fault tolerance, for example, preventing uncorrectable errors on the logical auxiliary qubit, since the second register is anyway reset (R) afterwards. As a last step, the syndrome is coherently copied (C) back from the third to the second register and the feedback operation F applies the correction on the data qubit in the first register that matches the syndrome. This last step needs to be repeated for all syndrome-correction pairs. Subsequently, the analogous procedure is applied to correct for Z errors with the previous X- and Z-type states and operations interchanged. An additional step of Hadamard gates on the a auxiliary qubits transforms the $|+\rangle$ states needed for the syndrome mapping to Z eigenstates for the controlled feedback operation.

As an illustrative application example, we demonstrate our scheme using the $[\![7,1,3]\!]$ Steane code. Our scheme is equally applicable to the distance-3 surface code [64,71], for which the treatment of single-qubit errors is analogous and we discuss the treatment of higher-weight errors in Appendix A. These two codes are the smallest instances of the leading approaches towards practical topological QEC.

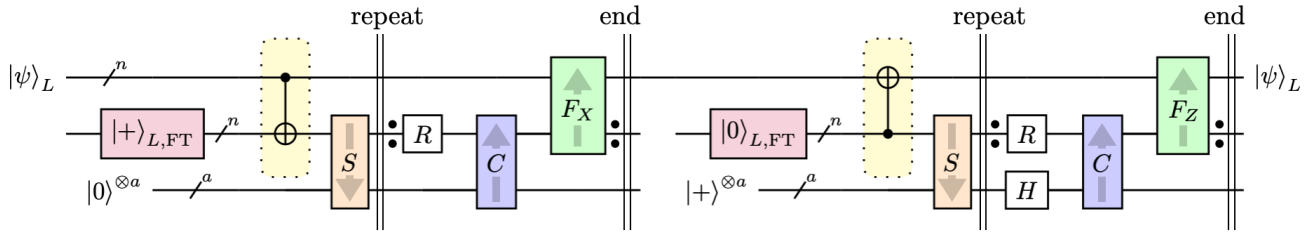

FIG. 1. Logical building blocks of the measurement-free fault-tolerant quantum error-correction cycle. Errors on the logical qubit $|\psi\rangle_L$ are copied to a logical auxiliary qubit initialized fault tolerantly in the appropriate basis. Then the a-bit syndrome is mapped from the logical auxiliary qubit (block S) to the second auxiliary block of a physical qubits. For each syndrome-correction pair, we repeatedly reset (R) the physical qubits to $|0\rangle$, copy (C) the syndrome and apply the matching feedback operation F_σ of Pauli type $\sigma \in \{X, Z\}$. The repetition refers to all $2^a - 1$ possible nontrivial syndromes. Instead of qubit reset, one may also supply fresh auxiliary qubits. The copy and feedback can be parallelized to avoid repetition and to reduce circuit depth and thereby the overall duration of the protocol if a larger number of physical auxiliary qubits is available (see Sec. II B).

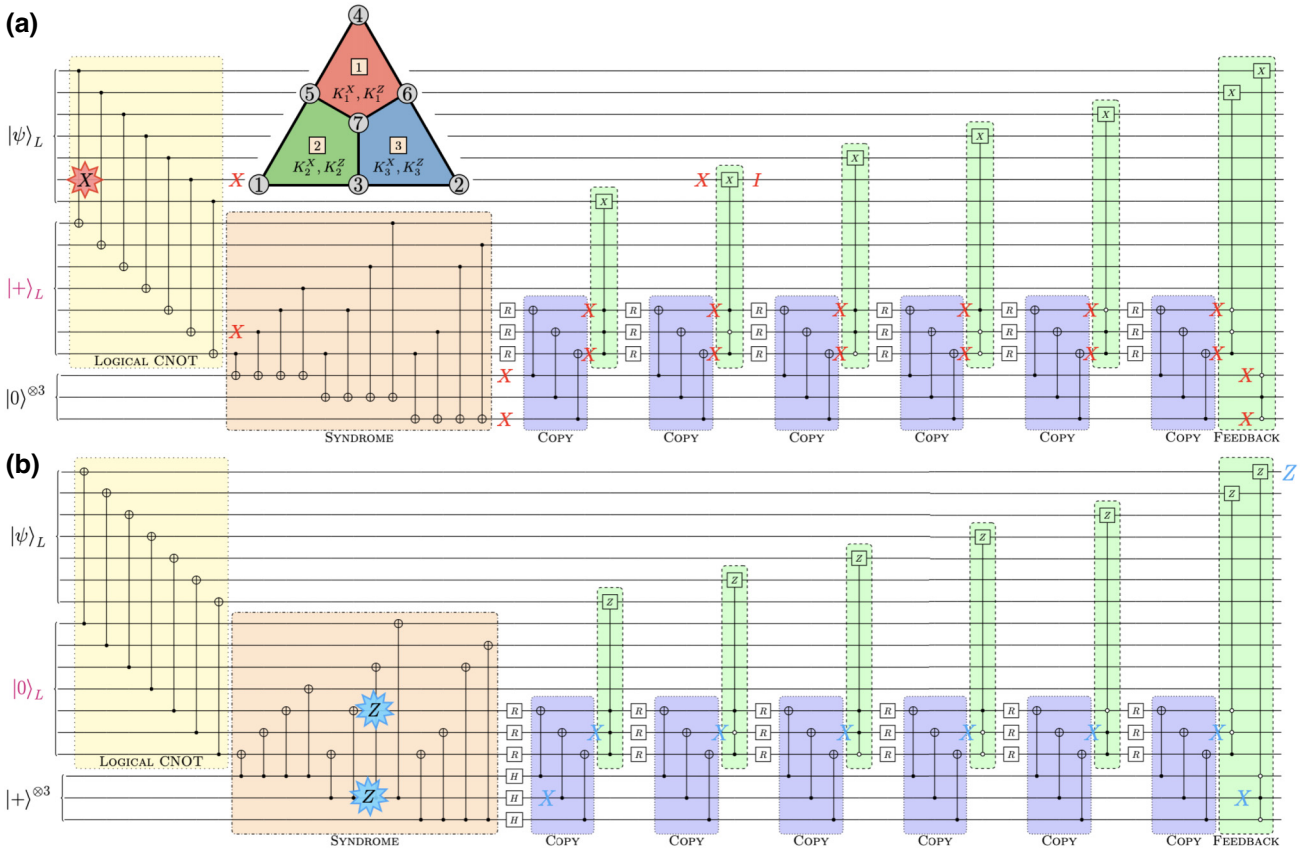

FIG. 2. Detailed circuit on the physical qubit level of the measurement-free fault-tolerant quantum error-correction cycle for the Steane code. The syndrome mapping (orange) does not require a distinctly FT routine because we perform intermediate reset operations R to the state $|0\rangle$ that erase potentially dangerous faults. The control qubits of the feedback gates (green) are conditioned on the physical qubits being in the $|1\rangle$ ($|0\rangle$) state for a black (white) circle. Any suitable procedure to prepare the logical auxiliary qubits fault tolerantly can be used. We provide a measurement-free FT initialization circuit in Fig. 6. For the last correction operation, copying from the third to the second block can be omitted. One can verify that no single error of any type on any circuit element will lead to an uncorrectable error. (a) X-correction block. A single bit-flip error on the logical data qubit, say X_6 (red star), is propagated to the logical auxiliary qubit. The sixth physical CNOT gate propagates the fault as illustrated by the two subsequent red X markers. For a Z fault, the propagation would happen reversely from the target to the control qubit of a CNOT gate. Propagation of Y faults can be viewed as simultaneous occurrence of X and Z faults. Then, the syndrome is mapped to three physical qubits and copied to all multiqubit-controlled feedback gates. The error is corrected by the second C_3NOT gate. For the first and all other C_3NOT gates the syndrome does not match the control structure. Thus, they have no additional effect on the logical data qubit. Note that, in contrast, for standard Steane-type EC, one would correct X_6 by measuring all qubits of the logical auxiliary qubit in the Z basis after the logical CNOT gate and applying the feedback conditioned on the measurement result. (b) Z-correction block. As required for an FT circuit, single faults within the auxiliary system can never cause more than a weight-1 error on the logical data qubit. As an example, we show the single fault event $Z_{12}Z_{16}$ (blue stars), which propagates to a correctable weight-1 error on the logical data qubit through the last C_3Z gate.

For the surface code, FT state preparation has recently been realized without measurements in Ref. [59]. The Steane code allows one to encode $k = 1$ logical qubit in the code space as defined as the joint +1 eigenspace of the six stabilizer generators

$$\begin{aligned} K_1^X &= X_4X_5X_6X_7 \quad K_1^Z = Z_4Z_5Z_6Z_7 \\ K_2^X &= X_1X_3X_5X_7 \quad K_2^Z = Z_1Z_3Z_5Z_7 \\ K_3^X &= X_2X_3X_6X_7 \quad K_3^Z = Z_2Z_3Z_6Z_7 \end{aligned} \tag{1}$$

on $n = 7$ physical qubits as shown as part of Fig. 2(a). The logical operators of the Steane code can be chosen as $X_L = X^{\otimes 7}$ and $Z_L = Z^{\otimes 7}$. The Steane code can correct $t = 1$ arbitrary Pauli error and thus has distance $d = 3$. For a logical measurement after the QEC cycle, all physical qubits can be measured transversally (and thus fault tolerantly).

The detailed circuits are depicted on the physical qubit level in Fig. 2. Here we remark that each data qubit correction is conditioned on its distinct three-bit syndrome, which is encoded into the control pattern of the C_3NOT

(or C_3Z) gates that perform the corrections. Since the repetition for each data qubit correction starts by resetting the second register, the syndrome information can be copied anew from the third register using—in this example—$a = (n-k)/2 = 3$ transversal CNOT gates without breaking fault tolerance. The feedback operations are quasitransversal in the sense that a distinct syndrome is uniquely connected to a single physical data qubit. Due to the reset operations there is no connection between the individual syndromes. Consider, for example, the error X_6 in Fig. 2(a). It will be mapped to the three-qubit state $|101\rangle$ in the third register and, as a consequence, only the second C_3NOT gate with the 101-control structure will act nontrivially on the logical data qubit and correct the error. As long as only a single fault occurs on the second or third register, at most one (potentially erroneous) correction operator is applied to the first block. The input state $|\psi\rangle_L$ is assumed fault free when a fault happens within the cycle because the scheme is FT towards a single fault only. This resulting single error on $|\psi\rangle_L$ will always be correctable by the QEC code. If $|\psi\rangle_L$ already carries a single error, it is guaranteed by the then fault-free QEC cycle that the correct syndrome is mapped to the third register and the appropriate correction is applied. Two faults are necessary to cause failure of the protocol but a single fault can never cause failure because of fault tolerance. Assuming a physical fault rate p, the probability of failure is of order p^2 while for a non-FT protocol the probability of failure is of order p.

Note that we required only that transversal CNOT operations between the first and second block (to propagate the errors) as well as between the second and third block (to coherently copy the syndrome) are available. The FT auxiliary qubit initialization, syndrome mapping, and feedback can be implemented with any routine that is most suitable for the particular hardware under consideration. Possible implementations into a neutral-atom tweezer array and an ion trap are sketched in Fig. 3, which we elaborate in more detail in Sec. IV.

B. Resources

The scheme as presented in Fig. 2 requires $2n$ physical qubits for the two logical qubits and a qubits to store the syndrome of one Pauli type. In total, $N = 2n + a = \mathcal{O}(n)$ physical qubits are needed for an $[\![n, k = 1, d = 3]\!]$ CSS code. If the X and Z syndromes have the same length, as for color codes or surface codes, we can take the number of syndrome qubits to be $a = (n-k)/2$. Note that some additional physical qubits might be required for the FT initialization of the logical auxiliary qubits depending on the specific code under consideration. The time overhead that is needed in order to perform the $2^a - 1$ feedback operations can be transformed into a qubit overhead, which is useful, e.g., if the cycle time would be too long to implement the repeated copy steps or when no reset operation is available. Instead of repeatedly applying resets we can coherently copy the syndrome $2^a - 2$ times to fresh auxiliary qubits. In this case the total number of qubits would increase to $N' = 2n + a\,(2^a - 1) = \mathcal{O}[2^{(n/2)}]$ because we still need two logical qubits using n physical qubits each but then we also need $2^a - 1$ blocks of a qubits each to connect each feedback operation to a distinct syndrome block.

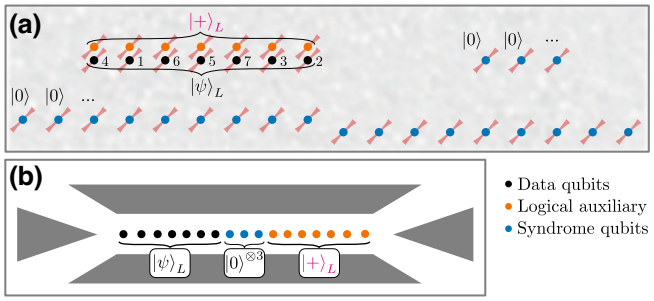

FIG. 3. Sketched embedding of the scheme for the Steane code into (a) a neutral-atom tweezer array and (b) a static linear ion trap. For the tweezer array, we show a proposed initial configuration of the atoms. Entangling gates can by applied in parallel to atoms at close range. Between the application of entangling gates, atoms are shuttled to new locations, which we outline in more detail in Fig. 11.

Let us now count the number of CNOT gates that are needed to implement one QEC cycle, assuming for simplicity that the X-correction block and the Z-correction block are symmetric and thus require the same number of CNOT gates. Each logical CNOT gate amounts to n physical CNOTs. Then, $a \times s$ CNOTs are needed for the syndrome mapping step where we assume, for simplicity, that all stabilizers have the same weight s, i.e., the number of physical qubits that the stabilizers act nontrivially on. Coherently copying the syndrome $2^a - 2$ times requires a bitwise CNOT gates each. We need $m = 2^{a+1} - 3$ two-qubit gates to exactly decompose a single a-qubit-controlled feedback operation targeting a single physical data qubit [72]. For all $2^a - 1$ feedback operations we need m CNOT gates each. Therefore, in total, we require at most $2 \times (n + a(s + 2^a - 2) + m\,(2^a - 1))$ CNOT gates to implement the QEC cycle.

It is desirable to reduce the circuit depth of the QEC cycle as much as possible due to the limited coherence times in near-term devices. If CNOT gates can be executed in parallel, the transversal CNOT gate can be run in just one time step, the stabilizer readout needs s time steps (again assuming all stabilizers have the same weight) and copying the syndrome from one block to $2^a - 1$ blocks can be done in a time steps. All feedback operations can in principle be executed in a single time step if the physical architecture permits.

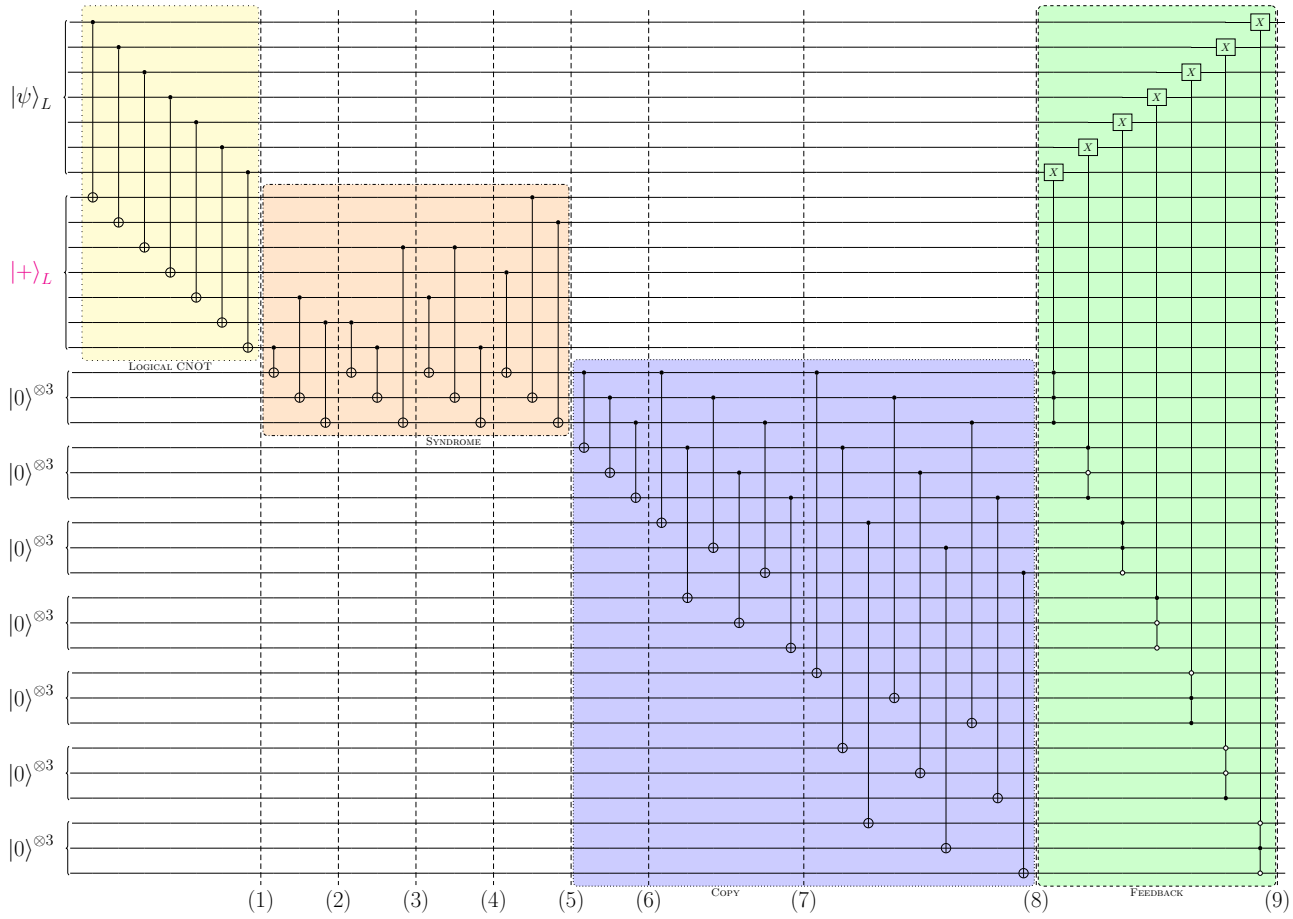

FIG. 4. The X-correction block of the measurement-free FT QEC scheme can be scheduled in nine time steps (dashed vertical lines) when parallel gate operations and $N' = 2 \times 7 + 3 \times (2^3 - 1) = 35$ physical qubits are available. In the first step, the logical CNOT is applied. Then, from time step 2 to 5, the syndrome is mapped to a fresh set of auxiliary qubits. From time step 6 to 8, the syndrome is copied 6 times. In the last time step, the seven feedback operations are applied. It is possible to parallelize the Z-correction block analogously.

For the Steane code, these requirements amount to a total of 256 CNOT gates with $n = 7$ physical qubits, $a = 3$ stabilizers of each type that have weight $s = 4$. We elaborate a simplification of the multiqubit-controlled gate decomposition in Sec. IV and Appendix B that will allow one to reduce m from 13 to 8 (from $2^{(a+1)} - 3$ to 2^a in general) and thus realize the Steane code QEC cycle with 186 CNOT gates. We note that the large number of CNOT gates mainly originates from the decomposition of multiqubit-controlled gates into two-qubit gates. If these gates can be performed natively, one counts 88 two- and multiqubit gates. The measurement-based quantum error-correction scheme for comparison requires up to 52 CNOT gates, which is shown in Appendix F. In total, the minimum circuit depth that can be achieved with the Steane code is $2 \times 9 = 18$ as shown in Fig. 4. Note that furthermore the X- and Z-type correction part of the QEC cycle [see Figs. 2(a) and 2(b)] could also be largely carried out in parallel if one disposes of two simultaneously operated logical auxiliary logical qubits and registers of additional bare physical qubits.

Let us remark that the a physical auxiliary qubits are not strictly necessary to map the syndrome from the logical auxiliary qubit. Instead one may use an appropriate decoding circuit to obtain the syndrome on a subset of the physical qubits forming the logical auxiliary qubit and perform the quantum feedback as we discuss in more detail in Appendix C.

C. Measurement-free advantage

In the following, we analyze under which conditions the measurement-free (MF) EC protocol can be expected to yield lower logical failure rates than conventional EC involving syndrome measurements (SMs). We provide an analytical estimation for advantageous use of the MFEC scheme and compare it to numerical state-vector simulations.

We assume that all operations, i.e., gates, qubit initializations, and measurements, in the circuits of the protocol, compiled into CNOT gates, are prone to depolarizing noise of strength p (see Appendix D for details on the noise model). Also, we consider an idling error rate $p_{\text{idle},m}$ for idling during measurements for the measurement-based protocol and an idling error rate $p_{\text{idle,op}}$ for idling during operations for the MFEC protocol. These are the two dominant sources of idling noise for both protocols, assuming that the time to perform a qubit measurement is much longer than the time to perform a gate operation or qubit initialization or reset. The finite duration t of physical operations causes an idling time on those qubits that are not targeted by these operations. The idling error rate for a qubit with coherence time T_2 that is prone to pure Markovian dephasing during an idling time t is

$$p_{\text{idle}} = \frac{1}{2}\left(1 - \exp\left(-\frac{t}{T_2}\right)\right). \tag{2}$$

The rate p_{idle} is linearly proportional to the idling time t if $t/T_2 \ll 1$.

Denoting the logical failure rates of the two protocols p_L^{MF} and p_L^{SM} respectively, MFEC is advantageous when the ratio of the failure rates $p_L^{\text{MF}}/p_L^{\text{SM}} \leq 1$. We estimate in Appendix E that the MFEC protocol is advantageous when the ratio of measurement to operation time fulfills the inequality

$$\frac{t_{\text{meas}}}{t_{\text{ops}}} \geq \sqrt{\frac{\tilde{c}^2}{\tilde{c}'^2} + \frac{c\tilde{c}}{\tilde{c}'^2}\frac{p}{p_{\text{idle,op}}} + \frac{c^2}{\tilde{c}'^2}\frac{p^2}{p_{\text{idle,op}}^2}}. \tag{3}$$

Here, c ($\tilde{c}$) is the number of operations (idling locations) in the MFEC circuit and $\tilde{c}'$ is the number of idling locations during measurements in the conventional EC protocol.

As an example of a measurement-based protocol, we choose a state-of-the-art flag-qubit-based EC protocol [57], described in Appendix F. We pick a set of noise parameters, which satisfies Eq. (3) with a large margin, given the constants for the flag EC circuits in Eqs. (E13)–(E16), as

$$p = 5 \times 10^{-4} \tag{4}$$

$$p_{\text{idle,op}} = 10^{-4} \overset{T_2 = 10^{-2}\,\text{s}}{\Longleftrightarrow} t_{\text{ops}} = 2 \times 10^{-6}\,\text{s} \tag{5}$$

$$p_{\text{idle},m} = 6.5 \times 10^{-2} \Longleftrightarrow t_{\text{meas}} = 1.4 \times 10^{-3}\,\text{s}. \tag{6}$$

For these parameters we find via Monte Carlo simulation that MFEC achieves a logical failure rate of $p_L^{\text{MF}} = (3.44 \pm 0.25)\%$ when compiled into CNOT gates while flag EC fails for $p_L^{\text{FL}} = (3.96 \pm 0.26)\%$ of the runs. The numerical data in Fig. 5 is obtained by sampling logical failure rates of both schemes in Monte Carlo simulation until the uncertainty intervals of the two estimators allow one to distinguish which of the two schemes is advantageous.

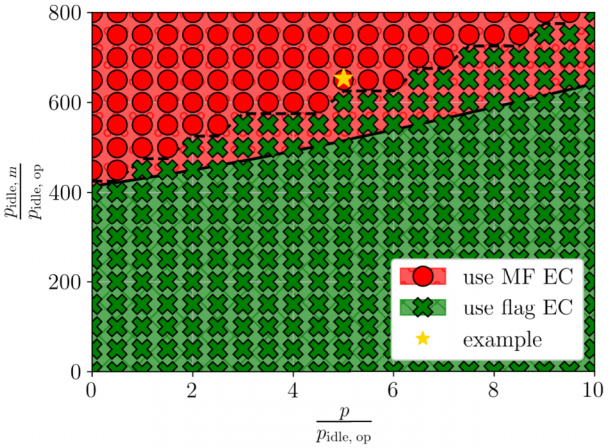

FIG. 5. Utility diagram for measurement-free (MF) EC and flag EC. Regions of advantage based on numerical simulation (markers) and the estimation in Eq. (3) (filled area) are shown in terms of the parameter ratios $p/p_{\text{idle,op}}$ and $p_{\text{idle},m}/p_{\text{idle,op}}$, which approximates $t_{\text{meas}}/t_{\text{ops}}$, with $\tilde{c}^2/\tilde{c}'^2 = 171\,041$, $c\tilde{c}/\tilde{c}'^2 = 13\,471$ and $c^2/\tilde{c}'^2 = 1061$ in accordance with Eqs. (E13)–(E16). The lines mark the estimated boundaries between regions of advantage. In the limit of vanishing operation errors, $p = 0$, MFEC yields an advantage over flag EC if measurements are at least 400 times slower than operations. The star marker represents the parameters given in Eqs. (4)–(6). At $p/p_{\text{idle,op}} = 1$ and $p_{\text{idle},m}/p_{\text{idle,op}} = 1$, we use absolute values of $p = p_{\text{idle},m} = p_{\text{idle,op}} = 10^{-4}$ in the numerical simulations.

While gate error rates of $p = 5 \times 10^{-4}$ are experimentally demanding, we stress that our scheme offers the possibility to perform FT QEC in physical systems that currently cannot support the measurement duration necessary for conventional QEC schemes.

III. DETERMINISTIC FT LOGICAL STATE PREPARATION

Our MFEC scheme needs logical auxiliary qubits whose encoding must be FT in order to render the full scheme FT. In this section we describe how to fault tolerantly initialize the logical auxiliary qubit (and also the logical data qubit) without measurements. This way, our FTEC scheme can be performed in a fully measurement-free setting. Let us remark nevertheless that the measurement-based encoding protocol from Ref. [73] has been realized recently in ion-trap platforms [12,14,16].

In Ref. [58] some of us suggest an extension of the prescription for logical qubit initialization in Ref. [73] by making use of the flag-qubit information instead of discarding the state. The circuit for measurement-free FT initialization to $|0\rangle_L$ is shown in Fig. 6. By mapping the two eigenvalues of both the logical operator $Z_3Z_5Z_6$ (red block, "flag") and the complementary stabilizer $Z_1Z_2Z_4Z_7$ (orange block, "stabilizer") to two auxiliary qubits, all dangerous

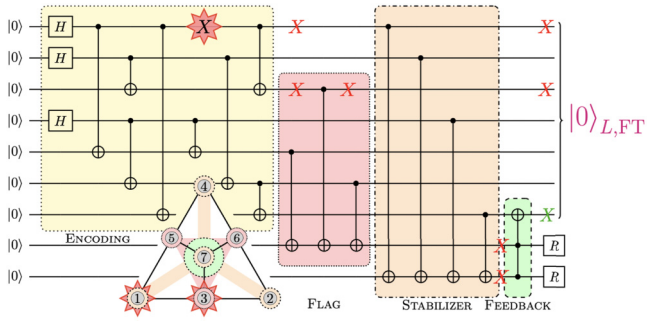

FIG. 6. Circuit to fault tolerantly initialize the logical zero state of the Steane code without measurements. The first eight CNOT gates prepare the state non-fault-tolerantly. The subsequent three CNOT gates map the logical operator $Z_3Z_5Z_6$ to a flag qubit that heralds successful preparation (red dotted circles on code graph). The last four CNOT gates map the complementary stabilizer $Z_1Z_2Z_4Z_7$ (orange dashed circles on code graph) to a second auxiliary qubit. Only if both measurements yield the -1 eigenvalue, the correction X_7 is applied via the Toffoli gate (large green circle on code graph). In the end, both auxiliary qubits are reset (R). The dangerous fault X_1 after the fourth CNOT gate (red star) propagates to both auxiliary qubits and triggers the Toffoli feedback (green box). The resulting operator $X_1X_3X_7$ is stabilizer equivalent to the correctable error X_5 via application of K_2^X.

weight-2 errors at the end of the circuit can be transformed into correctable errors.

In fact, there are only two dangerous errors, namely X_1X_3 and X_4X_5 (X_6X_7 is stabilizer equivalent to X_4X_5 via application of K_1^X), which flip the first auxiliary qubit from $|0\rangle$ to $|1\rangle$ since their support has odd overlap with $Z_3Z_5Z_6$. Of course, X_1X_3 and X_4X_5 also have odd overlap with the qubits that take part in the subsequent stabilizer mapping step so the second auxiliary qubit is also flipped from $|0\rangle$ to $|1\rangle$. The dangerous errors will lead to both auxiliary qubits being in the $|1\rangle$ state. Correctable weight-1 errors only flip one of the two from $|0\rangle$ to $|1\rangle$. No single fault during the mapping of either Z operator can result in the auxiliary qubits being in the state $|11\rangle$. The operator X_7 is applied coherently via the Toffoli gate if both the flag qubit and the extra stabilizer qubit are in the $|1\rangle$ state (green block, "feedback"). This way, any dangerous weight-2 error will be transformed into a correctable weight-1 error by multiplication with X_7. Treatment of the X_1X_3 error is sketched as an example in Fig. 6.

The auxiliary qubit state before applying the Toffoli gate can only be different from $|00\rangle$ if a fault has happened at some circuit location before. An additional fault during the Toffoli gate would render the total fault configuration to be of order p^2. If instead the circuit up to the Toffoli gate has been fault free and the $t = 1$ fault now occurs within the Toffoli gate with probability p, it can at most propagate to a correctable error since the Toffoli is only connected to a single data qubit.

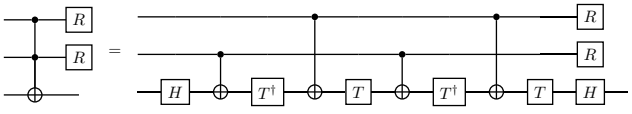

FIG. 7. Decomposition of the Toffoli gate followed by reset of the control qubits into Hadamard gates H, the standard T, $T^\dagger$, and CNOT gates as well as reset R.

The Toffoli gate can be decomposed into a sequence of single- and two-qubit gates [74]. Since the auxiliary qubit state is discarded at the end of the circuit anyway, we can modify the well-known decomposition into six CNOT gates from Ref. [60]. Figure 7 shows the decomposition of the Toffoli gate followed by reset into only four CNOT gates.

In summary, since the state preparation scheme can be performed without qubit measurements, it qualifies to prepare logical auxiliary qubits and thereby completes our measurement-free FT QEC scheme.

IV. PRACTICAL IMPLEMENTATION

The suggested measurement-free fault-tolerant quantum error-correction protocol can be implemented using various sets of basis gates that are native to different quantum computing platforms. In the following, we provide compilations of our 17-qubit scheme (Fig. 2) into CNOT gates, native multiqubit-controlled gates as well as multiqubit Mølmer-Sørensen gates. The latter are widely used entangling gates in trapped-ion systems [75].

If native multiqubit gates are practically available and if their physical error rates are lower than the expected overall error of their decompositions, they are preferential to implement the feedback operation (green boxes in Fig. 2) over a gate decomposition into single- and two-qubit gates in order to minimize circuit depth. For the syndrome mapping step (orange boxes in Fig. 2), multiqubit gates can still be used to decrease the gate count. It is crucial that the transversal CNOT gates used for fault propagation (yellow boxes in Fig. 2) cannot be replaced by multiqubit gates. These would destroy the FT property of the scheme under a general error channel [see Eq. (D1)] since single faults could result in higher-weight errors that are uncorrectable in the Steane code.

To be truly fault tolerant, every qubit operation used in an actual implementation acting on a respective qubit state ρ must be assumed to be prone to noise. Here we employ the standard depolarizing noise model (see Appendix D for details) with different noise strengths than in Sec. II C: For the decomposition into two-qubit gates, we show simulations for a single-parameter depolarizing noise model with noise strength p on operations. On idling locations, we choose a corresponding noise strength $p/100$, which is the order of magnitude reached for two-qubit entangling gates in state-of-the-art ion trap systems [76]. This

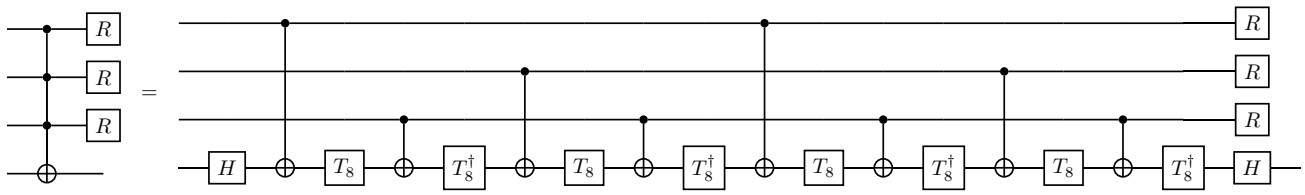

FIG. 8. Decomposition of a triple-controlled-NOT gate followed by reset R of the control qubits into a sequence of Hadamard gates (H), CNOT gates, and $T_8 = \exp(-i(\pi/16)Z)$ gates followed by reset R of the control qubits.

model has been assumed before for simulation of QEC blocks [55,77]. For the decompositions into multiqubit gates, we use a multiparameter noise model with different noise strengths $\vec{p} = (p_1, p_2, \ldots)$ for the respective multiqubit depolarizing channel [see Eq. (D1)] on operations. The parameters are based on values that either can be achieved experimentally in quantum processors already [16,76] or are based on theory proposals [78–81]. Since dephasing is the dominant source of noise on idling qubits in atomic architectures, we make use of the dephasing channel [see Eq. (D2)] with noise strengths assumed to be $\vec{p}/100$ for simplicity [82] on the respective idling locations for the multiparameter noise model. To assess the break-even point where $p_L = p_2$, we scale all physical error rates uniformly with a scaling parameter λ like

$$(p_1, p_2, \ldots) \to \lambda \cdot (p_1, p_2, \ldots). \tag{7}$$

Numerical state-vector simulations of these noisy circuits are performed with a modified version of the python package PECOS [83,84].

A. Decomposition in two-qubit gates

A large extent of the scheme is already expressed in terms of CNOT gates. The only components left to decompose are the multiqubit-controlled feedback gates C_3NOT and C_3Z. The authors of Ref. [72] state that 13 two-qubit gates are necessary to exactly decompose the full gate. However, since the state of the control qubits is reset after the gate anyway, decomposition is possible with fewer CNOT gates. Figure 8 shows the circuit equivalence of C_3NOT and a sequence of eight CNOT gates and standard single-qubit rotations when the state of the three control qubits after the gate is irrelevant. Alternating rotations of angle $\pm\pi/8$ cancel each other exactly if the control qubit state is different from $|111\rangle$. Only if all CNOT gates are activated, the intermediate X flips make the eight Z rotations align in order to realize a full $X(\pi)$ rotation in combination with the outermost Hadamard gates on the target qubit.

In Fig. 9 we compare the logical failure rate of the MFEC scheme with CNOT gates to the conventional flag EC from Sec. II C. Quadratic scaling behavior $p_L \sim p^2$ as $p \to 0$ for both logical input states $|0\rangle_L$ and $|+\rangle_L$ is clearly visible in Fig. 9. This is expected for the two FT schemes since there exist no single fault events that occur with probability p and contribute to the logical failure rate p_L. Our MFEC scheme achieves logical failure rates p_L approximately one order of magnitude larger than the flag scheme for a given physical error rate p.

To narrow the gap between the two schemes and achieve lower logical failure rates with the MFEC scheme, we now look into possible improvements using multiqubit gates.

B. Use of multiqubit gates

Depending on the physical architecture under consideration, specific multiqubit gates might be available for practical operation of the scheme. In neutral-atom platforms, the Rydberg blockade can be utilized to perform native multiqubit gates. CCZ gates that require only global laser pulses have already been realized in experiments

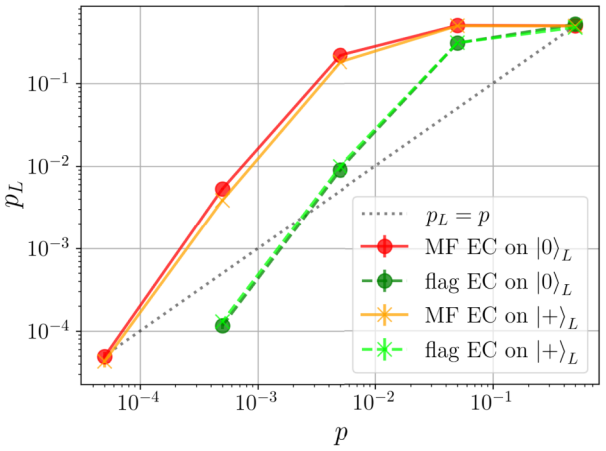

FIG. 9. Logical failure rates for the measurement-free (MF) EC scheme compared to conventional flag EC for two logical input states $|0\rangle_L$ and $|+\rangle_L$ with a single-parameter depolarizing noise model of strength p. The MFEC scheme is compiled into CNOT gates. Threshold values for outperforming the physical error rate $p_L = p$ lie at approximately $p = 3 \times 10^{-3}$ for the flag scheme and $p = 6 \times 10^{-5}$ for the measurement-free scheme, which is a factor of 50 smaller. This is due to the more complicated circuitry, however, the simple single-parameter noise model yields an overly pessimistic estimate for the threshold of the MFEC scheme, as shown in Fig. 10.

TABLE I. List of physical error rates (all in %) used for simulation of three different gate implementations at scaling parameter $\lambda = 1$. The error rates for idling positions during an operation are assumed to be 1% of the respective operation's error rate. Multiqubit gate error rates (p_3, p_4, p_5) are based on theory proposals [78–81] while single-qubit operation (p_1, p_i, p_m) and two-qubit gate error rates (p_2) are state-of-the-art values [16].

Impl.	p_1 [%]	p_2	p_3	p_4	p_5	p_i	p_m	p_{idle}
CNOT	0.007	0.3	...	...	...	0.0002	0.3	$p/100$
NATF	0.007	0.3	1	1	1	0.0002	0.3	$p/100$
MIMS	0.007	0.3	1	1	1	0.0002	0.3	$p/100$

[85,86]. Moreover, there are multiple theoretical proposals to implement, e.g., C_nNOT gates [81,86–88], CNOT$_n$ gates [88,89], or C_nNOT$_m$ gates [90], up to single-qubit rotations. In ion traps the *iToffoli* gate with varying number of control qubits can be implemented directly [80,91]. Additionally, one can realize multi-ion MS gates in these systems [43,75]. Also in superconducting architectures there are proposals and demonstrated implementations of native *iToffoli* [92,93] and CCPHASE gates [94].

In the following we provide decompositions and numerical simulations of the MFEC scheme using different sets of multiqubit gates where possible. Logical failure rates of these compilations are compared via numerical simulation to the scheme that uses only CNOT gates.

1. Native multiqubit-controlled feedback in neutral-atom platforms

We now describe the usage of native C_3NOT gates for feedback operations (green boxes in Fig. 2). With the large fidelities and fast gate times of such gates (see Table I and Refs. [78–81]) an improvement of logical failure rate can be expected over a decomposition into two-qubit gates, also due to the reduction of idling locations. From inspection of Fig. 8 we notice that due to the reset operations only the target qubit can cause erroneous output of the multiqubit-controlled feedback gate. In this decomposed version, eight two-qubit gate locations and ten single-qubit gate locations can cause an error in first order in p. We thus estimate that using a native multiqubit-controlled feedback gate to be advantageous over the decomposition as long as $p_4 < 8p_2 + 10p_1$ at least, which is fulfilled for the parameters in Table I.

2. Coherent syndrome mapping and quantum feedback in ion traps

The 17-qubit scheme for the Steane code from Fig. 2 can be embedded into a trapped-ion quantum processor, as sketched in Fig. 3(b), hosting a static one-dimensional ion crystal as in Ref. [26]. In these systems, the native entangling gate can be implemented by a laser-driven X-type MS gate described by the unitary

$$U_q(\theta) = \exp\left(-\mathrm{i}\frac{\theta}{4}\left(\sum_{k=1}^{q} X_k\right)^2\right) \tag{8}$$

targeting q ions simultaneously [75,95]. Such multiqubit MS gates can be used for the syndrome mapping (orange boxes in Fig. 2) and feedback steps [42,96]. Previously it has been found by exhaustive count of gate combinations in Ref. [97] that the Toffoli gate is equivalent to a sequence of local rotations and three-qubit MS gates (reproduced in Fig. 17 of Appendix G), which we do not improve further for use in our QEC scheme. An application of five-qubit MS gates for mapping the expectation value of a weight-4 stabilizer to a single auxiliary qubit has been given in Refs. [78,96] (see Appendix G for an example in Fig. 18). Six five-qubit MS gates are needed to map the syndrome to the physical auxiliary qubits. Recall that high-weight Pauli faults that are generated by the depolarizing noise channel of the five-qubit MS gate do not break fault tolerance since they act only on the logical auxiliary qubit, which is reset after syndrome mapping.

Using a variational circuit ansatz in pennylane [98], we found a decomposition of the C_3NOT gate followed by reset of the control qubits into four four-qubit MS gates that we depict in Fig. 19. The remaining CNOT gates are compiled into two-qubit MS gates and local rotations using Eq. (G1).

Figure 10 shows logical failure rates for all three previously described implementations for MFEC for both logical Steane code input states $|0\rangle_L$ and $|+\rangle_L$. Notably, all implementations are capable of achieving logical failure rates $p_L < p_2$ lower than the two-qubit error rate with improvements of the scaling factor λ of approximately one order of magnitude. For low physical error rates, where the six lines in Fig. 10 are (almost) parallel, native multiqubit-controlled feedback operations yield approximately a factor 5 of improvement over the CNOT compilation of the scheme. Multi-ion MS gates perform approximately a factor of 2 worse than the CNOT version in this regime [99].

C. Implementation with neutral atoms

As mentioned above, measurements in neutral-atom platforms are slow as compared to gates and it is challenging to perform measurements without atom loss and with real-time feedback. While multiqubit gates can be performed within roughly 100–500ns [85,86,100,101], recently demonstrated midcircuit measurements in free space take 3.5–25ms [33–36]. Such values correspond to ratios t_{meas}/t_{ops} between 7×10^3 and 2.5×10^5.

With a coherence time of $T_2^* = 4$ms, we estimate the logical failure rate of MFEC using native multiqubit-controlled feedback gates via numerical simulation to be

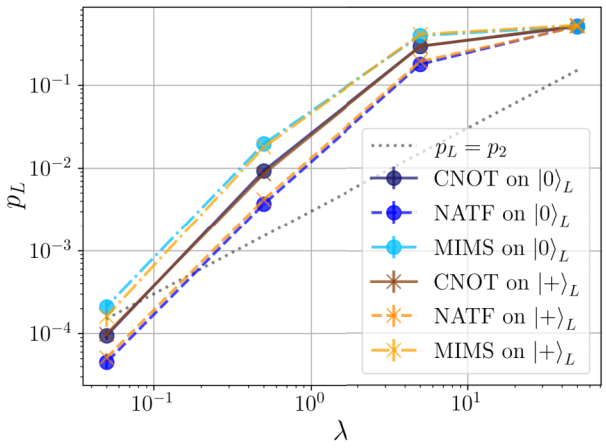

FIG. 10. Logical failure rates for the measurement-free scheme acting on both logical input states $|0\rangle_L$ and $|+\rangle_L$ with multiparameter noise and a scaling parameter λ that uniformly varies all physical error rates. Compilation of the scheme into CNOT gates is compared to implementations using native multiqubit-controlled feedback operations (NATF) and multi-ion Mølmer-Sørensen gates (MIMS) where applicable. Respective physical error rates are listed in Table I, $\lambda = 1$ corresponds to a two-qubit error rate $p_2 = 3 \times 10^{-3}$. Depending on the implementation, logical failure rates can vary to up to one order of magnitude. The thresholds for NATF and CNOT implementations correspond to two-qubit error rates of approx. 6×10^{-4} and 2×10^{-4}, respectively. For measurement-based QEC, the threshold lies at approx. 3×10^{-3} (see Fig. 9), being a factor 5 to 15 higher than in the measurement-free case.

$p_L^{\mathrm{MF}} = (5.9 \pm 0.3)\%$. With measurement times of approximately $t_{\mathrm{meas}} \in \{500\mu\mathrm{s}, 1\mathrm{ms}\}$, flag EC achieves respective logical failure rates of $p_L^{\mathrm{FL}} \in \{(4.9 \pm 0.2)\%, (11.8 \pm 0.4)\%\}$. Assuming an anticipated improvement of future operation error rates p_1, p_2, p_3, p_4, and p_{i} by a factor of 2, the logical failure rate of MFEC drops to $p_L^{\mathrm{MF}} = (1.7 \pm 0.1)\%$, i.e., by about a factor of 4, in agreement with the expectations for an FT protocol.

Using the substantially longer coherence time $T_2 = 1\mathrm{s}$, which can be achieved by involving spin-echo techniques, the failure rate of MFEC is reduced only slightly to $p_L^{\mathrm{MF}} = (5.6 \pm 0.1)\%$. This can be understood because the performance of the MFEC protocol is in this parameter regime not limited by its overall duration, but operational error rates. In contrast, the performance of the flag EC protocol improves more strongly, with the scheme benefiting more from an extended coherence time, resulting in a logical failure rate of $p_L^{\mathrm{FL}} = (0.66 \pm 0.04)\%$ for a measurement time $t_{\mathrm{meas}} = 1\mathrm{ms}$. Improving the operation error rates by a factor of 2 yields a predicted MFEC logical failure rate of $p_L^{\mathrm{MF}} = (1.7 \pm 0.1)\%$. The simulated [102] failure rates are summarized in Table II.

Our proposed scheme might thus open a competitive pathway for this platform to achieve beneficial FT QEC before fast in-sequence measurements and in-sequence logic will become widely available. Although leakage out of the computational subspace is a dominant error source in neutral-atom platforms, such errors can be handled either by converting them into Pauli Z errors [22] or erasures [23]. To execute the quantum circuits presented in this work, a certain connectivity between qubits is required. In a static array of atoms with nearest-neighbor or even next-to-nearest-neighbor interactions this would require many SWAP gates. In neutral-atom quantum processors, however, individual atoms can be dynamically rearranged during a computation, which yields a very good effective qubit connectivity [21,103,104] but can increase effective gate times. Moreover, the multiqubit gates required for our scheme are natively available in this platform [86].

TABLE II. Comparison of simulated logical failure rates for MFEC and flag EC, assuming that either the coherence times T_2^* or T_2 can be achieved. We list MFEC failure rates for *realistic* operation times and error rates, as well as anticipated future error rates that are *improved* by a factor of 2. For flag EC, we consider measurement times of 500μs and 1ms as representative values. While flag EC yields the lowest failure rate if coherence time T_2 can be achieved, MFEC outperforms flag EC with improved operations and if coherence times are limited to T_2^*.

Protocol (varied parameters)	$T_2^* = 4\mathrm{ms}$	$T_2 = 1\mathrm{s}$
MFEC (*realistic*)	$(5.9 \pm 0.3)\%$	$(5.6 \pm 0.1)\%$
MFEC (*improved*)	$(1.7 \pm 0.1)\%$	$(1.7 \pm 0.1)\%$
Flag EC ($t_{\mathrm{meas}} = 1\mathrm{ms}$)	$(11.8 \pm 0.4)\%$	$(0.66 \pm 0.04)\%$
Flag EC ($t_{\mathrm{meas}} = 500\mu\mathrm{s}$)	$(4.9 \pm 0.2)\%$	$(0.65 \pm 0.04)\%$

In Fig. 11 we propose a layout of atoms in a tweezer array, together with shuttling moves, to realize the measurement-free FT QEC scheme in an experiment. We assume a near-term neutral-atom platform with a global Rydberg laser illuminating all atoms in the tweezer array. This allows two-qubit gates or multiqubit gates to be performed on sets of atoms that are located within the blockade radius of each other. If those sets of atoms are placed sufficiently far away from each other, such gates can be performed in parallel [21,86]. Furthermore, we assume that atoms can be locally addressed to perform individual single-qubit gates. If also single-qubit gates can only be performed globally, additional shuttling moves of subsets of atoms into dedicated single-qubit gate operation zones are necessary. The left-hand side of Fig. 11 shows a circuit that realizes the measurement-free FT correction cycle for X errors. On the right-hand side we first depict the initial layout of 35 atoms in the tweezer array. As described in Sec. II, the higher number of qubits avoids that qubits have to be reset during the computation and allows for a minimal circuit depth. If in-sequence qubit reset is available, it is also possible to work with 17 atoms in a tweezer array, realizing the circuit shown in Fig. 2. We sketch the application of parallel two- and multiqubit gates as well as

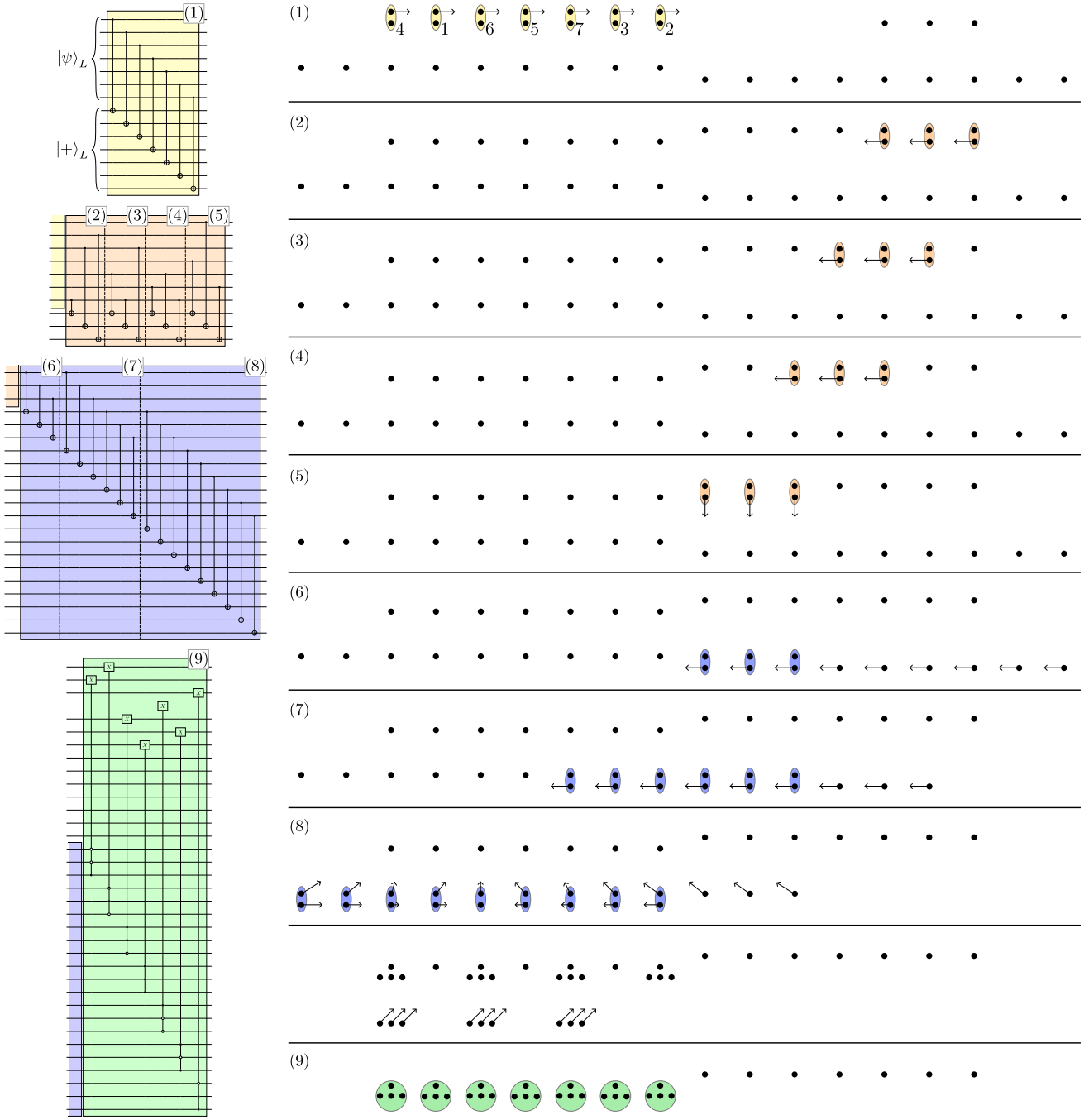

FIG. 11. Proposal for the implementation of the measurement-free FT QEC scheme with mobile neutral atoms in optical tweezers. The steps (1)–(9) correspond to the time steps as shown on the left-hand side of this figure and in Fig. 4. Ellipses that encircle sets of atoms correspond to the parallel application of entangling gates. Arrows indicate shuttling moves after the gate executions. Single-qubit gates are not shown.

shuttling moves, which are performed between the application of entangling gates. The application of single-qubit gates is not shown. We choose the atom layout in a way such that the total number of shuttling operations remains small and many parallel qubit moves are possible. The scheme requires a static 2D tweezer array, generated e.g., by a spatial light modulator (SLM), and a movable tweezer array realized with a single 2D acousto-optic deflector (AOD). Parallel moves of rows and columns are possible for atoms placed in the AOD array while atoms placed in the SLM tweezers remain fixed. Between shuttling operations, atoms can be relocated from static SLM tweezers into the dynamic AOD tweezers and vice versa [105, 106]. Our proposed shuttling protocol thus requires nine

parallel moves of atoms, which is comparable in complexity to already demonstrated experiments [21].

V. CONCLUSIONS AND OUTLOOK

In this work, we have presented a novel scheme for fault-tolerant quantum error correction without the need to measure individual physical qubits to read out the syndrome.

As we showed by numerical simulation, the measurement-free FT QEC scheme achieves logical failure rates approximately one order of magnitude higher than the corresponding flag error-correction protocol with single-parameter circuit-level depolarizing noise. Additionally, compilations of our scheme into different native gate sets can lead to variations and reductions in logical failure rates of up to one order of magnitude for the physical error rates we considered. This offers room for optimization to bridge the gap between the measurement-free and the conventional FT QEC schemes. We expect that a platform, which can realize an advantageous compilation, for instance, using native multiqubit-controlled gates with sufficient gate fidelities, can in this way at least partly compensate the extra infidelity introduced by the additional overhead in the measurement-free scheme compared to conventional syndrome-measurement EC. For a set of realistic parameters in a neutral atom setup, we showed via numerical simulation that the measurement-free FT QEC cycle can outperform flag-FT EC in the regime where system performance is limited by coherence time. Moreover, in neutral-atom platforms the outlined scheme may prove particularly useful due to the challenges posed by fast, low-loss, and fully parallelized measurements and real-time feedback. Furthermore, neutral atoms natively feature the possibility to realize multiqubit gates required for our scheme. Many of the required key components have been demonstrated recently in experiments, including midcircuit shuttling of atoms and parallel application of two-qubit and multiqubit gates [21,86]. Hardware-specific noise characteristics such as biased noise or bias-preserving gates [22], could even further compensate for the overhead of the measurement-free scheme. In this sense our simulations with depolarizing noise might be overly pessimistic.

However, also an embedding of the scheme into a solid-state platform is not futile since we do not require full all-to-all qubit connectivity. Optimizing the compilation of a scheme to hardware constraints like qubit connectivity in a systematic way could also further improve the scheme. It is an open question how additional physical qubits could be used for an embedding with reduced connectivity without breaking fault tolerance, for instance, by using the techniques of Refs. [107,108].

Extending our scheme to larger distance codes poses additional requirements for the construction of suitable fault-tolerant circuits on the auxiliary system. This is required to ensure that multiple faults do not cause a logical failure, which could be subject of future work, e.g., adapting concepts proposed in Refs. [55,56]. Since the measurement-free error-correction circuit has to implement a look-up decoder for an exponentially growing number of syndromes, we believe that code concatenation could be a promising approach to scale-up our scheme.

Additionally, developing new measurement-free versions of FT logical gates or FT gadgets such as code switching or lattice surgery would further enlarge the toolbox of measurement-free FT quantum computing protocols and thereby assist in enabling error-corrected universal quantum computation in future hardware platforms.

CODE AVAILABILITY

All codes used for data analysis are available from the corresponding author upon reasonable request.

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S.H. devised the scheme, its implementations, performed numerical simulations and analyzed the data. D.L. developed the neutral-atom implementation, embedding and schedules. All authors contributed to theory modeling. S.H. and D.L. wrote the manuscript with contributions from M.M. who supervised the project.

APPENDIX A: CORRECTING WEIGHT-2 ERRORS IN THE $d = 3$ SURFACE CODE

The distance-3 surface code has the property that in addition to all weight-1 errors some weight-2 errors can be corrected, e.g., with a look-up table decoder [71]. The code is defined by the stabilizers

$$\begin{aligned} K_1^X &= X_8X_9, & K_1^Z &= Z_6Z_7, \\ K_2^X &= X_5X_6X_7X_8, & K_2^Z &= Z_1Z_2Z_5Z_6, \\ K_3^X &= X_2X_3X_4X_5, & K_3^Z &= Z_4Z_5Z_8Z_9, \\ K_4^X &= X_1X_2, & K_4^Z &= Z_3Z_4 \end{aligned} \tag{A1}$$

and its logical operators can be chosen as $X_L = X_1X_6X_7$ and $Z_L = Z_1Z_2Z_3$ as shown in the insets of Fig. 12. The look-up table that is used in our measurement-free EC protocol to correct errors in the surface code is given in Table III. For example, the error X_4X_6 is correctable because its Z syndrome $\{-1,-1,-1,-1\}$ is not taken up by any other weight-1 X error. Due to the asymmetric arrangement of plaquettes, the error Z_4Z_6 is not correctable. Its X syndrome $\{+1,-1,-1,+1\}$ is already in use to correct the weight-1 error Z_5. This is why applying a multicontrolled-multitarget gate for the correction of X_4X_6 would destroy fault tolerance. In our scheme, however, a multicontrolled feedback gate will only couple to a single data qubit in order to preserve fault tolerance. Weight-2 errors could still be corrected by copying the respective syndrome twice and applying two distinct weight-1 feedback operations conditioned on this same syndrome instead of applying one weight-2 feedback operation. For instance, the Z syndrome $\{-1,-1,-1,-1\}$ must be copied twice to correct X_4 and X_6 distinctly. This, however, would increase the circuit depth and gate count of the coherent feedback circuit block considerably. Instead of applying weight-2 corrections, it is sufficient to transform weight-2 errors into correctable weight-1 errors—these will be corrected for in the subsequent EC round. This is sufficient to have a fully FT EC protocol. This conversion of weight-2 into weight-1 errors can be achieved for X and Z errors by the recovery operations given in Table III, which are translated into the feedback structure of the circuits in Fig. 12. Note that no weight-2 recoveries need to be applied. For the error X_4X_6, for instance, the circuit applies the recovery X_6 and leaves the correctable error X_4 on the logical data qubit. Note that, at the same time, all nine possible weight-1 errors will be corrected by the protocol, as required. Overall, this provides a compact fully FT and MF protocol, with the respective EC half-cycles for X- and Z-type correction implemented by the circuits in Figs. 12(a) and 12(b), respectively. Measurement-free and FT initialization of the auxiliary logical qubit is possible using, e.g., the encoding protocol recently demonstrated in Ref. [59].

For the measurement-free scheme applied to the surface code as shown in Fig. 12, we run numerical simulations with a single-parameter noise model (as in Fig. 9) to estimate the point where $p_L = p$. We find this threshold to lie at $p \approx 10^{-3}$, using native multiqubit-controlled gates. A detailed modeling of a realistic surface-code experiment is left for future work.

APPENDIX B: DECOMPOSING n-QUBIT-CONTROLLED-NOT GATES FOLLOWED BY RESET

An n-qubit-controlled-NOT gate followed by reset of the control qubits can be decomposed into a sequence of 2^n CNOT gates and additional single-qubit rotations. The recipe for such a construction is given in Fig. 13(a). Starting from the circuit identity in panel (i) for a single control qubit, decompositions of gates with more controls can be constructed iteratively by applying the substitution rule shown in panel (ii). Panel (iii) shows the circuit after one substitution step, realizing a Toffoli gate followed by reset of the control qubits. The construction of an $n+1$—from an n-qubit-controlled-NOT gate decomposition can be understood as follows. If the $n+1^{\text{st}}$ control qubit is in state $|0\rangle$, all T_k and $T_k^\dagger$ gates cancel pairwise and the circuit realizes the identity. If the $n+1^{\text{st}}$ qubit is in state $|1\rangle$, the circuit reduces to the circuit for n control qubits. To see this, one can insert pairs of X gates on the control qubit [for example, around the third CNOT gate in panel (iii)] and employ the identities $T_{2k}^\dagger X T_{2k} X = T_k^\dagger$ and $X T_{2k}^\dagger X T_{2k} = T_k$. Figure 13(b) shows the decomposition of a four-qubit-controlled-NOT gate followed by reset of the control qubits, which is required for the implementation of the measurement-free error-correction scheme for the surface code.

APPENDIX C: DECODING VARIANT

The syndrome mapping step from the n physical qubits that hold the logical auxiliary qubit state to the a physical qubits that hold the syndrome information can be simplified because the logical auxiliary qubit is discarded after the syndrome mapping anyway. Instead of supplying fresh

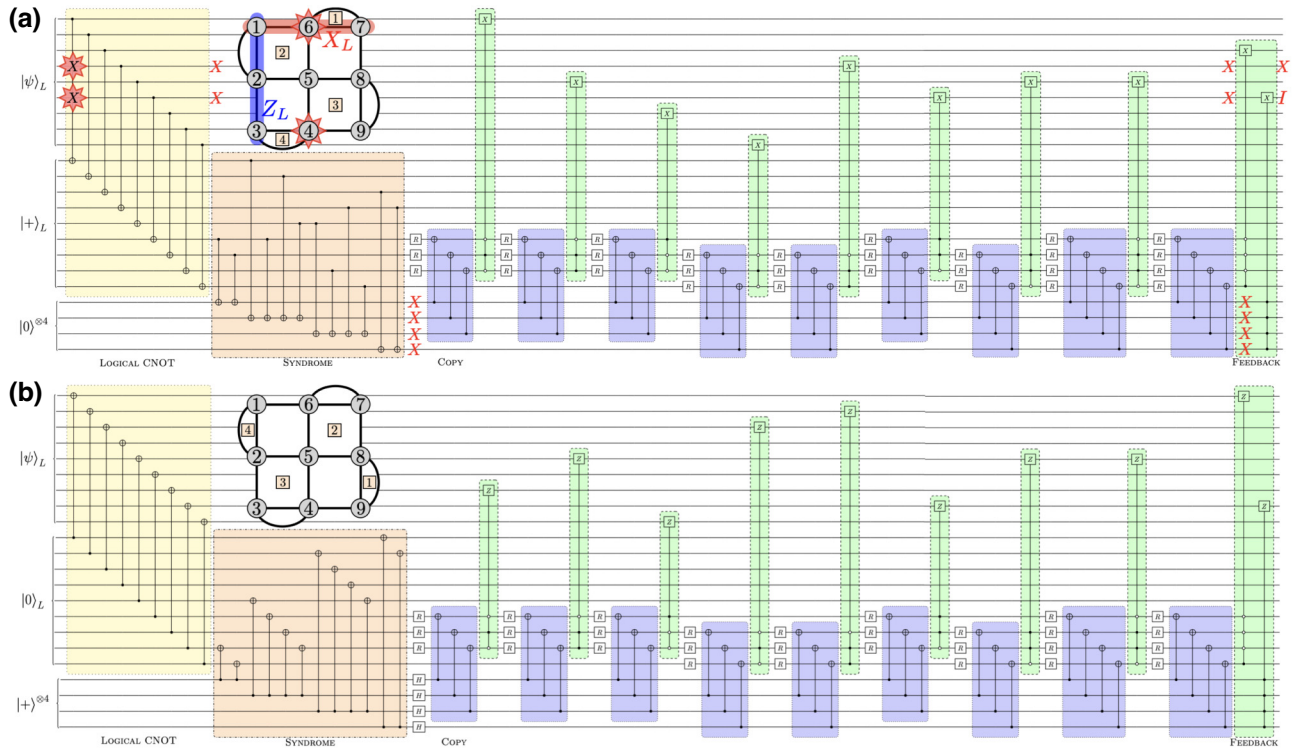

FIG. 12. Measurement-free FT QEC cycle for the distance-3 surface code based on the look up table in Table III. (a) X-correction block with the correctable weight-2 error X_4X_6 (red stars), which is transformed to X_4. (b) Z-correction block. Note that 7 (3) out of 10 feedback operations in each block are conditional 3-qubit-controlled (4-qubit-controlled) multiqubit gates.

auxiliary qubits, one may replace the syndrome mapping step [orange box in Fig. 2(a)] with a decoding circuit. This can reduce the required number of qubits to perform the MFEC cycle to $N = 2n$. The decoding circuits can be constructed by inverting encoding circuits of, for instance, surface code or color code states with similar numbers of CNOT gates as the syndrome mapping [109,110]. An example for the X-correction block of the Steane code, where the logical auxiliary qubit is initialized to the $|+\rangle_L$ state, is shown in Fig. 14. Here, the physical qubits 1, 2, and 4 carry the expectation value of the Z-type stabilizer generators K_2^Z, K_3^Z, and K_1^Z respectively. The expectation value is $+1(-1)$ if the physical qubit is in the $|0\rangle$ ($|1\rangle$) state.

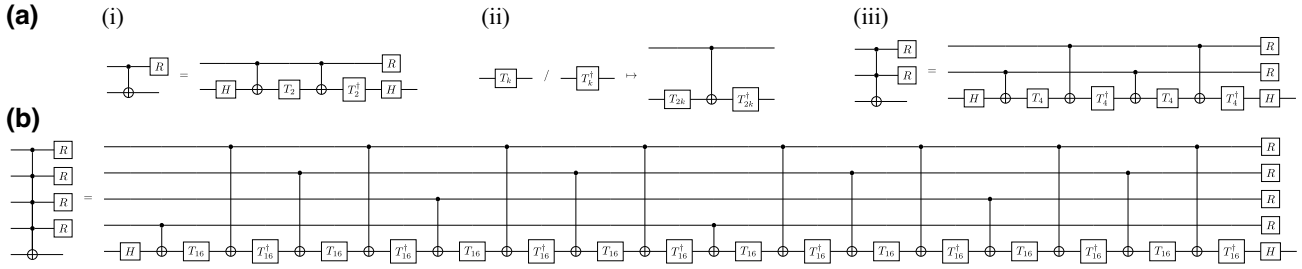

FIG. 13. (a) Recipe how to construct n-qubit-controlled-NOT gates followed by reset (R) of the control qubits from CNOT gates and single-qubit gates H (Hadamard) and $T_k = \exp(-\mathrm{i}\frac{\pi}{2k}Z)$. It is straightforward to see that the circuit identity in panel (i) holds. Going from an n-qubit-controlled-NOT gate to an $(n+1)$-qubit-controlled-NOT gate followed by reset of the control qubits can be realized by performing the substitution rule stated in panel (ii), where the CNOT gate is controlled on the newly added control qubit. Panel (iii) shows the resulting circuit realizing a Toffoli gate followed by reset of the control qubits. If the $n+1^{\text{st}}$ control qubit is in state $|0\rangle$, the circuit trivially reduces to the identity. If the $n+1^{\text{st}}$ control qubit is in state $|1\rangle$, the circuit reduces to the circuit for n control qubits, which can be seen by employing the identities $T_{2k}^\dagger X T_{2k} X = T_k^\dagger$ and $X T_{2k}^\dagger X T_{2k} = T_k$. (b) Decomposition of a four-qubit-controlled-NOT gate followed by reset of the control qubits into a sequence of CNOT and single-qubit gates. This gate is required to implement the measurement-free error-correction scheme for the surface code, as shown in Fig. 12.

TABLE III. The four-bit Z syndrome (upper half) of the surface code shown in the inset of Fig. 12(a) allows one to correct not only all nine single-qubit X errors but also some additional weight-2 X errors. Note that, for instance, applying X_8 corrects both errors X_8 and X_9 since $K_1^X = X_8X_9$ is a stabilizer. The third column contains the recovery operations that are applied by the circuit in Fig. 12 and the last column shows that the result RE is always an error of at most weight-1. The X syndromes and corresponding Z-type operations are given in the lower half of the table and the X stabilizers are shown in the inset of Fig. 12(b).

Syndrome $(K_1^Z, K_2^Z, K_3^Z, K_4^Z)$	Error E	Recovery R	Outcome RE
$++++$	I	I	I
$+++-$	X_3	X_3	I
$++-+$	X_8 (or X_9)	X_9	K_1^X (or I)
$++--$	X_4	X_4	I
$+-++$	X_1 (or X_2)	X_1	I (or K_4^X)
$+-+-$	X_1X_3	X_1	X_3
$+--+$	X_5	$X_5X_5X_5$	I
$+---$	X_3X_5	X_5	X_3
$-+++$	X_7	X_7	I
$-++-$	X_3X_7	X_7	X_3
$-+-+$	X_7X_9	X_9	X_7
$-+--$	X_4X_7	X_4	X_7
$--++$	X_6	X_6	I
$--+-$	X_3X_6	X_6	X_3
$---+$	X_5X_7	X_5	X_7
$----$	X_4X_6	X_6	X_4
Syndrome $(K_1^X, K_2^X, K_3^X, K_4^X)$	Error E	Recovery R	Outcome RE
$++++$	I	I	I
$+++-$	Z_1	Z_1	I
$++-+$	Z_4 (or Z_3)	Z_3	K_4^Z (or I)
$++--$	Z_2	Z_2	I
$+-++$	Z_7 (or Z_6)	Z_7	I (or K_1^Z)
$+-+-$	Z_1Z_7	Z_7	Z_1
$+--+$	Z_5	$Z_5Z_5Z_5$	I
$+---$	Z_1Z_5	Z_5	Z_1
$-+++$	Z_9	Z_9	I
$-++-$	Z_1Z_9	Z_9	Z_1
$-+-+$	Z_3Z_9	Z_3	Z_9
$-+--$	Z_2Z_9	Z_2	Z_9
$--++$	Z_8	Z_8	I
$--+-$	Z_1Z_8	Z_8	Z_1
$---+$	Z_5Z_9	Z_5	Z_9
$----$	Z_2Z_8	Z_8	Z_2

Note that, as for the syndrome mapping described in the main text, the decoding block itself does not need any fault-tolerance overhead for the full MFEC scheme to be fault tolerant. If there are not enough physical qubits after the decoding step to coherently copy the syndrome information, additional auxiliary qubits must be supplied.

The minimal circuit depth is unchanged with this modification of the orange block since the decoding in Fig. 14 needs four time steps, just as the syndrome mapping. However, one could use, for instance, a sequence of only three four-qubit MS gates, if practically available, to perform the decoding step [111].

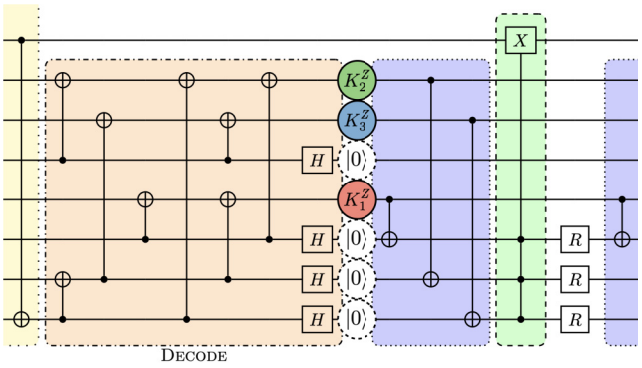

FIG. 14. Performing an inverse encoding circuit for the $|+\rangle_L$ state leaves the Z syndrome (K_1^Z, K_2^Z, K_3^Z) on qubits 4, 1, and 2 of the orange block as indicated, respectively, by the RGB-colored circles. The syndrome mapping step [orange box in Fig. 2(a)] is replaced with the decoding block and the copy and feedback steps are adjusted accordingly. In the absence of noise, each of the four other physical qubits is in the $|0\rangle$ state after decoding (dashed white circles).

APPENDIX D: NOISE MODEL

We consider the depolarizing channel of strength p

$$\mathcal{E}_p(\rho) = (1-p)\rho + \frac{p}{4^q-1}\sum_{\sigma\in\Lambda}\left(\bigotimes_{j=1}^{q}\sigma_j\right)\rho\left(\bigotimes_{j=1}^{q}\sigma_j\right) \tag{D1}$$

where $\Lambda = \{I, X, Y, Z\}^{\otimes q}\backslash\{I^{\otimes q}\}$ and q is the number of qubits the noise channel acts on. It is the most general noise channel in the sense that the 4^q Pauli operators (and the identity operation) form the basis of the q-qubit Pauli group. Thus, any fault that can happen in a physical gate can be expressed in this Pauli basis. As a consequence, if the circuit is FT under the channel in Eq. (D1), then it is FT towards any noise channel on the q qubits.

For the single-parameter noise model in Secs. II C and IV A we use the conventional depolarizing noise model where

(1) a single-qubit gate is followed by a Pauli fault drawn uniformly and independently from $\{X, Y, Z\}$ with probability $p/3$,
(2) a two-qubit gate is followed by a two-Pauli fault drawn uniformly and independently from $\{I, X, Y, Z\}^{\otimes 2}\backslash I\otimes I$ with probability $p/15$,
(3) qubit initialization is flipped ($|0\rangle \to |1\rangle$) with probability $2p/3$,
(4) qubit measurements yield a flipped result ($\pm 1 \to \mp 1$) with probability $2p/3$ and

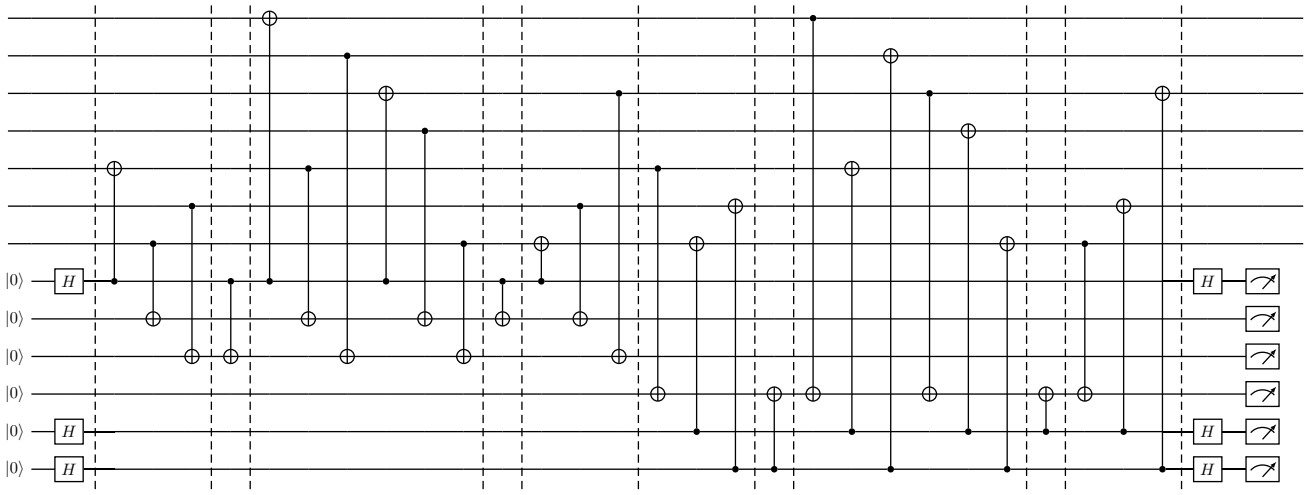

FIG. 15. Parallel measurement of three stabilizers in two sequential steps realizes the flag fault-tolerant circuit for error detection [57]. Due to the interleaved scheduling of CNOT gates, all six auxiliary qubits act as measurement and flag qubits at the same time.

(5) idling locations are followed by a Pauli fault drawn uniformly and independently from $\{X, Y, Z\}$ with probability $p/100$.

Additionally, for the multiparameter noise model in Secs. IV B and IV C, q-qubit gates are followed by Pauli faults drawn randomly and uniformly from $\{I, X, Y, Z\}^{\otimes q} \backslash I^{\otimes q}$ with respective probabilities p_q. For modeling of dephasing noise on idling locations during multiqubit gates, initializations and measurements in Secs. IV B and IV C, we use the single-qubit channel

$$\mathcal{E}_{p_{\mathrm{idle},q}}(\rho) = (1 - p_{\mathrm{idle},q})\rho + p_{\mathrm{idle},q} Z\rho Z \tag{D2}$$

with respective idling error rates $p_{\mathrm{idle},q}$ during q-qubit gates and a rate $p_{\mathrm{idle},i}$ ($p_{\mathrm{idle},m}$) during physical qubit initialization (measurement).

APPENDIX E: DETAILS OF MFEC PERFORMANCE

In this section, we provide the analytical estimation of a parameter region for advantageous use of the MFEC scheme, given by Eq. (3). First, we look at the two limits where only one type of noise, either on physical operations or idling locations, is present in the system. Then we interpolate between these limits and estimate parameter regions of advantageous use of either the MFEC or the SMEC protocol.

Let us consider the limit of vanishing physical operation error rates $p \to 0$ first so that only idling noise is present in the system. Then, MFEC is advantageous over SMEC when its QEC cycle time $\tau_{\mathrm{MF}} < \tau_{\mathrm{SM}}$ is smaller than the syndrome measurement EC cycle time. For their logical failure rates this means that then $p_L^{\mathrm{MF}}/p_L^{\mathrm{SM}} < 1$. For an FT protocol, the ratio of logical failure rates is proportional to the squared cycle time ratio

$$\frac{p_L^{\mathrm{MF}}}{p_L^{\mathrm{SM}}} = \left(\frac{\tau_{\mathrm{MF}}}{\tau_{\mathrm{SM}}}\right)^2 \tag{E1}$$

if idling were the only source of failure and we operate in a regime where $\tau \ll T_2$. Single faults of probability $p_{\mathrm{idle}} \sim \tau$ cannot lead to failure due to the FT circuit design of the protocol.

Assuming that a single operation in the MF protocol takes time t_{ops}, we can estimate the total cycle time as

$$\tau_{\mathrm{MF}} \simeq t_{\mathrm{ops}} \times \#\mathrm{operations} \tag{E2}$$

in case all operations are executed sequentially. When the SMEC protocol cycle time is dominated by the time t_{meas} to perform a qubit measurement, i.e., we assume that measurements take much more time than gate operations, we can estimate

$$\tau_{\mathrm{SM}} \simeq t_{\mathrm{meas}} \times \#\mathrm{measurements}. \tag{E3}$$

As another limiting case, we assume no idling noise at all, i.e., the coherence time $T_2 \to \infty$, so that the operation error rate $p \neq 0$ is the only nonvanishing physical error rate. In this case, the logical failure rates scale like

$$p_L^{\mathrm{MF}} \sim (cp)^2 \tag{E4}$$

$$p_L^{\mathrm{SM}} \sim (c'p)^2 \tag{E5}$$

for $p \ll 1$ since no single fault of probability p can cause a logical failure. The two constants c^2 and c'^2 are determined by the number of *bad* locations, i.e., fault locations that

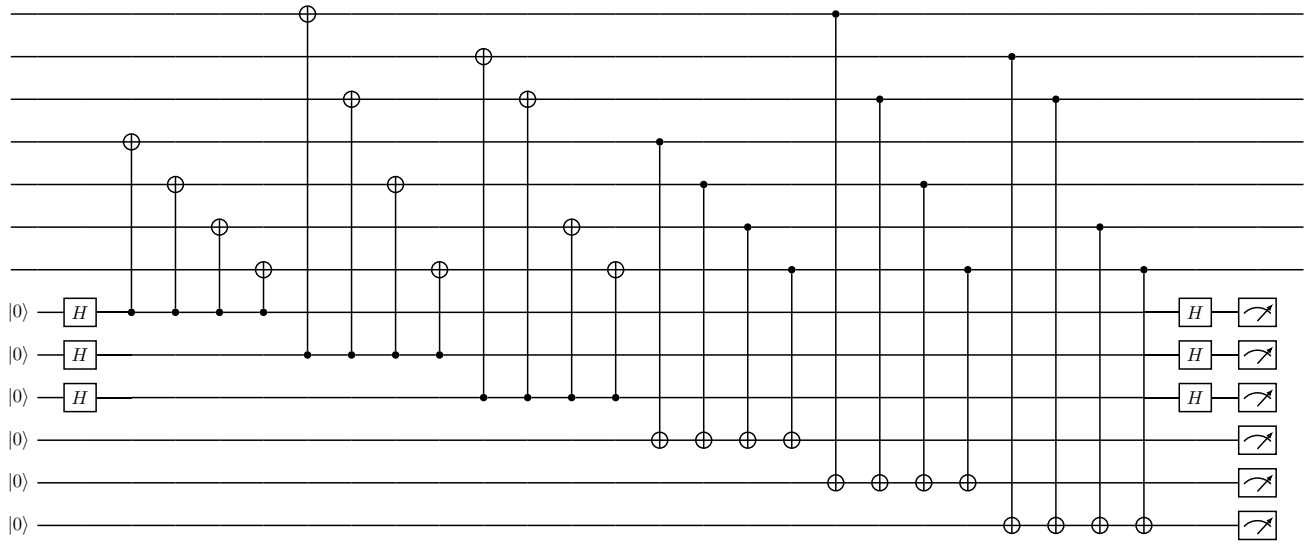

FIG. 16. Nonflagged circuit to readout all six stabilizers sequentially. Combined with the flag information from the circuit in Fig. 15, this circuit is used for FT syndrome readout.

can lead to failure, for each respective protocol. Their ratio determines the (dis)advantage of MFEC over SMEC since

$$\frac{p_L^{\mathrm{MF}}}{p_L^{\mathrm{SM}}} = \left(\frac{c}{c'}\right)^2. \tag{E6}$$

Now, in a realistic scenario where both idling and operations are prone to noise, the small-p behavior of the logical failure rate will be

$$p_L^{\mathrm{MF}} \sim c^2 p^2 + \tilde{c}^2 p_{\mathrm{idle,op}}^2 + bpp_{\mathrm{idle,op}} \tag{E7}$$

$$p_L^{\mathrm{SM}} \sim c'^2 p^2 + \tilde{c}'^2 p_{\mathrm{idle},m}^2 + b'pp_{\mathrm{idle},m} \tag{E8}$$

for $p, p_{\mathrm{idle}} \ll 1$ since at least two faults in total are needed to cause logical failure for both protocols: either two faults on operations with probability p each or two faults on idling locations with probability p_{idle} each or one operation fault with probability p and another idling fault with probability p_{idle} can cause logical failure. The constants $\tilde{c}, \tilde{c}', b$, and b' are determined analogously to c and c' by the number of bad locations of these respective fault combinations. Here we included the respective dominant source of idling noise for both protocols; idling during operations with rate $p_{\mathrm{idle,op}}$ for the MF protocol and idling during measurements with rate $p_{\mathrm{idle},m}$ for the SM protocol. Again, we assume for the latter that measurements are much slower than operations.

We can upper bound Eqs. (E7) and (E8) by assuming that the constants $c, \tilde{c}, b, c', \tilde{c}'$, and b' represent the *total* number of respective circuit locations for two operation faults, two idling faults or both one operation and one idling fault for either protocol. Then b and b' can be expressed as the products $c\tilde{c}$ and $c'\tilde{c}'$, respectively. In principle, one could also determine these constants by exhaustively counting the numbers of bad locations, i.e., placing all possible combinations of two fault operators on operation and idling locations, or estimate the fraction of bad locations to total locations via Monte Carlo simulation. The ratio of logical failure rates from Eq. (E6) is then extended to read

$$\frac{p_L^{\mathrm{MF}}}{p_L^{\mathrm{SM}}} \sim \frac{(cp)^2 + (\tilde{c}p_{\mathrm{idle,op}})^2 + c\tilde{c}pp_{\mathrm{idle,op}}}{(c'p)^2 + (\tilde{c}'p_{\mathrm{idle},m})^2 + c'\tilde{c}'pp_{\mathrm{idle},m}} \tag{E9}$$

where all contributions come with their own constants $c, c', \tilde{c}, \tilde{c}'$.

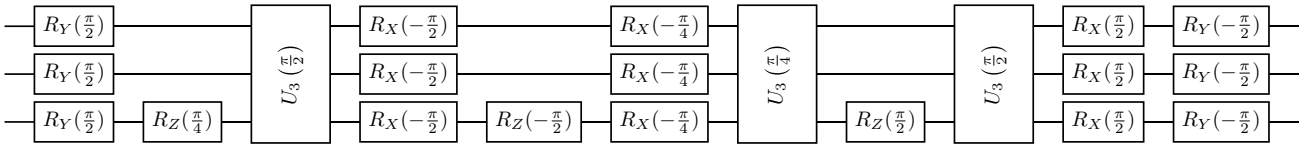

FIG. 17. The Toffoli gate used for the quantum feedback in Fig. 6 can be compiled to multi-ion MS gates given by Eq. (8) and local rotations $R_\sigma = \exp[-\mathrm{i}(\theta/2)\sigma]$ with $\sigma \in \{X, Y, Z\}$ [97]. The first two wires are the control qubits and the third wire is the target qubit. The decomposition is exact. The last X and Y rotations on the control qubits could be omitted in our case due to the subsequent reset.

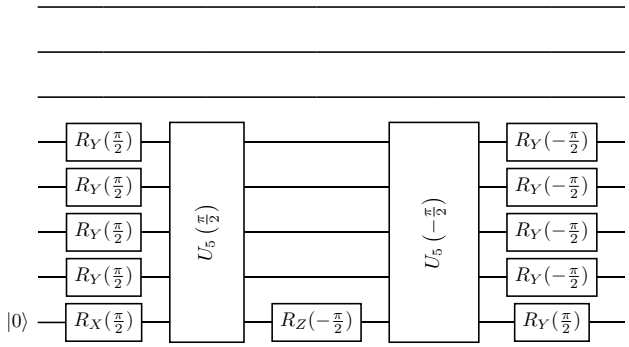

FIG. 18. Circuit to read out the stabilizer $K_1^Z = Z_4Z_5Z_6Z_7$ using two five-qubit MS gates with $\theta = \pm\pi/2$ and single-qubit rotations [78,96]. The stabilizer eigenvalue is mapped to the last qubit by the gate sequence. To read out the corresponding X-type stabilizer, the Y rotations on the data qubits must be omitted.

We can expand Eq. (E9) around $p = 0$ and $p_{\text{idle,op}} = 0$ so that we include all second-order terms:

$$\frac{p_L^{\text{MF}}}{p_L^{\text{SM}}} = \left(\frac{\tilde{c}^2}{\tilde{c}'^2}\frac{p_{\text{idle,op}}^2}{p_{\text{idle},m}^2} + \mathcal{O}(p_{\text{idle,op}}^3)\right) + p\left(\frac{c\tilde{c}p_{\text{idle,op}}}{\tilde{c}'^2 p_{\text{idle},m}^2} + \mathcal{O}(p_{\text{idle,op}}^2)\right) + p^2\left(\frac{c^2}{\tilde{c}'^2 p_{\text{idle},m}^2} + \mathcal{O}(p_{\text{idle,op}})\right) + \mathcal{O}(p^3). \quad \text{(E10)}$$

We roughly estimate the MF advantage $p_L^{\text{MF}}/p_L^{\text{SM}} \leq 1$, as given by Eq. (3), whenever the ratio of idling times (or error rates, provided they are sufficiently small due to $t/T_2 \ll 1$)

$$\frac{t_{\text{meas}}}{t_{\text{ops}}} \approx \frac{p_{\text{idle},m}}{p_{\text{idle,op}}} \geq \sqrt{\frac{\tilde{c}^2}{\tilde{c}'^2} + \frac{c\tilde{c}}{\tilde{c}'^2}\frac{p}{p_{\text{idle,op}}} + \frac{c^2}{\tilde{c}'^2}\frac{p^2}{p_{\text{idle,op}}^2}} \quad \text{(E11)}$$

is larger then the bound set by our estimation of the error-rate ratios, which translates to

$$\frac{t_{\text{meas}}}{t_{\text{ops}}} \gtrsim \sqrt{\frac{\tilde{c}^2}{\tilde{c}'^2} + 2T_2\frac{c\tilde{c}}{\tilde{c}'^2}\frac{p}{t_{\text{ops}}} + 4T_2^2\frac{c^2}{\tilde{c}'^2}\frac{p^2}{t_{\text{ops}}^2}} \quad \text{(E12)}$$

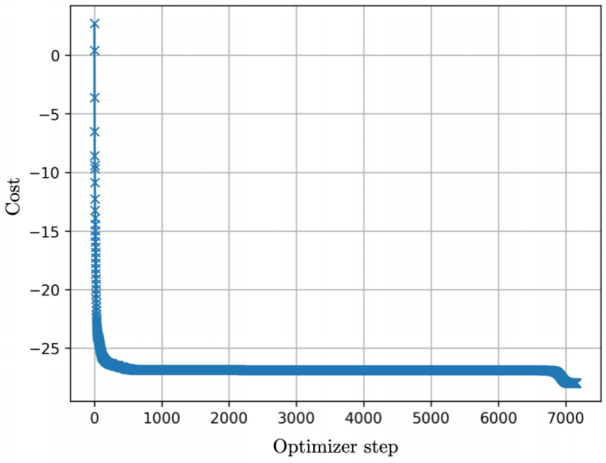

FIG. 20. The cost function converged to the target value of −28 for the parametrized circuit in Fig. 19.

using Eq. (2). Note again that we have assumed the ratios $\tilde{c}^2/\tilde{c}'^2$, $c\tilde{c}/\tilde{c}'^2$, and $c^2/\tilde{c}'^2$ for the numbers of *total* locations to be approximately equal to the ratios using the numbers of *bad* locations.

The boundary between regions of advantageous use of either MFEC or SMEC is estimated approximately by Eq. (E11), which is illustrated in Fig. 5 for comparison to a state-of-the-art flag EC protocol [57]. The flag scheme consists of sequentially running two blocks of three parallel stabilizer measurements. In case a nontrivial measurement occurs, an additional round of nonflagged syndrome readout is performed and the correction is inferred from the flag error set and the Steane code's look-up table (see Appendix F for details). All gate operations are executed sequentially, i.e., with only one gate per time step. Physical qubit initializations and measurements are executed in parallel in the simulation. For the MF scheme the numbers of locations are

$$c = \#\text{operations(MF)} = 456 \quad \text{(E13)}$$

$$\tilde{c} = \#\text{idlingduringoperations(MF)} = 5790 \quad \text{(E14)}$$

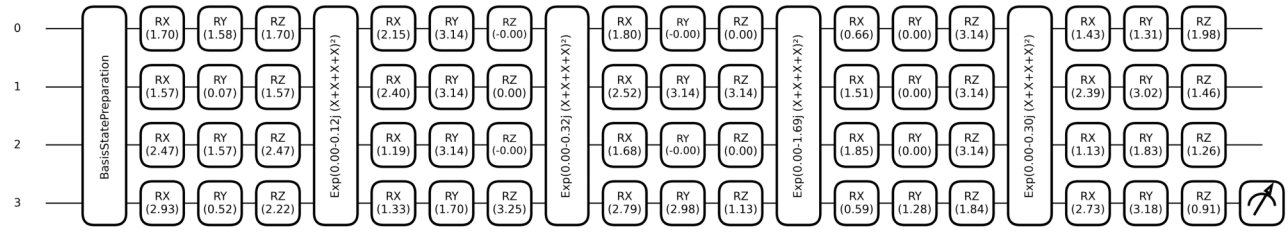

FIG. 19. Compiled circuit with rounded rotation angles that implements the C_3NOT gate followed by resetting the control qubits. The first three wires are the control qubits and the fourth wire is the target qubit.

TABLE IV. Angle parameters for the C_3NOT gate decomposition in Fig. 19.

Time step	rotation	Angle θ	Time step	rotation	Angle θ
1	$R_X^{(1)}$	1.7016306974989441	40	$R_X^{(1)}$	0.6597193711414078
2	$R_Y^{(1)}$	1.5795679517126637	41	$R_Y^{(1)}$	0.000127747992253436
3	$R_Z^{(1)}$	1.7016364361060135	42	$R_Z^{(1)}$	3.141326508787639
4	$R_X^{(2)}$	1.5706691398072636	43	$R_X^{(2)}$	1.5086374816792918
5	$R_Y^{(2)}$	0.07488703273604898	44	$R_Y^{(2)}$	0.0003195950440647524
6	$R_Z^{(2)}$	1.5708162845196991	45	$R_Z^{(2)}$	3.141618529495557
7	$R_X^{(3)}$	2.4733498110482617	46	$R_X^{(3)}$	1.851040827063517
8	$R_Y^{(3)}$	1.570978087668805	47	$R_Y^{(3)}$	$2.5330048710337304 \cdot 10^{-5}$
9	$R_Z^{(3)}$	2.473338798284629	48	$R_Z^{(3)}$	3.141620662584241
10	$R_X^{(4)}$	2.925198421469473	49	$R_X^{(4)}$	0.5851416542930774
11	$R_Y^{(4)}$	0.5184554247895697	50	$R_Y^{(4)}$	1.2817745160285958
12	$R_Z^{(4)}$	2.2155872069814624	51	$R_Z^{(4)}$	1.8434910130310886
13	MS	0.47618449796926465	52	MS	1.1852630143343514
14	$R_X^{(1)}$	2.1467351234080563	53	$R_X^{(1)}$	1.4334708713034108
15	$R_Y^{(1)}$	3.141888995985973	54	$R_Y^{(1)}$	1.3149000591854494
16	$R_Z^{(1)}$	−0.0007547728309335194	55	$R_Z^{(1)}$	1.9799754514097745
17	$R_X^{(2)}$	2.400499912253685	56	$R_X^{(2)}$	2.385180572177377
18	$R_Y^{(2)}$	3.1415882232243812	57	$R_Y^{(2)}$	3.0169184347659774
19	$R_Z^{(2)}$	$6.7559904951046 \cdot 10^{-5}$	58	$R_Z^{(2)}$	1.4620953315141385
20	$R_X^{(3)}$	1.185074722683019	59	$R_X^{(3)}$	1.1258670832503659
21	$R_Y^{(3)}$	3.141691576333686	60	$R_Y^{(3)}$	1.8289082653712643
22	$R_Z^{(3)}$	$-3.562993822558777 \cdot 10^{-5}$	61	$R_Z^{(3)}$	1.257061399856186
23	$R_X^{(4)}$	1.3267674839439592	62	$R_X^{(4)}$	2.726979125875662
24	$R_Y^{(4)}$	1.697674066992338	63	$R_Y^{(4)}$	3.182404050384048
25	$R_Z^{(4)}$	3.2542541431385135	64	$R_Z^{(4)}$	0.9113006716946862
26	MS	1.2961753988001792			
27	$R_X^{(1)}$	1.80332241033805			
28	$R_Y^{(1)}$	$-9.14307205449397 \cdot 10^{-6}$			
29	$R_Z^{(1)}$	0.00013217255162876435			
30	$R_X^{(2)}$	2.5206093101178855			
31	$R_Y^{(2)}$	3.141617687717394			
32	$R_Z^{(2)}$	3.141423898780103			
33	$R_X^{(3)}$	1.6829531013144419			
34	$R_Y^{(3)}$	$-1.2744701675664226 \cdot 10^{-5}$			
35	$R_Z^{(3)}$	$1.1892895790349708 \cdot 10^{-5}$			
36	$R_X^{(4)}$	2.7949214025522897			
37	$R_Y^{(4)}$	2.9814542086299864			
38	$R_Z^{(4)}$	1.134224555725302			
39	MS	6.779626443860337			

and for the flag scheme we use

$$c' = \#\text{operations(FL)} = 88 \tag{E15}$$

$$\tilde{c}' = \#\text{idlingduringmeasurement(FL)} = 14. \tag{E16}$$

The parameter regions shown in the utility diagram of Fig. 5 correspond to these values.

APPENDIX F: CIRCUITS FOR FLAG EC

The flag EC scheme used for comparison in Secs. II C, IV A and IV C was suggested in Ref. [57] and has been recently implemented with trapped ions [14,16]. It consists of application of the two circuits shown in Figs. 15 and 16.

As a first step, all stabilizers are measured in an interleaved way with the help of six auxiliary qubits. When all six qubits are measured as +1, we know that no uncorrectable error is present on the data qubits. When any of the qubits is measured as −1 however, we cannot tell whether

faults have propagated from within the measurement circuit to the data qubits or there have been faults on the input state already. The additional round of syndrome readout, performed as a second step, is needed to clarify the syndrome of the faulty state. If the syndrome is different from the previously measured one, we interpret the measurement outcome of the first block as a flag event. This means that we apply the appropriate two-qubit correction according to the flag error set if the syndrome is consistent with the possible two-qubit errors. Otherwise, or if the two measured syndromes agree, we apply the single-qubit correction according to the Steane code's look-up table. This way, logical failures can only happen with probability $\mathcal{O}(p^2)$.

APPENDIX G: MULTI-ION MS GATE CIRCUITS

In the following, we list the components needed to compile the MFEC scheme in Fig. 2 into multi-ion MS gates, as discussed in Sec. IV B.

CNOT gate. For the decompositions of CNOT gates into two-qubit MS gates and local rotations $R_\sigma = \exp[-\mathrm{i}(\theta/2)\sigma]$ with $\sigma \in \{X, Y, Z\}$ we use the identity

$$\begin{aligned} \mathrm{C}_i\mathrm{NOT}_j = {} & R_Y^{(i)}(-\pi/2)R_X^{(i)}(\pi/2)R_X^{(j)}(\pi/2)U_2^{(ij)} \\ & (-\pi/2)R_Y^{(i)}(\pi/2) \end{aligned} \tag{G1}$$

for a gate acting on qubits i and/or j [112].

1. Toffoli gate

The Toffoli gate decomposition into three three-qubit MS gates and local rotations from Ref. [97] is reproduced in Fig. 17.

2. Syndrome mapping

The circuit that uses two five-qubit MS gates for mapping of a stabilizer expectation value to a single auxiliary qubit from Refs. [78,96] is reproduced in Fig. 18 for the stabilizer K_1^Z. The circuits for the other Z-type stabilizers are analogous. For the mapping of X-type stabilizers, no Y rotations on the data qubits must be applied.

3. C_3NOT gate

The C_3NOT gate followed by reset of the control qubits can be decomposed into four four-qubit MS gates as shown in Fig. 19. We found the decomposition using a parametrized circuit ansatz in pennylane [98]. The parameters $\vec{x}$ are the 64 rotation angles that parametrize the four four-qubit MS gates and layers of arbitrary X, Y, and Z rotations on each qubit before and after the four-qubit MS gates. As a cost function, we use the weighted average of the Pauli-X and -Z expectation value of the target qubit for application of the parametrized circuit unitary $U(\vec{x})$ to all 16 computational basis states and additional 16 states with the control qubits in the computational basis and the target qubit in the polar basis. The expectation values of the states $U(\vec{x})\,|1110\rangle$, $U(\vec{x})\,|1111\rangle$, $U(\vec{x})\,|111+\rangle$, and $U(\vec{x})\,|111-\rangle$ are multiplied by $-7/2$ while all other states have weight $-1/2$ so that the minimal cost function value is -28. We keep optimizing the circuit parameters using the `AdagradOptimizer` in pennylane until the minimal value is found with an absolute tolerance of 10^{-4} (see Fig. 20). The converged angles for all 64 gates in the parametrized circuit are given in Table IV.

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