Variability Reduction with Bilayer RRAM Device

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***Abstract*—The inherent stochastic behavior of filamentary switching introduces significant cycle-to-cycle (C2C) fluctuations in the device characteristics, which poses a challenge to the practical applications of resistive random-access memories (RRAMs). Here, we report a simple bilayer oxide-based device structure of TaO_x/HfO_2 on a 180-nm CMOS substrate to address this variability issue and improve the overall performance of the memory device. The improved switching variability in the bilayer stack is attributed to the incorporation of a conductive TaO_x thin film, which serves as the switching layer after the conductive filament formation in HfO_2. More specifically, the switching happens at the interface between the conductive filament and TaO_x and exhibits a more gradual and less stochastic behavior than filamentary switching. As a result, 3-bit multi-level non-overlapping switching can be demonstrated in TaO_x/HfO_2 bilayer RRAM devices. These findings could be crucial for the high density data storage applications of RRAMs.**

Keywords—Bilayer RRAM, Variability, 3-Bit MLC

I. INTRODUCTION

Resistive random-access memory (RRAM) is considered a promising technology for the next generation of non-volatile memory (NVM) and neuromorphic computing applications due to its simple metal-insulator-metal (MIM) device geometry that possesses high speed operation, low power consumption, and excellent scalability [1-3]. Though the resistive switching phenomena has been observed in various dielectrics, simple binary metal oxides, namely, TiO_x, HfO_x, and TaO_x, etc., have been found to be more promising [4-6]. Within the realm of binary metal oxides, TaO_x and HfO_x-based devices have garnered significant attention, primarily due to their exceptional device performance, ease of fabrication, and compatibility with semiconductor (CMOS) process technology [7-8].

The filamentary resistive switching effect is generally driven by the growth and rupture of conductive filaments (CFs) within the switching oxide film. Particularly, the filaments in oxide-based RS devices are composed of a highly oxygen-deficient region. However, the size, shape, and location of these CFs inside the switching layer are completely stochastic, which, in turn, induces cycle-to-cycle (C2C) and device-to-device (D2D) variability in RRAMs [9]. This poses a major challenge for the commercialization of RRAM technology. Several strategies have been proposed to overcome this critical issue such as impurity doping, insertion of nanoparticles, and interface engineering [10-12]. In this work, we report a simple and practical approach for achieving low variability resistive switching operation in TaO_x/HfO_2 bilayer devices with 3-bit multilevel storage capability fabricated by physical vapor deposition technique. The stoichiometry and resistivity of the conductive TaO_x thin film is tailored by the oxygen flow rate during the sputtering deposition. In HfO_2-based RRAM devices utilizing a conductive metal oxide (CMO), such as TaO_x in the bilayer devices, a gradual SET transition in clockwise switching direction is observed [13]. After the CF is formed in the HfO_2-layer of CMO/HfO_2-based RRAM, the resistive switching happens within the CMO, specifically at the CMO/CF interface [14]. Since this type of resistive switching is less stochastic than filamentary switching, a gradual SET transition and a lower variability can be obtained. Hence, the bilayer device (TaO_x/HfO_2) structure considerably improves the C2C variability during the switching. The C2C variability is further compared with single switching oxide (W/Ta_2O_5) RRAM.

The multi-level cell (MLC) operation can be achieved either by varying the current compliance (I_{CC}) during the SET process or changing the RESET stop voltages during the RESET process [15, 16]. A precise control over multiple resistance states is obtained by using different I_{CC}. By varying the I_{CC} during the SET process, 8 distinct and reproducible resistance states are achieved for the bilayer RRAM devices.

II. DEVICE FABRICATION

For this study, 100 x 100 nm^2 RRAM devices were fabricated on a 180-nm CMOS substrate. On the processed substrate, which was designed and fabricated in collaboration with X-FAB, single 1T-1R structures as well as 1T-1R arrays of different dimensions can be found. All results shown in this work originate from single 1T-1R devices. The cross section schematic of the integrated 1T-1R device is shown in Fig. 1. After exposing the W-plug, a 25-nm-thick Pt layer, serving as bottom electrode is deposited on the CMOS substrate with DC sputtering process. This layer is eventually patterned by electron beam lithography, followed by back etching using reactive ion etching (RIE). Subsequently, for single layer RRAM, a 7-nm-thick TaO_X layer was deposited by RF-sputtering Ar (77%) and O_2 (23%) gas mixture at 236 W RF power followed by deposition of 13-nm-thick W through DC sputtering using Ar gas without breaking the vacuum. The bilayer RRAM stack was also deposited in the similar process consisting of 3-

nm-thick HfO_2 layer by RF sputtering using Ar (60%) and O_2 (40%) gas mixture at 200 W RF power followed by RF sputtering of 30-nm-thick TaOx using Ar (99%) and O_2 (1%) at 85 W RF power. The oxygen-deficient TaO_x thin-film in the bilayer stack exhibits a high electrical conductivity. Next, a 25-nm-thick Pt top electrode (TE) was deposited using DC sputtering on both samples. Finally, the switching oxide and TE stack were patterned and etched using electron beam lithography and RIE, respectively. Figure 1 shows the SEM image of the 100 x 100 nm^2 crossbar device fabricated on the CMOS substrate in 1T-1R configuration. In this configuration, an NMOS transistor serves as a current limiter for the RRAM device.

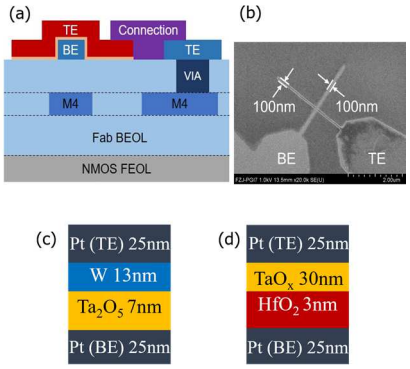

Fig. 1. Cross-sectional schematic diagram of RRAM device integrated on a 180-nm CMOS substrate, leaving out the lower metal layers for better visibility (a) and the SEM image of 100 x 100 nm^2 nano-crossbar RRAM device fabricated on the CMOS substrate (b). (c), (d) Both RRAM device stacks are shown with respective thickness of the layer. Additionally, the top electrode (TE) and bottom electrode (BE) assignment for the electrical characterization is displayed.

III. Result and Discussion

The electrical characterizations of the 1T-1R structures were carried out using Keithley 4200 SCS. Figure 2 (a) shows the layout of the 1T-1R structure used for electrical measurements. Measurements applied to the RRAM TE (e.g. electroforming) are assigned a positive polarity in all following figures showing current-voltage (*I-V*) characteristics, while measurements applied to the transistor source (e.g. RESET) are assigned a negative polarity. The voltages applied to the 1T-1R structure in both configurations are displayed in the schematics in Figs. 2(b) & (c). In both configurations, a voltage sweep is either applied at the TE or Source terminal while keeping the Source or TE and the Bulk terminal at ground level. The applied Gate voltage (V_G=const.) determines the compliance current (I_{CC}).

Figure 3 shows the the median value of the forming voltage for the single layer (W/Ta_2O_5) and the bilayer stacks (TaO_x/HfO_2). For each type, 25-39 devices were measured. Figure 3(b) shows the cumulative probability of the forming voltage, indicating a lower variability of the forming voltage for the bilayer TaO_x/HfO_2 devices.

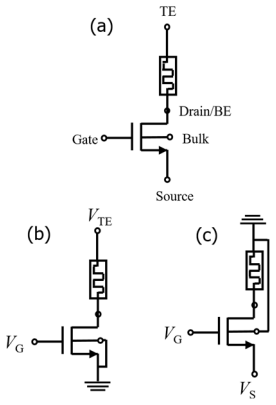

Fig.2 (a) Schematic diagram of electrical setup for 1T-1R device, including transistor and RRAM terminals. The RRAM BE is connected to the transistor Drain terminal. (b) Configuration for positive voltage sweeps (applied to the TE). (c) Configuration for negative voltage sweeps (applied to the Source).

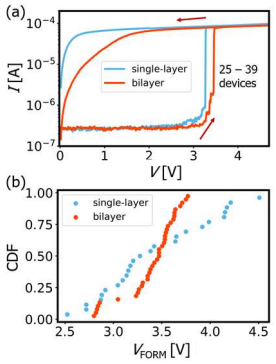

Fig. 3 (a) Median Forming *I-V* characteristics and (b) Cumulative distribution function of the forming voltage for single layer TaO_x/W and bilayer TaO_x/HfO_2 RRAM. 25-39 devices were measured for each case.

Figure 4 shows the *I-V* characteristics of the single layer W/Ta_2O_5 and bilayer TaO_x/HfO_2 RRAM in 1T-1R configuration for 100 cycles. It should be noted that the single layer W/Ta_2O_5 devices show counter-clockwise switching, whereas the bilayer TaO_x/HfO_2 devices show clockwise switching, which is happening within the TaO_x at the TaO_x/CF interface [13, 14]. Figures 4 (a) and (d) graphically display the switching mechanisms for single layer (counter-clockwise) and bilayer devices (clockwise), respectively. Counter-clockwise switching in single layer W/Ta_2O_5 devices is based on rupture/reconnection of the CF (Figure 4 (a)). As suggested by [13, 14], a dome-shaped region above the CF might result in the observed clockwise switching in bilayer TaO_x/HfO_2 devices, as illustrated in Fig. 4(d). In these works, the device properties enabling clockwise switching in TaO_x/HfO_2-based RRAM devices are discussed in more detail. Figures 4(c) and (f) show the cumulative probability of LRS and HRS for both type of devices. It is evident that the bilayer TaO_x/HfO_2 RRAM device shows lower C2C variability than its counterpart: the W/Ta_2O_5 stack. The coefficient of variation (CoV) for C2C switching is shown in Table 1. The CoV for LRS and HRS is calculated by dividing the standard deviation (StD) by the mean value of the distribution. For both LRS and

HRS, the bilayer (TaO_x/HfO_2) RRAM devices show the lower C2C variation.

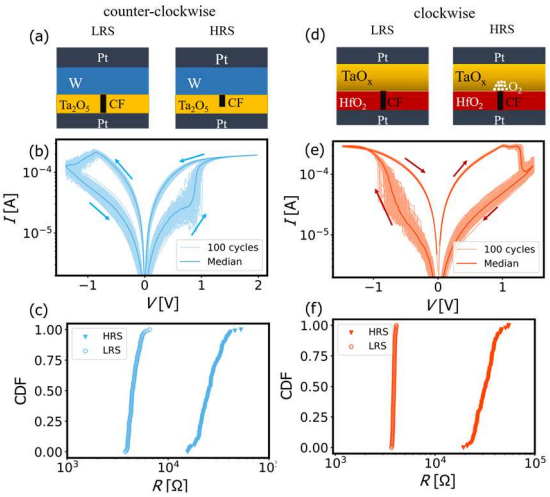

Fig. 4. Schematics illustrating the difference between LRS and HRS configuration for (a) counter-clockwise switching direction and (d) clockwise switching direction. (b), (c) *I-V* characteristics and cumulative probability of single layer W/Ta_2O_5 RRAM devices; $V_{SET,stop} = V_{TE} = 2$ V, $V_{gate,SET} = 1.2$ V, $V_{RESET,stop} = V_{Source} = 1.3$ V, $V_{gate,RESET} = 4$ V. (e), (f) *I-V* characteristics and cumulative probability of bilayer TaO_x/HfO_2 RRAM devices; $V_{SET,stop} = V_{Source} = 1.5$ V, $V_{gate,SET} = 2.9$ V, $V_{RESET,stop} = V_{TE} = 1.5$ V, $V_{gate,RESET} = 4$ V Each type of device was measured for 100 cycles. HRS and LRS values are extracted from the *I-V* characteristic of each cycle.

The lower variability in the bilayer (TaO_x/HfO_2) devices can be attributed to the fact that the switching process in these bilayer devices takes place at the TaO_x/CF interface. This type of switching exhibits a reduced non-linearity in the switching kinetics [14] compared to the kinetics of purely filamentary switching happening in single layer devices. As a result of the reduced non-linearity in the switching kinetics, a lower stochasticity in the resistance states (HRS & LRS) is observed in the bilayer devices.

Table 1. Coefficient of variation (CoV) for C2C switching variability. CoV = StD/Mean.

RRAM device	CoV HRS	CoV LRS	Off/On
Single layer, W/Ta_2O_5	0.34	0.14	7.43
Bilayer, TaO_x/HfO_2	0.30	0.080	6.53

IV. 3-Bit Multilevel Switching

To achieve higher data density for storage applications in RRAMs is to enable more than two bits to be stored in a single RRAM device. Many authors have demonstrated 2-bit and 3-bit MLC in 1T-1R and passive crossbar arrays [17, 18] by using I_{CC} control and varying V_{RESET}.

We have tested both types of RRAM devices with the I_{CC} control and varying V_{RESET}. The HRS and LRS values of each dataset in the 3-bit MLC operation are extracted from the *I-V* characteristics.

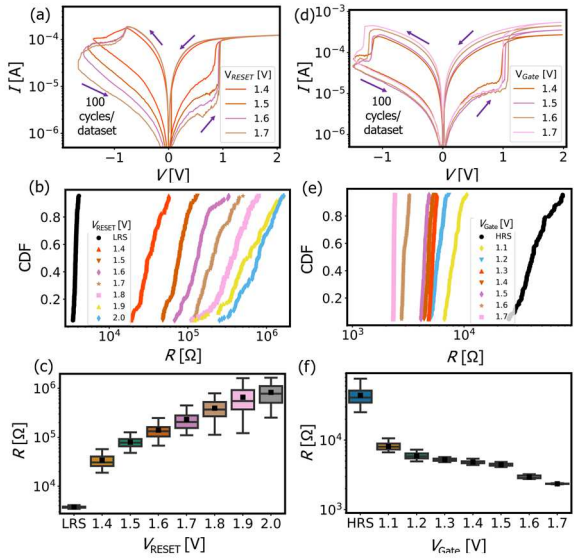

Fig. 5. 3-Bit MLC in single layer W/Ta_2O_5 1T-1R RRAM devices (a) median *I-V* characteristics, (b), (c) resistance state distributions for different V_{RESET}, switching parameters: $V_{SET,stop} = V_{TE} = 2$ V, $V_{gate,SET} = 1.2$ V, $V_{RESET,stop} = V_{Source}$ varies, $V_{gate,RESET} = 4$ V. 3-Bit MLC (d) median *I-V* characteristics, (e), (f) resistance state distributions for different I_{CC}, switching parameters: $V_{SET,stop} = V_{TE} = 2$ V, $V_{gate,SET}$ varies, $V_{RESET,stop} = V_{Source} = 1.3$ V, $V_{gate,RESET} = 4$ V. The I_{CC} dependent MLC shows lower variability among the different resistance states.

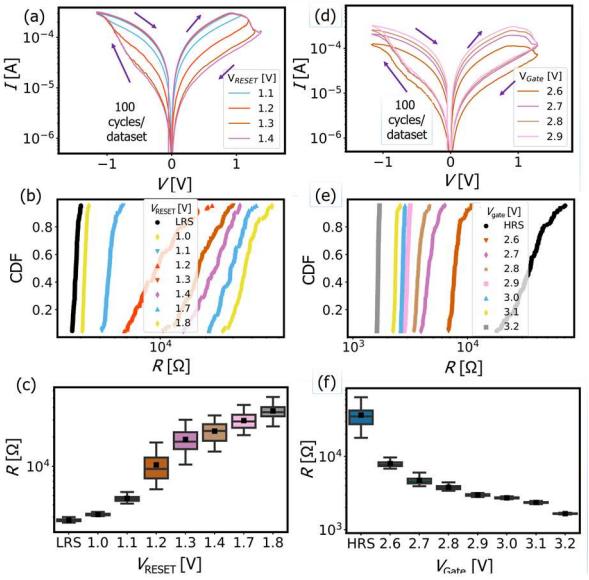

Fig. 6. 3-Bit MLC in bilayer layer TaO_x/HfO_2 1T-1R RRAM devices (a) median *I-V* characteristics, (b) (c) resistance state distributions for different V_{RESET}, switching parameters: $V_{SET,stop} = V_{Source} = 1.5$ V, $V_{gate,SET} = 2.9$ V, $V_{RESET,stop} = V_{TE}$ varies, $V_{gate,RESET} = 4$ V. 3-Bit MLC (d) median *I-V* characteristics, (e), (f) resistance state distributions for different I_{CC},,switching parameters: $V_{SET,stop} = V_{Source} = 1.5$ V, $V_{gate,SET}$ varies, $V_{RESET,stop} = V_{TE} = 1.3$ V, $V_{gate,RESET} = 4$ V. The I_{CC} dependent MLC shows lower variability among the different resistance states.

Figure 5 shows the 3-bit MLC operation in single layer W/Ta_2O_5 RRAM in 1T-1R configuration. Figures 5(a-c) & (d-f) show the MLC operation with varying the V_{RESET} and different I_{CC} control, respectively. It is evident that varying the V_{RESET}

introduces more variability than the I_{CC} control method. As a result, an overlapping of different resistance states is observed for the varying the V_{RESET} method. Figure 6 shows the 3-bit MLC operation in bilayer TaO_x/HfO_2 RRAM for 1T-1R configuration. Figures 6(a-c) & (d-f) show the MLC operation with varying the V_{RESET} and different I_{CC} control, respectively. Similar trends, i.e., a lower variability with the I_{CC} control method is also observed in the bilayer RRAM devices.

When comparing the different RRAM device stacks for the varying V_{RESET} method, a noticeable lower variability is observed for bilayer TaO_x/HfO_2 devices in comparison to single layer W/Ta_2O_5 RRAM devices. The CoV for both RRAM stacks are tabulated in Table 2.

Table 2. Comparison of maximum resistance state variability during 3-bit multilevel switching

RRAM device	CoV I_{CC}	CoV V_{RESET}
Single layer W/Ta_2O_5	≤ 0.27	≤ 0.68
Bilayer TaO_x/HfO_2	≤ 0.27	≤ 0.44

V. Conclusions

In this study, we have integrated single layer W/Ta_2O_5 and bilayer TaO_x/HfO_2 RRAM on 180-nm CMOS substrates and demonstrated that C2C variability in the filamentary switching can be reduced by introducing the bilayer device stack. When compared to single layer W/Ta_2O_5, the bilayer RRAM shows lower variability (D2D) during the forming process but also lower C2C variability during the switching. As a result, we were able to demonstrate 3-bit MLC operation with 8 distinct resistance states in the bilayer TaO_x/HfO_2 RRAM devices. Multistate devices enable novel in-memory applications, e.g. ternary computation, in which the computational complexity as well as the number of devices is reduced compared to binary computation [17]. We believe that these results could pave a way for designing a high performing RRAM device stack for high data density applications.

VI. Acknowledgement

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