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ABSTRACT

Resistive switching devices and other components with negative differential resistance (NDR) are emerging as possible electronic constituents of next-generation computing architectures. Due to the exhibited NDR effects, switching operations are strongly affected by the presence of resistance in series with the memory cell. Experimental measurements useful in the development of these devices use a deliberate addition of series resistance, which can be done either by integrating resistors on-chip or by connecting external components to the wafer probing system. The former approach is considered inflexible because the resistance value attached to a given device cannot be changed or removed, while the latter approach tends to create parasitic effects that impact controllability and interfere with measurements. In this work, we introduce a circuit design for flexible characterization of two-terminal nanodevices that provides a programmatically adjustable external series resistance while maintaining low parasitic capacitance. Experimental demonstrations show the impact of the series resistance on NDR and resistive switching measurements.

I. INTRODUCTION

Increasing research and development efforts aim to produce new types of scalable two-terminal nanodevices suitable for storing and processing information in both traditional and neuromorphic computing architectures.[1–3] Emerging devices are often based on incompletely understood mechanisms and may exhibit strong non-linearity, negative differential resistance (NDR), oscillations, stochasticity, and memory effects. In assessing the electrical capabilities of resistive switching devices such as ReRAM,[4] it is important to consider not only the device material properties but also the effects of feedback, runaway, excess electrical stresses, and the general role of the driving circuitry on measurement data.

Electrical measurements of patterned devices are inevitably carried out in the presence of resistance in series with the active material volume of the cell. This series resistance, commonly of unknown value,[5,6] may originate from a combination of the electrode leads, inactive layers of the material stack, or the triode region of a series FET current limiter. Internal and external series resistance adds current–voltage feedback to the system that affects stability and influences the operational behavior in important ways. Modification of switching speeds, threshold voltage/currents, and the range of achievable resistance states have all been observed and discussed theoretically.[7–12]

Series resistance is often intentionally placed to play the necessary role of an energy limiting mechanism, where its value can mean the difference between functioning and non-functioning devices. As an experimental technique, it is useful to be able to place different resistance values in series with the device under test (DUT) and examine the effect on switching processes. Here, the linearity of the resistive load is a convenient property for mathematical modeling. The circuit response of the simple two-element series configuration (2R) is easily predictable through load line analysis in the ideal case and is also straightforward to treat analytically in the presence of commonly encountered parasitics.

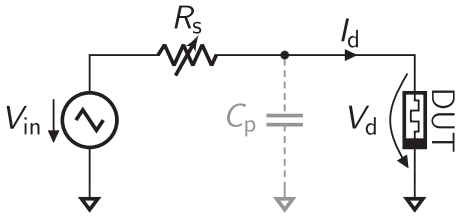

FIG. 1. A simple circuit configuration for device characterization uses a waveform generator and an external resistance in series with the DUT. In practice, the effect of the parasitic capacitance in parallel with the device requires careful attention.

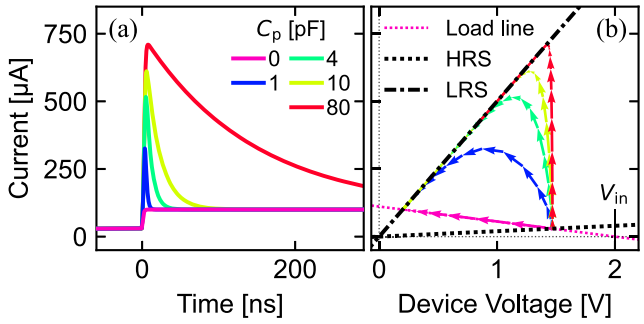

FIG. 2. Simulations [using Eq. (1)] of I_d and V_d transients following a rapid resistance transition of the DUT with V_{in} = 2 V and different values of C_p. Subplot (a) shows I_d vs T, while (b) shows I_d vs V_d of the same simulations. The DUT resistance value is assumed to change exponentially in time from a high resistance state (HRS) of 50 kΩ to a low resistance state (LRS) of 2 kΩ with a time constant of 1 ns. During and following the transition, the device is subjected to excess currents relative to the load line, an effect that is reduced by using lower C_p values.

Another advantage of the 2R configuration is the ease of implementation relative to the integration of active FET devices on a test chip, with the latter requiring substantial fabrication cycle time. However, integrating calibrated series resistances on-chip is inflexible because each cell is attached to a single static resistance value that cannot be changed or removed. Scenarios often arise that give good reason to alter or remove the series resistance *in situ*. Notably, devices possessing steady states with S-type or N-type NDR have different criteria for stable characterization, and both types are presented in the SET and RESET processes of ReRAM, respectively.[7] This imposes different requirements for the series resistance value even within a single switching cycle.

Where an adjustable series resistance is required, it must be implemented externally to the wafer. The main practical challenge associated with this is that the parasitic capacitance C_p at the node shared with the DUT is highly detrimental and difficult to avoid (Fig. 1). This stray capacitance slows down the dynamic response of the circuit, degrading the ability to control and to measure the voltage and the current experienced by the active cell volume vs time. Coupled with rapid conductance transitions of the DUT, harmful overshoot transients are generated that strongly impact the observed switching behavior and can cause irreversible damage.[13–16]

While discrete resistors are a common external solution, their use entails manually switching between resistance values where required. However, the stochastic nature of resistive switching cells is such that they benefit greatly from a statistical treatment using automated measurements with programmable parameters. In this work, we present an external circuit design providing an adjustable linear series resistance for flexible wafer-level device characterization. The circuit, based on a digital potentiometer (digipot) chip, is remotely programmable over the universal serial bus (USB) between 528 resistance levels. Importantly, the voltage signal at the low-capacitance DUT node is directly amplified for synchronous measurement with the DUT current with a bandwidth over 200 MHz. We demonstrate the circuit operation for the automated characterization of NDR devices and the cycling of bipolar ReRAM cells with high-speed voltage sweeps.

II. DESIGN

Applying Kirchhoff's current law, the dynamical equation governing the time evolution of the device voltage in the circuit of Fig. 1 is

$$C_p \frac{dV_d(t)}{dt} = \frac{V_{in}(t) - V_d(t)}{R_s} - I_d(t, \ldots), \tag{1}$$

where t is time and I_d, in general, depends on V_d and other internal state variables of the DUT. Possible steady-state solutions lie on the V_d-nullcline,

$$V_d = V_{in} - I_d R_s, \tag{2}$$

also known as the load line. For fast conductance switching events that are common in the targeted material systems, transient deviations from the load line occur as seen in the simplified situation of Fig. 2. During such transients, the excess energy delivered to the DUT due to capacitive discharge is significant and can strongly influence the end result of the switching process.

While the potential for overshooting transients is unavoidable in the context of a passive feedback arrangement, it is important that they are controlled to the extent possible and accurately measured when they occur. The only way that overshoots can be reduced in the discussed configuration is by minimizing the value of C_p. Practically, this means that a coaxial cable, acting approximately as a parasitic capacitance of 100 pF/m, cannot be used to connect R_s to the DUT. The series resistance should rather be placed as close as possible to the DUT, with the components carefully selected and the printed circuit board (PCB) layout designed for low contribution to the total C_p.

High-fidelity current measurements can be achieved by amplification of the voltage across a ground-referenced shunt termination following transmission over a coaxial line. Using this type of current measurement, positioning the DUT (rather than R_s) adjacent to the shunt is generally preferred because it avoids low pass filtering of the I_d signal, allowing measurement of I_d at a high bandwidth that is independent of the resistance state of the device. With prior knowledge of R_s, Eq. (2) is often used to calculate V_d from a measurement of I_d and V_{in}, but there are several drawbacks associated with this method. One is the inaccuracy that comes from neglecting the capacitive currents of the left-hand side of Eq. (1). Another problem is measurement noise introduced by the $I_d R_s$ term, as the

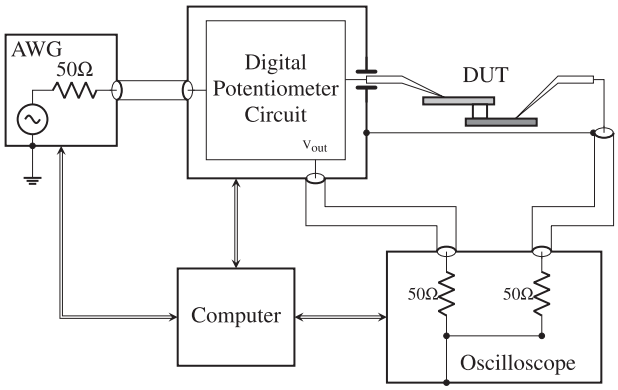

FIG. 3. Schematic depiction of the overall measurement setup. An arbitrary waveform generator (AWG) produces the driving signal $V_{in}(t)$, and the resulting current is sampled after the right electrode via the 50 Ω shunt of the oscilloscope input. A second oscilloscope channel simultaneously captures the amplified voltage at the left electrode. A ground jumper provides a low inductance return path and reduces RF interference. All instruments are under computer control.

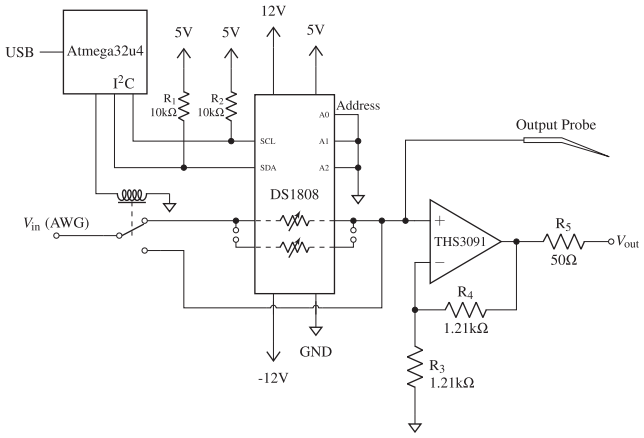

FIG. 4. Simplified schematic of the digipot measurement circuit. An Atmega32u4 microcontroller USB-serial interface communicates to the DS1808 digipot via an I^2C bus. An SPDT reed relay can be actuated in order to bypass the digipot and make a direct connection between input and output. The voltage at the output is amplified by a THS3091 non-inverting follower.

small I_d signal with high relative error is multiplied by a potentially large R_s value. It is, therefore, advantageous to directly amplify the voltage at the DUT electrode rather than attempting to calculate it from other measured signals.

Following these considerations, the basic intended configuration of external instruments and the designed circuit can be seen in Fig. 3. If sufficient resolution is not obtained by sampling the current with a bare oscilloscope input, additional voltage amplification should be placed at the termination, where the use of several output stages is beneficial for the dynamic range. Note that the length of the coaxial lines for the DUT voltage and current sampling should be matched so that post-processing is not needed for signal synchronization.

A commercial integrated circuit, the DS1808 digipot from Maxim Integrated, was chosen as the central component to control the series resistance, R_s. Internally, it contains two separate potentiometers, each consisting of a chain of 32 resistors whose junctions can be connected to a "wiper" output via a set of CMOS transmission gates (analog switches). For each potentiometer, there are 32 available resistance settings spaced logarithmically (piecewise) from ~300 Ω to ~45 kΩ. According to the published specifications, the DS1808 has a maximum parasitic capacitance of 10 pF and a maximum voltage range of ±12 V.[17]

To increase the coverage of R_s values, the PCB is routed in a way that allows the connection of both potentiometers either in series or in parallel by connecting or opening solder jumper pads. While a connection to a single potentiometer remains a possibility, the number of unique settings is increased to 528 between 600 Ω and 90 kΩ for the series combination and between 150 Ω and 22.5 kΩ for the parallel combination. Because a low resistance setting below 300 Ω is not provided by the digipots, a reed switch was also included on the PCB to add an option to short the input directly to the output.

To amplify the output voltage, the THS3091 current-feedback operational amplifier from Texas Instruments was used in a non-inverting configuration. This device features low distortion,

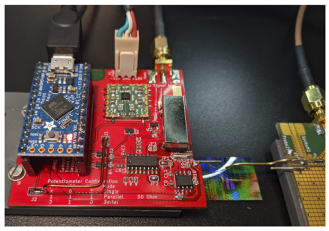

FIG. 5. A photograph of the probing PCB contacting a test chip. A non-coaxial BeCu probe tip is soldered directly to the output of the main PCB (red), which uses SMA connectors for additional input and output signals. An elevated PCB (blue) contains the microcontroller USB interface (Adafruit ItsyBitsy 32u4). A square PCB module (green) functions as a low noise dual voltage regulator providing ±12 V to the system. The right probe is directly connected to a 50 Ω oscilloscope input.

low noise, a bandwidth of 210 MHz, and a slew rate of 7300 V/μs while adding only 0.1 pF parasitic capacitance.[18]

All on-board settings are controlled via an Atmega32u4 microcontroller programmed as a USB serial interface to the PC. Control of the R_s value is accessible using any programming language able to open a serial COM connection and send a simple command composed of three integer values corresponding to the wiper positions and the state of the bypass relay. The total time from issuing a serial command to R_s reaching a new value is limited by USB/I^2C communication and is typically less than 300 μs. The overall circuit design is visualized in the block diagram of Fig. 4, and a corresponding fabricated PCB is pictured in Fig. 5.

III. MEASUREMENTS

For quasi-static measurements of classical NDR materials using a series resistance, saddle-node bifurcations can occur and separate the NDR characteristic into stable and unstable regions. The range

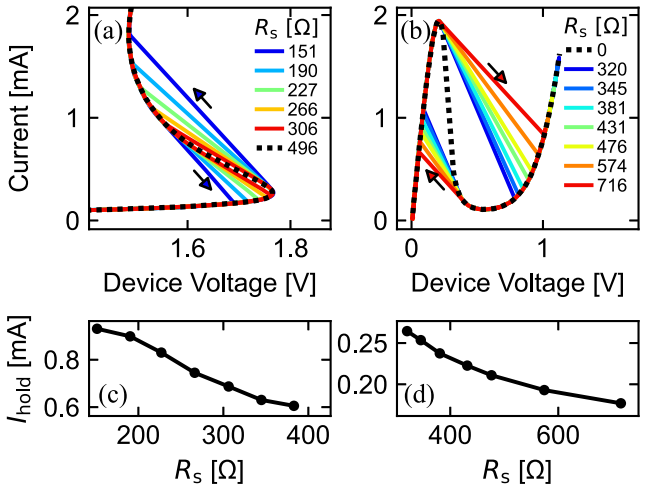

FIG. 6. Voltage sweeping measurements of NDR devices using different resistance settings. (a) 90 × 500 × 500 nm^3 S-type VCrOx device,[20] stabilized for R_s > 400 Ω. (b) N-type Ga–As tunnel diode 3µ306E, stabilized for R_s = 0 Ω. The dependence of the holding currents I_{hold} on R_s is shown in (c) for the S-type data and (d) for the N-type data.

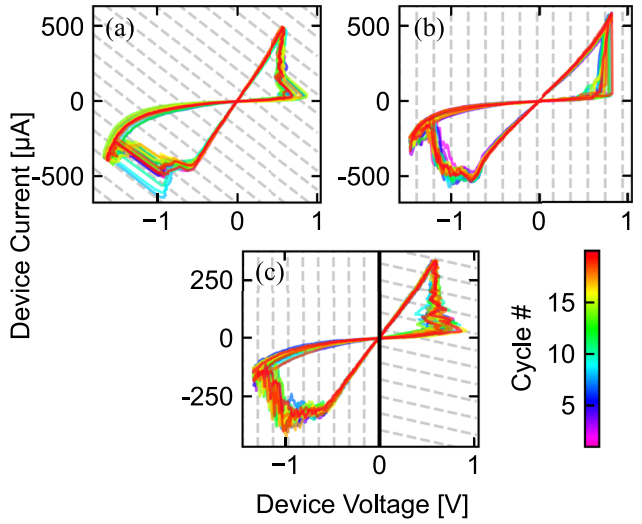

FIG. 8. Cycling measurements of a 100-nm ReRAM device[21] using bipolar triangular voltage sweeps with 1 ms duration. Each subplot contains 20 consecutive switching cycles differentiated by color. The value of added series resistance is indicated by the dashed lines with gradient $-1/R_s$. Transition behavior differs considerably when using (a) 2.4 kΩ, (b) 0 Ω, and (c) 11 kΩ for positive polarity and 0 Ω for negative polarity.

of the unstable region is determined by the value of the series resistor, with the bifurcations occurring where the derivative of the NDR curve voltage with respect to current crosses $-R_s$. While sweeping voltage, sudden current jumps are observed for sufficiently low values of R_s in S-type NDR [Fig. 6(a)] and for sufficiently high values of R_s in N-type NDR [Fig. 6(b)]. In this way, NDR curves are the device characteristic underlying the phenomenon of threshold switching, and they contain important information such as the threshold/hold voltages and currents that would be observed in different circuits.[19] The adaptable R_s value provided by the discussed circuitry allows control of the conditions under which both types of NDR curves can be fully characterized.

Where the material mechanism of NDR is dynamic and reversible, the presence of C_p makes the measurement circuit prone to transient oscillations, and stable oscillatory limit cycles can also occur. Useful in these cases, the presented circuit is able to capture high-speed transients and accurately project them onto the device (Id,Vd) plane (Fig. 7). These data can be used for device modeling and circuit simulations, each relevant, for example, in the ongoing investigations of coupled oscillatory devices in neuromorphic systems.

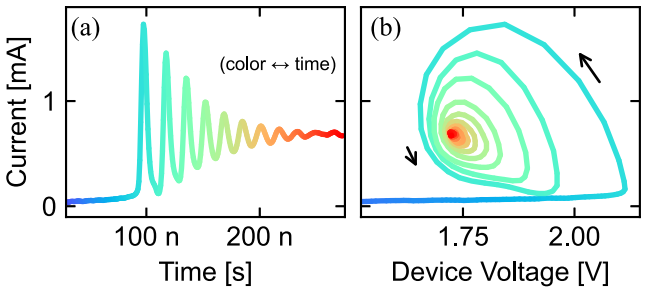

FIG. 7. Oscillations (57 MHz) occurring in a 30 × 250 × 250 nm^3 S-type VCrOx NDR device[20] following a square voltage pulse V_{in} = 0 V → 2.5 V using R_s = 1083 Ω. With the line color mapped to time of measurement, (a) shows I_d vs t of the transient, and (b) shows the trajectory of the same data on the (Id,Vd) plane.

In ReRAM devices, NDR behavior is mediated by a combination of Joule heating and migration of point defects in the oxide material that locally increases its conductivity.[4] Altering the R_s value allows these transitions to be probed in different ways, as seen in the example measurements of Fig. 8. In analogy to the NDR measurements of Fig. 6, a fixed value of R_s can result in sudden and unstable transitions for one or both of the SET or RESET processes. By switching the value of R_s during the measurement [Fig. 8(c)], it is observed that runaway load line transitions can be suppressed by the appropriate selection of external feedback.

IV. CONCLUSION

When performing electrical measurements of resistive switching systems, the use of well-understood circuitry is critical for realistic evaluation. With isolated devices vulnerable to runaway transitions, a series resistance circuit provides a simple means for control and tractable analysis of switching processes. In this context, parasitic capacitance is an important factor, and the values of both R_s and C_p lead to different switching outcomes, in general. We have presented a circuit design for the synchronized measurement of switching trajectories at high speed while using a programmable linear series resistance with low parasitic capacitance. Using this

circuit, possible implications of the physical processes that accompany runaway transitions can be conveniently investigated, yielding insights into how optimal control can eventually be achieved.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

Data sharing is not applicable as no new data were generated in this study.

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