Exploring Multi-Valued Logic and its Application in Emerging Post-CMOS Technologies

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ABSTRACT

Multi-valued logic (MVL), characterized by more than two possible logic states, presents distinct advantages compared to conventional Boolean logic. Novel post-CMOS technologies, particularly memristive and bio-sensitive devices, exhibit compelling attributes that make them promising candidates for realizing MVL computing components. To assess the viability of these devices, we delve into key aspects of Memristive and ISFETs, including their state transition dynamics, multi-level functionality, and compatibility with CMOS manufacturing processes. Through this investigation, we successfully demonstrate the practical implementation of ternary arithmetic MVL gates utilizing memristive and bio-sensitive devices. Our findings affirm that these innovative devices hold the potential to serve as MVL computing elements effectively.

KEYWORDS

Multi-valued logic computing, post-CMOS technologies, Resistive RAM, ISFET

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1 INTRODUCTION

With the approaching end of CMOS downscaling, computer circuits do not meet the application demands in terms of energy consumption [4] and reliability [31]. Today's computer architecture also suffers from the von Neumann bottleneck due to the physical separation of the memory and the central processing unit [4]. These challenges have forced computer architects to look beyond the traditional solutions for future-generation computing platforms.

To alleviate the von Neumann bottleneck and provide solutions for high-speed operations, multi-valued logic (MVL) is a promising substitute over conventional Boolean logic. MVL offers compelling advantages over Boolean logic, such as high-speed arithmetic operations, low power consumption circuits [3], and hardware intellectual property protection [20]. For arithmetic operations, MVL requires fewer components and interconnects compared to its Boolean logic counterpart. Therefore, it reduces the on-chip interconnection area and energy consumption. It has been shown that replacing binary interconnections with MVL provides a 29-30% reduction in energy consumption for on-chip and 55-62% for off-chip interconnections [33].

Due to the advantages of MVL-based circuits, the scientific community has started exploring different technologies that can support MVL [30]. In the past, researchers compared the binary and MVL-based integrated circuits according to very large-scale integration criteria such that MVL circuits were only restricted to small niches [9, 29]. Here, metal-oxide-semiconductor field-effect transistors (MOSFETs) and bipolar junction transistors in current mode (CM) and voltage mode (VM) were used to implement the MVL-based circuits [32]. The circuits designed on CM and VM had limited use as the MVL implementation required more transistors than binary logic-based circuits.

Recently, memristive devices or memristors [28] and bio-sensitive devices [18] are attracting focus as potential MVL elements of future computing platforms. The logic states of memristive devices are stored in the form of resistances. The device's resistive states are switched between a high resistive state (HRS) and a low resistive state (LRS) with appropriate voltage bias. The state-switching

dynamics of memristive devices allow for the exploitation of reliable MVL characteristics and the opportunity to perform logic operations. This dual functionality of memristive platforms enables a novel path towards computation-in-memory (CIM) architectures, overcoming the von Neumann bottleneck. Next, we have bio-sensitive devices realized as classical ion-sensitive field-effect transistors (ISFETs) operated in an electrolyte gate, where switching operation between logic states can be performed via manipulating molecular interactions at the bio-recognition layer. We believe that the memristive and bio-sensitive devices (BioFETs) based on redox-based resistive random access memory (ReRAM) [26] and ISFET, respectively, are promising as MVL computing elements.

MVL has various subset logics. One of them is ternary logic, which has three logic states. These states can be represented by notations such as voltage levels, symbols, balanced and unbalanced ternary digits (trit) (see Table 1). Among various approaches for ternary logic-based circuits, ternary arithmetic circuits have also been implemented based on ReRAM devices [26]. The ternary primitive logic functions AND, OR, and NOT, combinational gates: NAND, NOR, XOR, and XNOR, and data handling gates: MAX and MIN, have been demonstrated using the Memristor-CMOS logic family [25].

Despite the advantages of MVL, present mainstream computing heavily focuses on Boolean logic-based implementations. In this context, we use TaO_x-based ReRAMs and silicon-based ISFETs for exploring the potential of memristive and BioFET technologies [10, 18], respectively, as MVL elements and documents the following contributions:

- The exploration of state switching dynamics of memristive and bio-sensitive devices for the support of MVL operations.
- The exploration of the possible number of logic states in these devices by implementing MVL-based applications.
- Finally, the investigation on the compatibility of these devices with standard CMOS technology.

The rest of the paper is structured as follows. Section II reviews the existing and related work on memristive and BioFETs. Section III provides the details of MVL behaviors of memristive devices. Section IV provides behavior analysis and discussion on BioFETs. Finally, Section V concludes and provides an outlook of this work.

2 RELATED WORK

Some of the early works towards implementation of MVL focused on Si-CMOS and carbon nanotube (CNT) based devices as gates to design arithmetic circuits [19, 24]. As per the analysis in [29], the CMOS-based MVL implementations require more transistors than Boolean logic-based implementations. The implementation presented in [19] requires large resistive loads, which are hard to integrate and waste large chip areas. Although a complementary CNTFET network presented in [14] overcomes the problem of large resistive load, it still requires six CNTFETs to implement a standard ternary inverter.

Table 1: Ternary logic representations: Voltage levels, Logic Symbols, Balanced and unbalanced trits

Voltage level	Logic symbol	Balanced trits	Unbalanced trits
V_{EE} (-2.5V)	F (False)	-1	0
0	0 (Unknown)	0	1
V_{DD} (+2.5V)	T (True)	+1	2

ReRAM devices have emerged as a viable solution to MVL, where the device properties allow the exploitation of the multi-valued behavior. The implementation of ternary arithmetic circuits and fuzzy logic realization has been demonstrated in [5, 26]. Even though these implementations provide proof of concept for MVL realization, a detailed analysis of these devices is required. Apart from the ReRAM device as an MVL element, BioFETs presented in [18] discuss specific recognition of biomolecules such as deoxyribonucleic acid sequences, which is evidently a multi-valued operation.

This work explores ReRAM and bio-sensitive devices for a multi-valued computing element by analyzing different properties such as switching dynamics, multi-level capabilities, and CMOS compatibility. We examine our findings by implementing multi-valued arithmetic circuits and MVL inverted gates on ReRAM and ISFET devices, respectively.

3 REDOX-BASED RESISTIVE SWITCHING DEVICES

In the group of memristive devices, redox-based memristive devices stand out due to their possibility for low power consumption, multilevel capability and dense integration [8]. In addition, the opportunity to directly perform Boolean logic operations with such memristive devices, the 'stateful logic', seems a promising path towards CIM [5, 11, 27]. Their multilevel capabilities were recently demonstrated by utilizing a multilevel memristive device based on TaO_x for the implementation of a ternary Łukasiewicz logic and fuzzy logic circuit as well as a ternary adder circuit [6, 26]. Logic that uses more than two truth values reduces the number of devices needed for a certain operation, increasing the integration density. This work showcases an adder circuit based on ReRAM devices with seven stable, addressable resistance states [22]. We show the experimental device characterization as well as a proof-of-concept measurement. Using the physics-based compact model JART VCM v1b model [7, 10], we can accurately describe the measurements and scale up the proposed adder circuit to a 41 trit addition (roughly equivalent to 64-bit) using a select device in series to a memristive device (1S1R).

3.1 Adder concept and experimental results

For the realization of the ternary adder concept proposed in [26], a 1x3 crossbar array with 5 µm x 5 µm-sized junctions has been fabricated. The shared bottom electrode is made of 5 nm-thick Ti and 30 nm-thick Pt, which are deposited sequentially by sputtering on top of a 430 nm-thick thermally grown SiO_2 layer. A photolithography and dry etch processes are applied to pattern the bottom electrode. Then, a 7.0 nm-thick TaO_x layer is deposited by reactive sputtering under process gas mixture of Ar (23%) and oxygen (7%) with the RF power of 116 W at the chamber pressure of 2.3×10^{-2} mbar. Without breaking the vacuum, 13 nm tungsten (W), and 25 nm Platinum (Pt) are deposited consecutively. Finally, the top electrode (TE) is patterned using photolithography and reactive ion etching. It has been shown that these devices can store 7 different resistance states [26]. To program the different resistance states, the gradual RESET transition is exploited. After programming the devices to a low resistance state, a RESET pulse with a defined voltage amplitude is applied to program the device to a HRS. By

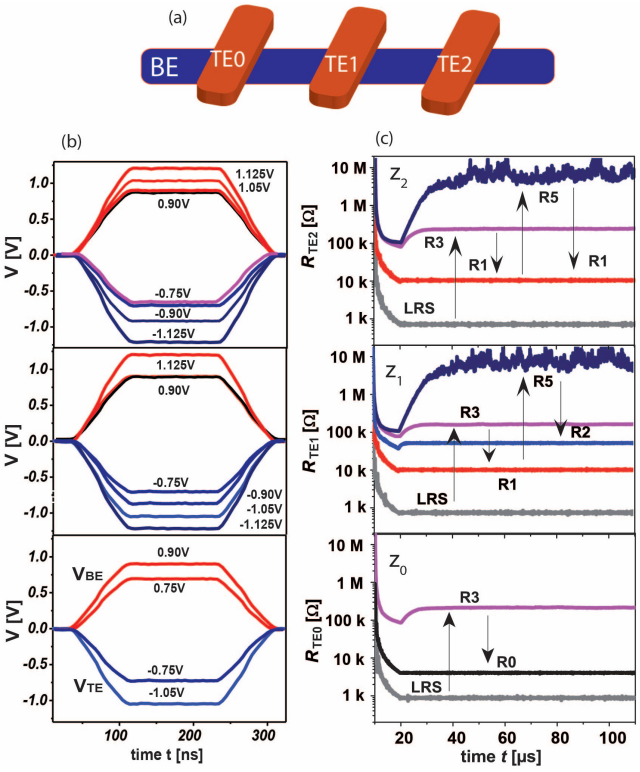

Figure 1: (a) Schematic diagram of 1x3 memristor crossbar array. (b) Demonstration of logic functionality, with the logic operands p and q applied to TE and BE, respectively. An offset voltage (V_{offset}) ensures even voltage steps in operands, resulting in different resistance states depending on the pulse height. (c) Ternary adder proof of concept. In this example, p=21(2·3 + 1·1 = 7) and q=22 (2·3 + 2·1 = 8) are used for the calculation. The final resistive states are as follows: z2=R1, z1=R2, and z0=R0, corresponding to 1·9 + 2·3 + 0·1 = 15.

increasing the device voltage magnitude in 0.15 V steps from 1.5 V to 2.25 V, the 6 resistance states R_0 to R_5 are achieved. If a lower voltage is applied, the device remains in the LRS.

The ternary adder relies on implementing a modulo sum operation. Thus, while 3 states are enough to represent a trit, 2x3 = 6 states are required to enable a proper modulo operation. The levels R_0, R_1, and R_2 represent the logic levels 0, 1, and 2, respectively. The operands of the operation are encoded as voltage levels ($V_{\mathrm{op,\,i}}$), while the result of the operation is directly stored in the memory array. Here 0 V, 0.15 V and 0.3 V represent the logic levels 0, 1 and 2, respectively.

To implement the Carry and Sum operation, the operands 1 and 2 are applied to the top electrode (TE) and the bottom electrode (BE), respectively, according to $V_{\mathrm{BE}} = V_{\mathrm{offset}} + V_{\mathrm{op,\,1}}$, and $V_{\mathrm{TE}} = -(V_{\mathrm{offset}} + V_{\mathrm{op,\,2}})$. The offset voltage is chosen in such a way that the device voltage $V_{\mathrm{device}} = V_{\mathrm{TE}} - V_{\mathrm{BE}}$ resets the device to the intended resistance state. Moreover, the offset voltage of the current depends on the carry bit of the previous state. If the carry bit is zero (one), $V_{\mathrm{offset}} = 0.75$ V (0.825 V) is used. This means that the applied device voltage is increased by an increment of 0.15 V, which is the physical equivalent of adding a logic 1. After the programming step, a read operation is performed. The read resistance is compared to R_2 to implement the carry operation. If $R > R_2$ ($R \leq R_2$), the carry bit is one (zero). In contrast, the resistance is compared to different resistance levels for the sum operation. If $R \leq R_2$, the final sum bit is already programmed. If $R = R_3$, $R = R_4$ or R_5, the resistance has to be mapped to R_0, R_1, or R_2, respectively, by a re-programming step. Note that before all programming steps in the RESET direction, the device is set to the LRS to exploit the tunability of the RESET.

As a proof-of-concept, Fig. 1 shows the addition of the two ternary numbers $\mathbf{p} = p_1p_0 = 21(\widehat{=}7)$ and $\mathbf{q} = q_1q_0 = 22(\widehat{=}8)$ on the fabricated 3x1 crossbar array. As we have two trit numbers, we need three devices z_2, z_1 and z_0 to perform the addition. All devices are initialized to LRS. Then, p_0 is applied to all TEs, while q_0 is applied to the common BE. While this operation resembles the sum operation on device z_0, the carry c_0 of the least significant bit is calculated in device z_2 and z_1. The result of this operation is then stored in the next programming cycle. As 2+1 gives 3 and results in R_3, device z_0 needs to be re-programmed to R_0 to store the final sum bit s_0, i.e., $V_{\mathrm{op,\,2}} = 0$ and $V_{\mathrm{op,\,1}} = 0$. The carry operation on devices z_1 and z_2 can be performed in parallel, by setting $V_{\mathrm{op,\,2}} = 0.15\,V$. Now, the final sum bit s_0 is already stored in z_0 and thus V_{TE0} is set to 0 for all following steps. As a common bottom electrode is used, a voltage will drop over the device z_0, but it will be too low to change its state. Next, the sum bit s_1 will be calculated in z_1 and the carry bit $c_1 = s_2$ in z_2. As $c_0 = 1$, which is verified by a read, the offset voltage is now $V_{\mathrm{offset}} = 0.825\,V$ and p_1 and q_1 are applied. This drives the devices z_1 and z_2 to R_5. As device z_1 performs the sum operation, the device is re-programmed to R_2 in the next cycle. In z_2, the carry operation is performed. Thus, z_2 is re-programmed to R_1. The final result is now stored in the three devices as $z_2z_1z_0$ = 120 ($\widehat{=}$15).

3.2 Simulation of a 41 Trit Addition

The experimental results of [26] were fitted with the JART VCM v1b model [7, 10]. They are identical to those chosen in [6] except for $N_{\mathrm{disc,\,min}}$ which was set to $0.1{\cdot}10^{26}$ m^{-3} to allow for a stronger RESET. As in [6], R_{th} is chosen the same for SET and RESET and the temperature-dependent series resistance of the lines is neglected. The physics-based model utilizes the motion of ionic defects and the subsequent change in the concentration N_{disc} at the electronically active electrode (AE) to describe the change of device resistance. Pt is named AE since the platinum/oxide interface is the relevant place for switching. A high or low concentration represents a low or high resistive state, respectively.

When using the proposed adder circuit in a passive crossbar array, it was observed that the half-selected cells were susceptible to a drift of their resistive state since roughly half of the voltage was always applied to the common electrode. This drift especially occurred for additions with larger operands. To prevent the drift of these half-selected cells, selector devices were introduced in series to the ReRAM devices, which lead to the circuit structure shown in Fig. 2 (a). While the summands both consist of 41 trits, the resulting sum contains 42 trits due to the carry bit of the last bit numbering. Therefore, we require 42 devices for the addition. The selector consists of a Pt/TaO_x/TiO_2/TaO_x/Pt device stack, which

shows a symmetric bidirectional nonlinear $I-V$ characteristic. The model is fitted to the $I-V$ data shown in [23]. The selector prevents the switching of the half-selected devices as most of the applied voltage drops over the selector. Using our simulation model, we can easily scale up the size of the studied problem.

The selector, however, requires us to adapt the voltage scheme towards higher voltages if we want to keep the same pulse timing schemes. The SET now happens at $V_{1S1R} = V_{SET} = 4.5$ V. The read operation is defined at $V_{1S1R} = V_{Read} = 1.7$ V. Lastly, the RESET voltages are also shifted towards -3.65 V - -4.15 V with a spacing of 100 mV between the six levels. The resulting current levels of the 1S1R structure at V_{Read} are shown as in Eq. 1 for all resistance levels.

The final result of the 41 trit addition is shown in Fig. 2 (b) to (g). The top row shows the voltages across elements one, 22 and 42, while the bottom row shows their respective currents. Each step of the addition can be broken down into a SET (brown), RESET (yellow) and read (turquoise) phase. SET and read phases are always the same. In the RESET phase, we have to vary the voltage according to $V_{BE} = V_{offset} + V_{op,1}$, and $V_{TE} = -(V_{offset} + V_{op,2})$. The time axis is scaled to the region of interest for the specific device, which is the final addition step of the respective significance as well as one addition step before and after that. The resulting resistances in the first, 22nd and last device are R_2, R_0 and R_1. While in all previous addition steps, the resistance states R_0 to R_5 can be reached, and we need to map these states to the resistances available in the ternary number system, i.e., R_0, R_1, and R_2 corresponding to 0, 1, and 2, respectively. After the addition step that determines the final resistance value, the corresponding TE is set to ground. Therefore, the voltage levels are roughly halved. This half voltage would lead to a state drift of the programmed resistance state over the execution time of the addition, which is prevented through the addition of the selector device.

$$\begin{aligned} &I_{read,\,LRS} = 158\ \mu A,\ I_{read,\,R_0} = 58\ \mu A,\ I_{read,\,R_1} = 17\ \mu A \\ &I_{read,\,R_2} = 7.4\ \mu A,\ I_{read,\,R_3} = 2.91\ \mu A \\ &I_{read,\,R_4} = 0.98\ \mu A,\ I_{read,\,R_5} = 0.27\ \mu A \end{aligned} \quad (1)$$

4 BIO-SENSITIVE DEVICES

This section delves into the MVL-based BioFET implementation, a bio-inspired computing platform rooted in molecular recognition and electrochemical state manipulation. Integrating the high-radix number system promises to simplify computational complexity and spatial resource usage. To illustrate, we explore BioFETs' role in ternary logic (T, 0, F), which offers more logic states than binary (T, F), reducing the need for logic gates and transistors. BioFETs' architecture draws inspiration from ISFETs within the MOSFET family.

4.1 ISFET Sensors

Bergveld et al. [2] introduced the ISFET as a derivative of the MOSFET, a fundamental element within modern electronic devices. The innovation of the ISFET lies in replacing the conventional metal gate of the MOSFET with components including an ion-sensitive membrane, an electrolyte solution, and a reference electrode, as

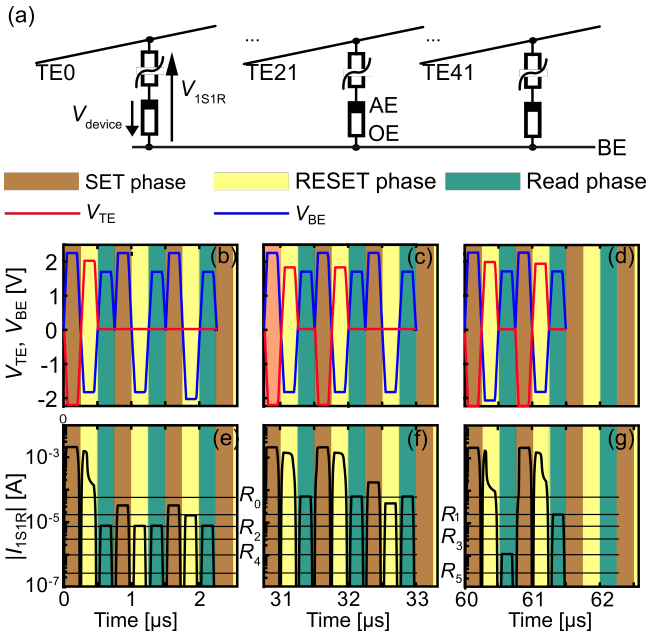

Figure 2: (a) Depicts the circuit structure for a 1S1R line array, proposed for a 41 trit addition. The figure displays the first, middle, and last devices of the entire array. (b) to (d) Illustrate voltage drops across the devices for specific device numbers 1, 22, and 42. (e) to (g) Show the currents flowing through the corresponding devices. Different adder phases are color-coded, with brown representing the SET phase, yellow indicating the RESET phase, and turquoise denoting the read phase in (b) to (g).

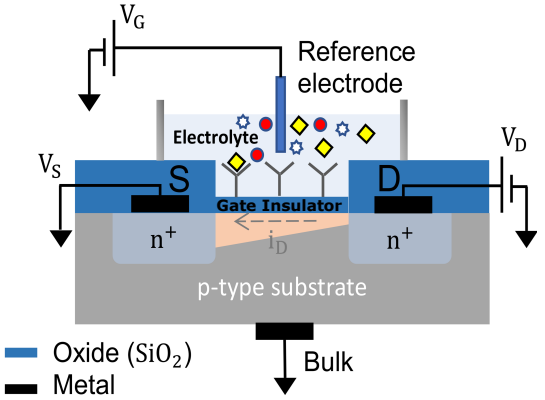

Figure 3: ISFET configuration schematic.

illustrated in Fig. 3. This modification facilitates the measurement of ion concentrations in solutions.

The operation of the ISFET is based on the fundamental principle that changes in the ion concentration in the adjacent solution can alter the charge distribution on the ion-sensitive membrane and subsequently affect the conductivity of the transistor channel. By monitoring the electrical characteristics of the ISFET, such as its current-voltage correlation, changes in ion concentration can be detected and quantified. Molecular events, such as ion accumulation or binding of charged molecules, cause shifts in the surface potential

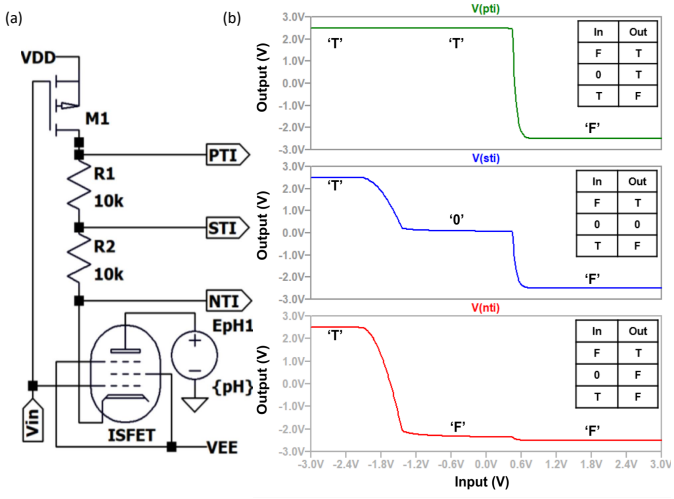

Figure 4: Illustration of ternary inverter gate configurations, comprising (a) the circuit schematic design, and (b) $V_{out} - V_{in}$ characteristic curves showcasing the behaviors of PTI, STI, and NTI.

at the solid/electrolyte interface. These shifts induce changes in the gating effect, thereby modifying the device's threshold voltage (V_{th}). The V_{th} in an ISFET marks the point at which a significant change in the conductance of the transistor channel begins. This change in conductance is a consequence of the modulation of the ion concentration in the solution, which interacts with the ion-sensitive membrane located at the gate of the transistor. Hence, the V_{th} equation of the MOSFET can be modified for ISFET as follows [1]:

$$V_{th} = E_{ref} - \Psi_0 + \chi_{sol} - \frac{\phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f. \quad (2)$$

The Eq. 2 clearly shows that the threshold voltage of an ISFET shares the constant physical component of the threshold voltage of the MOSFET. This fundamental parallelism is accompanied by two additional potential contributions: the steady potential of the reference electrode to vacuum, denoted E_{ref}, and the potential at the interface between the solution and the oxide, described by the interfacial potential $\Psi_0 + \chi_{sol}$. The surface dipole potential of the solution, represented by χ_{sol}, and Ψ_0 is the surface potential, which depends on the (bio)chemical composition of the electrolyte and the gate surface material. In this context, the gate voltage (V_g) of the ISFET remains constant, while the V_{th} encompasses the varying input signal originating from biomolecules. Conversely, in the case of the MOSFET, V_{th} remains static, while V_g varies. The shift in V_{th} of the ISFET device is reflected in the overdrive voltage (V_{OD}) of the FET, expressed as $V_{gs} - V_{th}$. This nuanced modification of the threshold serves as the designated methodology for achieving multiple output voltage levels (V_{out}), which is conducive to the implementation of MVL circuits. As a result of the biosensor threshold shift, the V_{out}/V_{in} characteristic assumes a multi-voltage nature anchored in the dynamic change of the threshold. This provides the ability to record a spectrum of voltage levels that form the basis for different output levels according to the shifting threshold, effectively enabling the construction of multi-valued logic circuits.

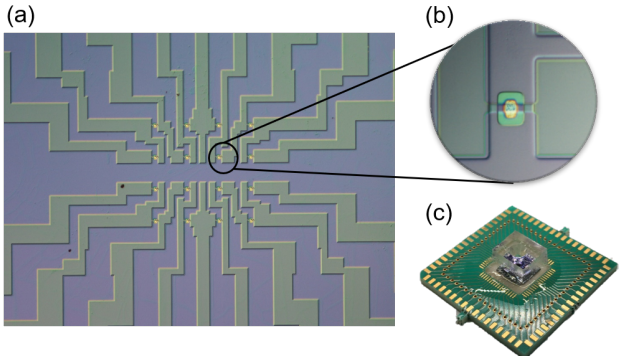

Figure 5: ISFET device structure. (a) DIC-microscope image of 4×4 array (b) Detailed view of a single device structure (c) An encapsulated n-type micro-scale ISFET sensor with 16 devices and total area consumption of $5 \times 5\ mm^2$.

In this study, we use micro-scale ISFETs, previously fabricated and detailed in the existing literature [12, 17, 21], to demonstrate the principles of MVL. The ISFET sensor consists of a common source 4×4 transistor array, eventually culminating in 16 measurement points on a $5 \times 5\ mm^2$ silicon die (as shown in Fig. 5(a)(c)). In particular, drain contacts are used for the individual addressing of each device. Fig. 5(b) shows the structure of a single device with a gate oxide (SiO_2) layer 8-10 nm thick, 16 μm wide and 6 μm long. To prepare the chip, its surface was cleaned and activated in a piranha solution (H_2O_2:H_2SO_4 1:5), after which it was wire-bonded to a chip carrier and encapsulated for connectivity, allowing FET measurements to be made in an electrolyte environment (as shown in Fig. 5(c)). The intrinsic transconductance of each device can be derived from the collected data using a specialized readout system, as described in previous work [16].

4.2 Demonstration of MVL Using ISFET

The goal is to show the practical realization of a basic ternary logic gate, specifically an inverter, using an ISFET biosensor. In a p-valued logic system, the number of unary functions is determined by p^p [15]. For binary systems, where $p = 2$, this translates to $2^2 = 4$ unary operators. However, the introduction of a third value in a ternary system results in $3^3 = 27$ distinct operators for a single input value [15]. Notably, among these unary functions, only a subset possesses meaningful significance [13] relative to the robust framework of Boolean algebra. Typically, the essential functions within ternary logic include the standard ternary inverter (STI), positive threshold inverter (PTI), and negative threshold inverter (NTI) [19]. STI works like a NOT function, returning F (False) for a T (True) input and vice versa while remaining unchanged if the input is 0 (Unknown). NTI returns 'F' when presented with '0' or 'T', and inverts 'F' to 'T' input. PTI inverts 'F' and '0', resulting in 'T', but reverts to 'F' if the input is 'T'. The circuit implementation of a ternary inverter is shown in Fig. 4(a), which exploits the distinctive features of ISFET and P-type enhancement mode field-effect transistors. The basic principles of ternary logic, including the corresponding logic symbols and representative voltage levels, are detailed in Table 1.

The proposed circuit is created based on the ISFET sensor devices that were fabricated in earlier projects [12]. The simulation has been

Table 2: Comparison of ternary logic implementation using ISFETs and MOSFETs

Aspect	ISFETs	MOSFETs
Principle	Relies on ion concentration variations to represent ternary logic states.	Uses voltage-controlled semiconductor channel to control logic states.
Logic States	True, False, Unknown (High Impedance)	True, False, Unknown (High Impedance)
Signal Representation	Ion concentration levels (pH levels)	Voltage levels
Gate Control	Ion concentration	Voltage control
Speed	Typically slower due to ion diffusion	Generally faster due to electronic processes
Power Consumption	Lower power consumption in some scenarios	Can vary; generally moderate to high
Noise Immunity	Can be sensitive to environmental factors	Generally immune to ion-based disturbances
Manufacturing	May require specialized processes	Established semiconductor fabrication
Compatibility	Limited integration with traditional CMOS	Well-integrated with traditional CMOS
Scalability	Limited scalability for complex circuits	Highly scalable for complex circuits

performed in LTspice based on the ISFET model to demonstrate the PTI, STI and NTI as it is shown in Fig. 4(b). For the bio-sensitive ternary inverter, the output is represented as $V_{Out} = V_{DD} \times R1/(R1+R2)$. When the ratio of resistors R1 and R2 is constant, the output voltage will be unchanged, showing the output of '0' while V_{in} is in middle voltage. Hereby, it is easy to find three other stable stages as well. Based on different thresholds and, consequently, different transconductances of the ISFET, the R1 and R2 can be controlled (PMOS resistance can be neglected). Thus, the middle logic level in STI can be tuned to be very high for PTI or very low for NTI.

This simulation showcases an exemplar of ternary inverter gate implementation along with its corresponding outcomes. Additionally, Table 2 compares the implementations of ternary logic using ISFETs and MOSFETs.

4.3 Discussion

Moore's Law, which describes the doubling of transistors in a densely integrated circuit approximately every two years, is reaching its limits due to physical constraints. However, recent advances in nanofabrication techniques have opened the possibility of using multiple-array ISFET sensors to reduce size by increasing array density. In addition, well-established clean room fabrication has made it possible to achieve uniform sensor characteristics at the wafer scale for biorecognition. Here, we present and confirm the notion of multivalued biosensors by exploiting the unique electronic properties of ISFETs to perform MVL. By ingeniously combining an ISFET transistor with a P-type enhancement mode field-effect transistor and using two resistors (R1 and R2) to regulate the ratio, we construct a series of ternary inverter gates that include PTI, STI, and NTI functions. This innovative approach allows the output voltage to exhibit three stable levels, which is achieved by adjusting the intermediate output logic level of the STI to be either significantly high or low, thereby implementing PTI and NTI, respectively, based on the resistance ratio. Our research highlights the potential of utilizing bio-sensitive devices such as ISFETs to implement MVL. As a result, ISFET multiple-array sensors can function as MVL devices, resulting in reduced chip area and increased computational speed compared to their CMOS counterparts. The proposed model addresses the challenges posed by the plateauing of Moore's Law and opens up exciting possibilities for efficient and advanced logic processing. Adopting ternary inverters with ISFET devices aligns with the quest for streamlined, condensed, and adaptable computing frameworks and represents a promising trajectory for advanced electronic systems. In addition, this approach is relevant in the area of hardware security. The potential advantages of ternary logic in this area can potentially strengthen encryption and authentication schemes, underscoring its relevance and potential contributions to security-focused applications.

5 CONCLUSION

This paper delves into the realm of MVL design within the context of ReRAM and ISFET devices. The study leverages the dynamic nature of state transitions in ReRAM and ISFET devices to create functional MVL circuits. For instance, a ternary arithmetic circuit is realized using a ReRAM crossbar array, harnessing its seven resistive states for stateful logic. Similarly, ISFET devices are employed to demonstrate three ternary inverted logic gates: STI, PTI, and NTI. Through experimental evaluation, it becomes evident that both ReRAM and ISFET devices offer highly dependable seven states in ReRAM and three in ISFET. Additionally, the IS1R architecture and the implementation of inverted gates underscore the compatibility of these devices with conventional CMOS technology. The obtained experimental results strongly suggest the remarkable potential of both technologies to drive advancements in MVL implementations, even in the context of mainstream computing.

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REFERENCES

[1] P Bargveld. 2003. Thirty years of ISFETOLOGY - What happened in the past 30 years and what may happen in the next 30 years. *Sensors and actuators. B: Chemical* 88, 1 (2003), 1–20. https://doi.org/10.1016/S0925-4005(02)00301-5

[2] Piet Bergveld. 1972. Development, operation, and application of the ion-sensitive field-effect transistor as a tool for electrophysiology. *IEEE Transactions on Biomedical Engineering* 5 (1972), 342–351.

[3] Elena Dubrova. 1999. Multiple-Valued Logic in VLSI: Challenges and Opportunities. *Proceedings of NORCHIP'99* (11 1999).

[4] Boroumand et al. 2018. Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks. *ACM SIGPLAN Notices* 53 (03 2018), 316–331. https://doi.org/10.1145/3296957.3173177

[5] Bhattacharjee et al. 2018. Multi-valued and Fuzzy Logic Realization using TaO_x Memristive Devices. *Scientific Reports* 8, 8 (2018), 1–10.

[6] Bengel et al. ISCAS 2021. Implementation of Multinary Lukasiewicz Logic using Memristive Devices. (ISCAS 2021).

[7] C. Bengel et al. 2020. Variability-Aware Modeling of Filamentary Oxide based Bipolar Resistive Switching Cells Using SPICE Level Compact Models. *TCAS 1* (2020).

[8] D. Ielmini et al. 2018. In-memory computing with resistive switching devices. *Nature Electronics* 1, 6 (2018), 333–343.

[9] Etiemble et al. 1988. Comparison of binary and multivalued ICs according to VLSI criteria. *Computer* 21, 4 (1988), 28–42. https://doi.org/10.1109/2.49

[10] F. Cueppers et al. 2019. Exploiting the switching dynamics of HfO_2-based ReRAM devices for reliable analog memristive behavior. *APL Mater.* 7, 9 (2019), 91105/1–9.

[11] Hoffer et al. 2020. Experimental Demonstration of Memristor-Aided Logic (MAGIC) Using Valence Change Memory (VCM). *IEEE Trans. Electron Devices* 67, 8 (2020), 3115–3122.

[12] Ingebrandt et al. 2006. Label-free detection of DNA using field-effect transistors. *physica status solidi (a)* 203, 14 (2006), 3399–3411.

[13] Keshavarzian et al. 2014. A novel CNTFET-based ternary full adder. *Circuits, Systems, and Signal Processing* 33, 3 (2014), 665–679.

[14] Lin et al. 2009. CNTFET-based design of ternary logic gates and arithmetic circuits. *IEEE TNANO* 10, 2 (2009), 217–225.

[15] Miller et al. 2007. Multiple valued logic: Concepts and representations. *Synthesis lectures on digital circuits and systems* 2, 1 (2007), 1–127.

[16] Nguyen et al. 2018. Readout Concepts for Label-Free Biomolecule Detection with Advanced ISFET and Silicon Nanowire Biosensors. (2018).

[17] Offenh et al. 1997. Field-effect transistor array for monitoring electrical activity from mammalian neurons in culture. *Biosensors and Bioelectronics* 12, 8 (1997), 819–826.

[18] Pachauri et al. 2016. Biologically sensitive field-effect transistors: from ISFETs to NanoFETs. *Essays in biochemistry* 60, 1 (June 2016), 81—90. https://doi.org/10.1042/ebc20150009

[19] Raychowdhury et al. 2005. Carbon-nanotube-based voltage-mode multiple-valued logic design. *IEEE TNANO* 4, 2 (2005), 168–179.

[20] Rai et al. DATE 2021. Vertical IP Protection of the Next-Generation Devices: Quo Vadis? (DATE 2021).

[21] Sprössler et al. 1999. Electrical recordings from rat cardiac muscle cells using field-effect transistors. *Physical review E* 60, 2 (1999), 2171.

[22] Singh et al. 2023. Finite State Automata Design using 1T1R ReRAM Crossbar. In *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*. 1–5. https://doi.org/10.1109/NEWCAS57931.2023.10198206

[23] S. Kim et al. 2012. Selector Devices for Cross-point ReRAM. In *13th CNNA, Turin, ITALY*. 2012 13th International Workshop On Cellular Nanoscale Networks and Their Applications (cnna).

[24] Temel et al. 2004. Implementation of Multi-Valued Logic Gates Using Full Current-Mode CMOS Circuits. *Analog Integrated Circuits and Signal Processing* 39, 2 (2004), 191–204. https://doi.org/10.1023/B:ALOG.0000024066.66847.89

[25] Wang et al. 2021. High-Density Memristor-CMOS Ternary Logic Family. *IEEE TCAS I: Regular Papers* 68, 1 (2021), 264–274. https://doi.org/10.1109/TCSI.2020.3027693

[26] W. Kim et al. 2016. Multistate Memristive Tantalum Oxide Devices for Ternary Arithmetic. *Sci. Rep.* 6 (2016), 36652.

[27] Xu et al. 2018. Fully Functional Logic-In-Memory Operations Based on a Reconfigurable Finite-State Machine Using a Single Memristor. *Advanced Electronic Materials* 4 (2018), 1800189.

[28] Zacherle et al. 2016. *Resistive switching: from fundamentals of nanoionic redox processes to memristive device applications / Edited by Daniele Ielmini and Rainer Waser*. Wiley-VCH, Weinheim. https://doi.org/10.1002/9783527680870.ch3

[29] Daniel Etiemble. 2003. Why M-valued circuits are restricted to a small niche? *Journal of Multiple-Valued Logic and Soft Computing* 9 (01 2003), 109–123.

[30] Daniel Etiemble. 2019. Evolution of Technologies and Multivalued Circuits. *CoRR* abs/1907.01451 (2019). arXiv:1907.01451 http://arxiv.org/abs/1907.01451

[31] J. W. McPherson. 2007. Reliability Trends with Advanced CMOS Scaling and The Implications for Design. In *2007 IEEE CICC*. 405–412. https://doi.org/10.1109/CICC.2007.4405763

[32] Smith. 1981. The Prospects for Multivalued Logic: A Technology and Applications View. *IEEE TC* C-30, 9 (1981), 619–634. https://doi.org/10.1109/TC.1981.1675860

[33] Özer et al. 2006. Multiple-valued logic buses for reducing bus energy in low-power systems. *Computers and Digital Techniques, IEE Proceedings* - 153 (08 2006), 270 – 282. https://doi.org/10.1049/ip-cdt:20050160