Fabrication of Ultrasmall Si Encapsulated in Silicon Dioxide and Silicon Nitride as Alternative to Impurity Doping

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Further miniaturization of CMOS devices based on impurity doped semiconductors is limited due to statistical fluctuation of the impurity concentration in very small volumes and dopant deactivation, increasing the resistance and power consumption. Based on DFT calculations and backed by experimental data, the nanoscale electronic structure shift induced by anions at surfaces (NESSIAS) was described recently. It explains the structure shift of low doped single crystalline Si-nanowells (Si-NWs) with thicknesses $\leq 3\,\mathrm{nm}$ embedded in SiO_2 (Si_3N_4) towards n-type (p-type) behavior. The influence of the anions is on the scale of a few nanometers, allowing for very steep p-n junctions without the drawbacks of impurity doping. The process to fabricate crystalline silicon (c-Si) nanowells (NWs) embedded in SiO_2 and Si_3N_4, starting with silicon on insulator (SOI) across $15 \times 15\,\mathrm{mm}^2$ samples, is described. Four possible methods to fabricate Si-NWs by thinning down single crystalline top-Si of a SOI substrate are evaluated in terms of reproducibility and surface roughness.

1 Introduction

The complementary metal oxide semiconductor (CMOS) technology is the foundation of our modern computers. Impurity doping is an essential element of CMOS devices, resolving many of their electronic key properties [1]. Hence, the type and density of impurity dopants is at the centre of device design, allowing for the versatility and adaptability of CMOS technology to virtually every semiconductor technology, from analog design to very large scale integration (VLSI). By scaling down CMOS transistor dimensions, the influence of the applied gate potential on the channel current decreased. This phenomenon, known as short channel effects, gave rise to the introduction of silicon on insulator (SOI) substrates, the development of Fin-FET (field effect transistor) technology and the upcoming gate-all-around (GAA)-FET technology. With increasing surface to volume ratio, impurity doping on the nanoscale faces the problems of dopant inactivation, due to increased ionization energy as consequence of dielectric mismatch [2, 3], the dopant out-diffusion being on the same length scale as the gate length[4, 5] and statistical fluctuations of the dopant concentration in nanoscale volume transistors [4, 6, 7], leading to unpredictable device behavior. The deactivation of dopants near the surface in nanowires effecively reduces the conducting path and increases the resistance of GAA-FETs. Beside the aforementioned issues, dopants can freeze out at low temperatures leaving them electronically inactive and restricting their application in cryoelectronics. With these drawbacks it would be beneficial to avoid impurity doping altogether, en-

abling further efforts in device miniaturization, namely down-scaling gate lengths below the dopant out-diffusion limit of drain and source regions.
Based on DFT calculations, the effect of a nanoscale electronic structure shift induced by anions at surfaces (NESSIAS) was predicted [8, 9] and would allow very steep p-n junctions on GAA-FETs with a diameter of a few nanometers [10]. Recently we demonstrated the NESSIAS effect on ultrathin Si-NWs as a function of Si thickness and embedding dielectric, with SiO_2 and Si_3N_4 yielding an effective n- and p-type doping, respectively [10–13]. The conduction band edge of these samples was measured with grazing incidence x-ray absorption spectroscopy in total fluorescence yield (XAS-TFY) and the valence band edge with synchrotron UV photoelectron spectroscopy (UPS) measurements at Elettra Sincrotrone Trieste, Italy. The fabrication of appropriate samples combines, etching down of the top-Si of SOI, digital etching, rapid thermal nitridation, CVD deposition of SiN_x and SiO_2, chemical mechanical polishing, direct-bonding and deep reactive ion etching. The present work presents the processing protocols and parameters to arrive at high-quality crystalline silicon (c-Si) nanowells (NWs) embedded in SiO_2 and Si_3N_4 on samples of 15 mm × 15 mm. Samples fabricated this way lead to the measurement of the valence band fine structure of Si-NWs [13]. The fabrication of Si-NWs embedded in Si_3N_4 involves direct-bonding, rendering the surface roughness of the samples during processing to be an important parameter. The Si-NWs for the XAS-TFY measurements had to be homogeneously thinned down across at least 4 mm, due to the required grazing incidence angle and the beam width at the XAS-TFY set-up (supporting information of [12]). Section 2 explaines the methods used in sample fabrication and characterization. Section 3 presents characterization results, enabling us to evaluate our approaches of sample fabrication in terms of optimum structural properties. Section 4 delivers a conclusion.

2 Methods

Unless stated otherwise all samples described here originate from a 12 inch silicon on insulator (SOI) wafer with a p-doping concentration of $1 \cdot 10^{15}\,cm^{-3}$ in the top-Si. The initial SOI layer stack consists of 85 nm (100)-oriented Si (top-Si), 145 nm SiO_2 as buried oxide (BOX) and 775 µm (100)-Si as substrate. The wafer was diced into square pieces with a side length of 15 mm. Regardless of whether the Si-NWs were embedded in SiO_2 or Si_3N_4, the top-Si was thinned down and served as the Si-NW. Although the bond interface is not the Si-NW itself, high initial roughness of the remaining Si layer may be passed on to the upper layers. Therefore, it is imperative to keep the bond interface as smooth and free of defects as possible, for the sucessful fabrication of Si_3N_4-embedded Si-NW samples. Four different approaches to the initial thinning down procedure were investigated. Using the best of these four methods determined, the SiO_2- and Si_3N_4-embedded NW-samples were fabricated.

2.1 Thinning down the top-Si

In order to roughly thin down the first 80 nm of top-Si 4 different processes were explored. The tested processes are (I) dry thermal oxidation (TO) and subsequent wet-etching in buffered oxide etch (BOE), (II) wet-etching in tetramethylammoniumhydroxide (TMAH), (III) isotropic radical etching (IRE) and (IV) inductively coupled plasma reactive ion etching (ICP-RIE). The samples used for these tests originated from a 6 inch Si wafer, with a p-type doping (B) corresponding to a resistivity of 1 to 100 Ω cm and a thickness of 675 µm. The wafer was diced into quadratic pieces with a side length of 15 mm. In order to grow a thermal oxide (I), a Centrotherm Centronix 1200 furnace was used at a temperature of 1200 °C. The thickness of the grown SiO_2 was estimated prior to the oxidation by the Deal-Grove model [14], and the resulting oxide thickness was measured with an Accurion nanofilm_ep4 spectroscopic ellipsometer. By taking the molecular weight and density of SiO_2 and Si into account, the thickness of the consumed Si can be estimated to be 45 % of the measured oxide thickness [15]. Before performing atomic force microscopy (AFM), the samples were immersed in BOE for 2 min to completely remove the thermal SiO_2. For the wet chemical etching (II), the native SiO_2 on the samples was removed with 1 % HF prior to etching with TMAH. The etch rate and roughness of the remaining Si are strongly dependent on

the choice of TMAH solution. In this work, a solution consisting of 25 % TMAH and isopropyl alcohol (IPA), mixed in a 5:1 ratio, as described in [16], was used. To increase the etch rate further, the etching took place at 75 °C, instead of 60 °C. For the radical etching process (III), an Oxford Instruments Plasmalab PRS 90 barrel reactor was used with O_2 and SF_6 as reactive gases at a pressure of 810 mTorr and an HF power of 100 W. For the ICP-RIE process (IV), an Oxford Instruments PlasmaPro 100 Cobra ICP RIE system was used with a flow of 30 sccm O_2 and 15 sccm SF_6 at a pressure of 15 mTorr and only 20 W HF power.
The resulting surfaces were characterized by a DS95 AFM from DME in alternating current mode. Two samples per preparation method were measured in three areas each, with a size of $2 \times 2\,\mu m^2$. Measurement data was processed with Gwyddion 2.56 [17].
The surface morphology after each thinning method is shown in **figure 1**. The surface roughness appears largely to be uniformly distributed as hills and valleys, being a few nanometers deep and wide. Method III shows an exception: there are larger hills of about 100 nm in diameter distributed across the entire surface.
Figure 2 illustrates that all methods result in a sub-nanometer RMS roughness, while the highest value for the IRE process is in the order of 0.55 nm and therefore slightly above the acceptable RMS roughness for bonding of 0.5 nm [18]. The lowest roughness however is obtained by method I with around 0.14 nm. As the etching part is self-limited and stops at the Si layer, this method provides best overall results and process control for rough thinning of top-Si. The possible influence on the surface roughness by the BOE component in method I was investigated by comparing the etched Si to the sample state after thermal oxidation, see **figure 3**. It was found that the RMS roughness reduces from about 222 pm prior to etching to 142 pm after the BOE step. The AFM image in **figure 3b** shows the occurrence of multiple particles with height up to 2 nm in the oxidized state. These are not detected after oxide removal.

2.2 Sample fabrication

Thinning down the top-Si by thermal oxidation is the most controllable process and also yields the smoothest surface. Therefore, all Si-NWs were fabricated by initially thinning down by thermal oxidation.

2.2.1 Si-NW in SiO_2

In order to realize Si-NWs emedded in SiO_2, it was sufficient to thin down the Si and oxidize the top side of the remaining Si layer, since its rear side already was in contact with the BOX. The thermally grown oxide was removed with BOE, before digital etching in HNO_3 and HF was employed to reach the desired thickness [19]. A cycle of digital etching starts with the removal of SiO_2 in BOE, for the thermal oxide only, or HF for subsequent etching cycles, and ends with oxidation of Si in HNO_3. The formation of SiO_2 in HNO_3 is described as a self limiting process, making it the perfect choice for thinning down top-Si in a controlled way and the oxide was reported to be of comparable quality to thermally grown oxide. The oxidizing solution consists of 69.6 % of HNO_3 and deionized water (DI-water) in a ratio of 59:41 and was heated up to 108 °C. Before immersing the samples in the oxidizing solution for 10 min, the native oxide was removed with 1 % HF. It was found that one oxidation cycle consumes (0.65 ± 0.10) nm of top-Si and grows (1.4 ± 0.2) nm of SiO_2 on top of the surface. The etching cycles of HF and HNO_3 were repeated until the thickness of the remaining Si-NW, below the SiO_2 grown in HNO_3, matched the required thickness. The oxide thickness is sufficient to protect the NWs from oxidation in air. The fabrication of Si-NWs embedded in SiO_2 was concluded by the deposition of a 100 nm thick Al frame, to prevent the sample from charging up during UPS measurements. After depositing the Al contacts, the samples were coated with photo resist to protect the wet chemical oxide from chemical or mechanical changes, during the transport to the synchrotron.
Since the smoothest surfaces were observed with method I, the influence of multiple digital etching cycles on samples etched by method I was investigated by fabricating six samples of bulk-Si. Out of these samples, two each were etched for one, four and seven cycles; a selection of the resulting surfaces is shown in **figure 4**. No negative impact can be seen for etching method I. On the contrary, already after the

first cycle, the RMS roughness reduced to about 110 pm. In **figure 5a**, the additional etch cycles performed showed no further RMS roughness reduction. This is of significant importance for the confined Si layer, as it is not possible to precisely predict how many digital etching cycles will be needed in order to achieve the required thickness. A variation in RMS roughness or a late saturation point of this value would not only prove difficult for fabrication, but also affect the synchrotron measurements. Furthermore, it is beneficial to perform at least one HNO_3/HF cycle when utilizing this method. Due to the high-quality surface achieved by digital etching, an investigation on its effect on the method III, which yielded the roughest Si surface, was performed. The Si surface etched by method III was measured after one, four and seven cycles on six different samples (two samples per cycle count) of bulk-Si fabricated by method III. In **figure 6**, large pinholes with up to 40 nm depth can be seen already after the first etching cycle. Although the application of at least a single HNO_3/HF cycle appears to reduce the roughness (**figure 5b**), it is important to note that different samples were first brought to the various etching stages, and then were measured in sequence by AFM. This reduction in thickness, combined with the high variance between samples at the same etch state, suggests that deep impinging and surface damage or oxidation is occurring during the IRE step. The random nature as well as severity of these defects render this method unviable, regardless of HNO3/HF etching, which even in the most favourable cases did not significantly reduce the RMS roughness.
Overall the AFM measurements suggest that each digital etching step has the potential to reduce the RMS roughness. However extending the number of etching cycles beyond the first one, does not have any further effect on the surface roughness.

2.2.2 Si-NW in Si_3N_4

Like for the Si-NWs embedded in SiO_2 the Si-NWs embedded in Si_3N_4 had to be fabricated across at least 4 mm × 4 mm and to a thickness variation within one atomic layer. In contrast to Si-NWs embedded in SiO_2, Si_3N_4 had to be grown on the top and rear side of the NWs, since it is not possible to start with SOI, where the burried insulator is Si_3N_4 instead of SiO_2 and the top-Si is single crystalline. Getting access to the rear side of the NW can be realized by direct-bonding the sample to another piece of Si and removing the substrate of the original SOI sample and the BOX after processing the top side.
In order to thin down the top-Si it was thermally oxidized and digitally etched. In contrast to Si-NWs in SiO_2 the thickness of the remaining top-Si has to be thicker than the final Si-NW thickness, because the consumption of Si during the fabrication has to be taken into account. Immediately before thermal nitridation of the top-Si, the wet chemical SiO_2 was removed with 1 % HF. The nitridation took place in an AnnealSys AS-ONE 150 RTP at atmospheric pressure in an atmosphere consisting of Ar and NH_3 achieved by a flow of 1000 sccm Ar and 300 sccm NH_3. The RTP was heated up to 1050 °C with 20 K s^{-1} and held there for 120 s. Benefits of thermally grown Si_3N_4 are a self-limiting growth process [20], with a strong dependency of the resulting layer thickness on the processing temperature and good interface quality[21] and the possibility to grow layers of up to 3.7 nm with roughness of 0.32 nm as determined by X-ray reflectivity [22], which is still acceptable for direct-bonding. A schematic cross section of the sample after rapid thermal nitridation is shown in **figure 7a**. On top of the thermal Si_3N_4, about 24 nm of substoichimetric SiN_x were deposited by using an Oxford Instruments PlasmaPro 100 ICP-PECVD (plasma enhanced chemical vapor deposition). The tool is equipped with N_2, O_2, He and a silane mixture of 10 % SiH_4 and 90 % He, which subsequently will be referred to as silane. The deposition of SiN_x is a cycled two step process and takes place at 350 °C; process parameters are listed in **table 1**. The first step is the deposition of SiN_x itself, followed by pumping down the chamber for 20 s. The second part is a nitrogen plasma, which is used to reduce the amount of hydrogen in the deposited layer. To further reduce the amount of H in the layer after deposition, the samples were annealed in the AS-One 150 in Ar at atmospheric pressure at 1050 °C. After the deposition and annealing of SiN_x about 80 nm of SiO_2 were deposited by the same ICP-PECVD. Similar to the SiN_x process, the SiO_2 deposition is a cycled 3 step process at 350 °C, the process parameters are listed in **table 2**. The first half of the cycle is the deposition itself and is followed by pumping down the chamber for 1 min. In the second half of the cycle, it is attempted to reduce the amount of H using two oxygen plasmas. After the SiO_2 de-

position in the ICP-PECVD, the samples were annealed in the RTP again, using the above-mentioned recipe. The ICP-PECVD was chosen for the deposition of SiN_x and SiO_2, since its processing temperature of 350 °C is closest to the temperature used for bonding, therefore reducing the strain of the layers during bonding. **Figure 7b** schematicially shows the layer seqeuence on the sample after the deposition of SiN_x and SiO_2. The surface of the SiO_2 was mechanically polished with a silica slurry for three minutes, applying a pressure of 4.8 kPa in a Logitech PM5. This process reduces the RMS roughness below the required 0.5 nm to be able to direct-bond the sample to a piece of bulk-Si [18]. Prior to direct-bonding the sample and the piece of bulk-Si were RCA cleaned, providing a thin wet chemical SiO_2 remaining on top of the bulk-Si for enabling hydrophilic bonding [23, 24]. During the RCA two HF-dips were performed, one after the piranha clean and one after standard clean one. The duration of the HF-dips was 10 s each, enough time to remove the SiO_2 grown on the Si sample, while removing only a small amount of the thick SiO_2 ontop of the SOI sample. The RCA did not include a third HF-dip to improve the bonding quality. Immediately after the RCA clean, the polished SiO_2 surface of the SOI sample was brought into contact with the polished side of the bulk-Si piece, holding the pieces in place via van der Waals forces and hydrogen bonds [24]. The sample was put into a SÜSS MicroTec SB6e Wafer Bonder. The tool was pumped down to $1 \cdot 10^{-4}$ mbar and heated up to 250 °C and the sample removed after 20 h. Following the initial bonding step the samples were annealed for 10 h at 1100 °C at atmospheric pressure in a N_2 atmosphere with a flow of 5000 sccm N_2, see **figure 7c** for a schematical cross section of the bonded sample. After bonding the sample to bulk-Si, the original Si wafer from the SOI-sample was removed using cycled 3 step deep reactive ion etching (DRIE) in a PlasmaPro 100 Cobra. A single cycle consists of three steps: a deposition step, a breakthrough and a main etching step; process parameters are listed in **table 3**. In the first step, a polymer is formed and deposited onto sides and on top of the sample. The deposited polymer on the side of the sample is important, to protect the bonded interface from being etched along imperfections in the bond interface. During the breakthrough step reactive ions are accelerated towards the surface of the sample and react with the polymer on the top of the sample, while it remains on the sides of the sample. The sides of the sample are protected by the polymer during the main etching step. The DRIE process removes 1.3 µm of Si per cycle with a selectivity of 1:1000 between SiO_2 and Si. Therefore, the initial BOX with a thickness of 145 nm is a suited etch stop, giving a tolerance of almost 100 etching cycles. Following the etching of the SOI substrate, the sample was RCA cleaned, with very short HF dips to keep the BOX intact and protect the Si-NW from oxidation. Immediately before a nitridation in the RTP AS-One 150, the BOX was removed with BOE. The sample fabrication of the Si-NW embedded in Si_3N_4 was concluded by locally removing the top Si_3N_4 and directly contacting the Si-NW with Al to prevent the sample from charging up during UPS measurements. For the transport to the synchrotron, the Si_3N_4-embedded samples are coated with resist as well. The finished sample is depicted in **figure 7d**.
After measurement at the synchrotron FIB lamella were prepared by a FEI Strata400 system with a gallium (Ga) ion beam, and high-resolution TEM (HRTEM) images were recorded with a FEI Tecnai G2 F20 at 200 kV operation voltage.

3 Results

In this section, the results of the fabrication of Si-NWs in SiO_2 and Si_3N_4 will be described. A comparison between ellipsometric measurements and high resolution transmission electron microscopy (HR-TEM) images will be made and a brief overview of the results obtained by synchrotron measurements will be presented. A detailed discussion of the synchrotron measurements is beyond the scope of this work and is given in [10–12].

3.1 Si-NWs in SiO_2

Si-NWs embedded in SiO_2 follow a simplified fabrication sequence as compared to the Si-NWs in Si_3N_4. The thickness of the remaining top-Si of every sample was measured by ellipsometry after every step of

digital etching. Since the top-Si for Si-NWs embedded in Si_3N_4 has to be thicker after digital etching than for Si-NWs in SiO_2, samples with a remaining top-Si deemed too thin to be used for a Si-NW in Si_3N_4 were still be usable as a Si-NW in SiO_2. The thickness of the Si-NWs has been measured by ellipsometry and confirmed by high resolution transmission electron microscopy (HR-TEM) [10–12]. The energy levels of the conduction and valence band with respect to the vacuum energy for Si-NWs between 1.1 to 5 nm thickness [10–13] are shown in **figure 8** (magenta triangles). The binding energy for the conduction band edge was measured by gracing incidence XAS-TFY and the binding energy for the valence band edge by synchrotron UPS. Of particular interest is the fact that neither the conduction nor the valence band behave like predicted by conventional quantum confinement (solid green lines). The binding energy of the band edges is larger as compared to bulk-Si(grey solid lines), indicating n-type behavior with respect to bulk-Si. On the measured thickness an error of ± 1.5 monolayers along $\langle 100 \rangle Si$ or ± 0.2 nm was assumed. The valence and conduction band for a NW of 1.9 nm thickness, were measured on the same sample, reducing the error due to sample to sample variation.

3.2 Si-NWs in Si_3N_4

The sample fabrication of Si-NWs in Si_3N_4 starting from SOI, as described in section 2.2.2, has the benefit of a single-crystalline NW with a known low-index orientation. **Figure 9a** shows a HR-TEM cross section image of Si-NW in Si_3N_4 along the $\langle 100 \rangle$ direction. The cyan area marks the Si-NW and its thickness is (3.5 ± 0.5) unit cells. With a lattice constant of $a = 0.54$ nm [25], the thickness is determined to be (1.9 ± 0.3) nm from the HR-TEM image. The thickness of the sample depicted in **figure 9a**, measured by ellipsometry, is (1.7 ± 0.3) nm. From the NW thickness of another sample (shown in [13]) measured by HR-TEM ((1.5 ± 0.3) nm) and ellipsometry ((1.3 ± 0.3) nm) it is concluded, that there is a constant offset of 0.2 nm between NW-thicknesses determined by HR-TEM and ellipsometry. This offset can be explained by inaccuracies in the dispersion relations, which have to be assumed for every layer in the ellipsometric model. The single-crystalline nature of the NWs means for UPS measurements, that there is no signal originating from amorphous Si, which was the case for earlier samples, fabricated for UPS measurements, with a consequent increase in SNR and sensitivity regarding the detected valence band edge. The earlier Si-NWs embedded in Si_3N_4 used for measurements of the valence band, were fabricated by CVD deposition of Si_3N_4, amorphous Si (a-Si) and Si_3N_4 on (111) Si and subsequent annealing in order to crystallize the amorphous silicon forming small Si crystallites [10, 11, 13]. **Figure 9b** shows a HR-TEM image of one of these samples with a nano-crystal highlighted in the cyan area. While it is not possible to determine the crystalline fraction of Si forming the NW, it is save to say that the NW in [10] is poly-crystalline and thus significantly inferior to a monolithic Si-NW as formed by a thinned down SOI layer of defined global orientation. The notable amorphous fraction of Si in such NWs results in a low signal to noise ratio, leading to long integration times during measurements and lower sensitivity as was impressively demonstrated by resolving the valence band fine structure by synchrotron UPS, using samples processed in accord with our findings presented herein [13]. The measured valence band energies for crystallized Si nano crystalls are shifted towards lower binding energies with respect to the energy of bulk-Si, as is shown in **figure 8** (blue squares), indicating p-type behavior.
In **figure 8** the binding energy of the valence band of Si_3N_4-embedded NWs of 1.5 to 5.0 nm is shown. Notable is, that the binding energy of the valence band with decreasing NW thickness is decreasing, despite the prediction by conventional quantum confinement. It should be noted, that for valence and conduction band measurement of the NW of 1.9 nm thickness, the same sample was used. The measured valence and conduction bands for SiO_2- and Si_3N_4-embedding, indicate a possible n- and p-type behavior enabling the fabrication of dopantless FETs.

4 Conclusion

We demonstrated the fabrication of single crystalline Si-NWs embedded in Si_3N_4 of homogeneous thickness across 15 mm × 15 mm SOI samples. The challenge of the fabrication of these samples is to grow

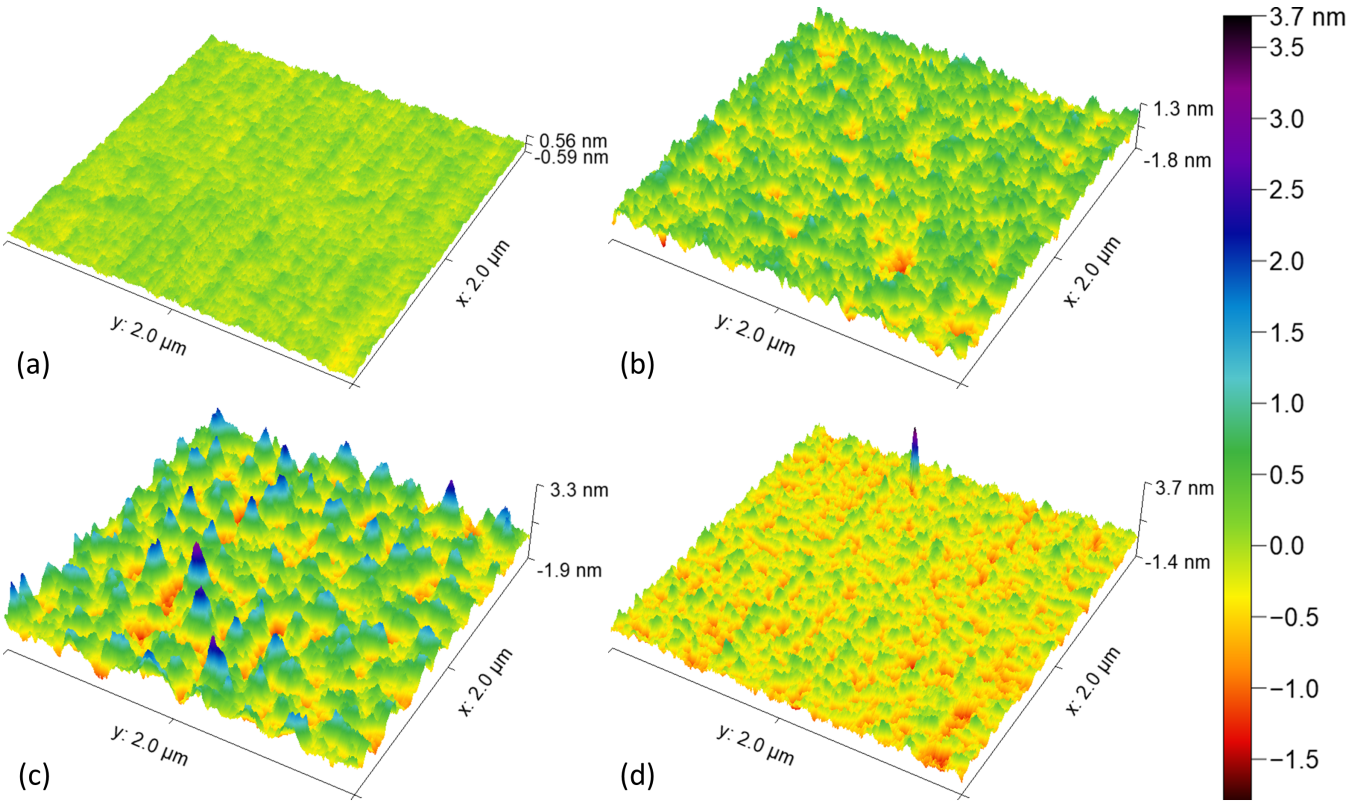

Figure 1: AFM measurements on bulk-Si samples prepared with the following methods. a) Thermal oxidation (TO) and removal of the SiO_2 with BOE. b) Wet-etching in 25 % TMAH and IPA, mixed in a ratio of 5:1, at 75 °C. c) Isotropic radical etching (IRE). d) Inductively coupled plasma reactive ion etching (ICP-RIE).

Table 1: ICP-PECVD process for the deposition of SiN_x at 350 °C.

Step	t [s]	p [mTorr]	P_{RF} [W]	P_{ICP} [W]	N_2 [sccm]	O_2 [sccm]	He [sccm]	10 % SiH_4 [sccm]
Deposition	30	10	10	300	200	0	50	25
H reduction	300	30	0	450	200	0	50	0

Si_3N_4 on the front and rear side of the NW. This was realized by polishing and direct-bonding the samples, after the front side had been nitridated, to a piece of Si and removing the original SOI-substrate and the BOX, before nitridation of the rear side. For Si-NWs in Si_3N_4 it was found, that ellipsometry yields NW thicknesses, which are 0.2 nm thinner as compared to values derived from HR-TEM images. From comparison of ellipsometric measurements and HR TEM images, it is concluded, that the thickness of Si-NWs in SiO_2 measured by ellipsometry matches with HR-TEM images. The NWs were fabricated by thinning down the top-Si of SOI. Since a rough surface after thinning down might be passed on to layers deposited ontop of the NW, we investigated four different methods of thinning down and found that dry thermal oxidation is the most controllable process and yielded the smoothes surfaces. The thinning down was concluded by digital etching, using BOE during the first cycle to remove the thermal oxide and to grow about 1.4 nm of wet chemical SiO_2 in HNO_3. For further cycles HF instead of BOE was used to remove the wet chemical SiO_2. It was found, that even one cycle of digital etching further improves the surface roughness of thinned down top-Si. With a process established to fabricate Si-NWs in Si_3N_4 across $15 \times 15\,mm^2$ samples, measurements will be done to determine the valence and conductance band energies of different Si-NW thicknesses in Si_3N_4.

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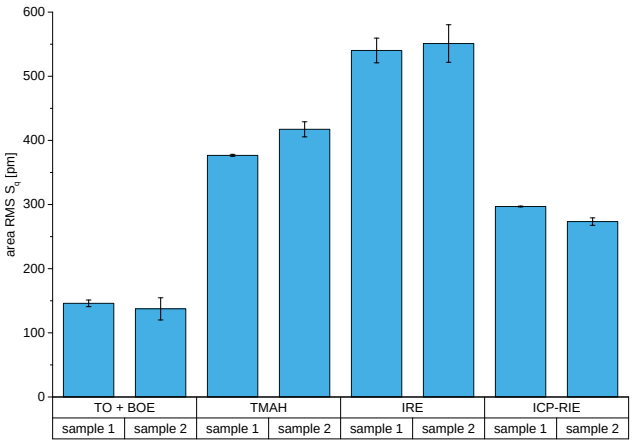
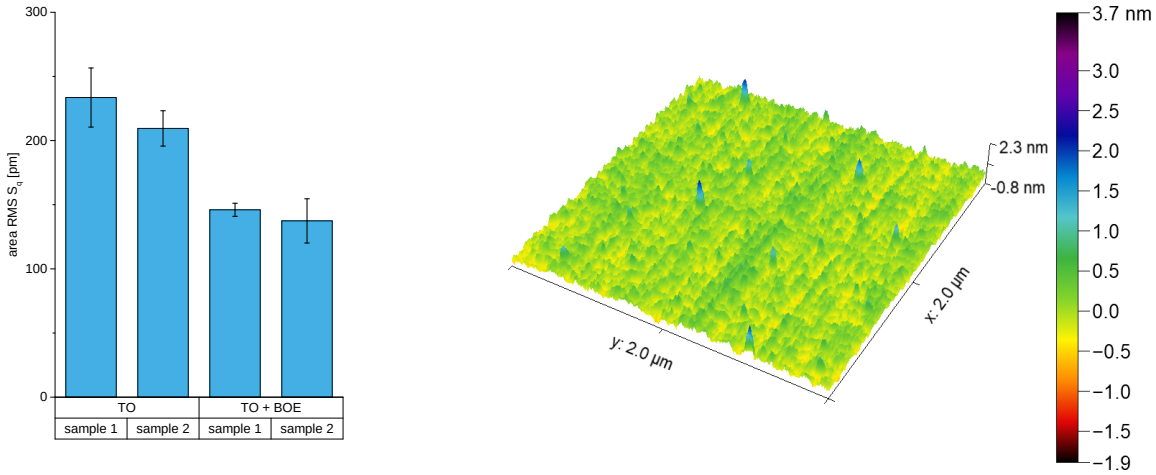


Figure 2: Area root mean square roughness (RMS) S_q for each of the Si thickness reduction methods. For each bar an individual sample was fabricated.



(a) (b)

Figure 3: a) RMS roughness S_q of TO before and after BOE etching and b) surface of TO before BOE etching. For each bar an individual sample was fabricated.

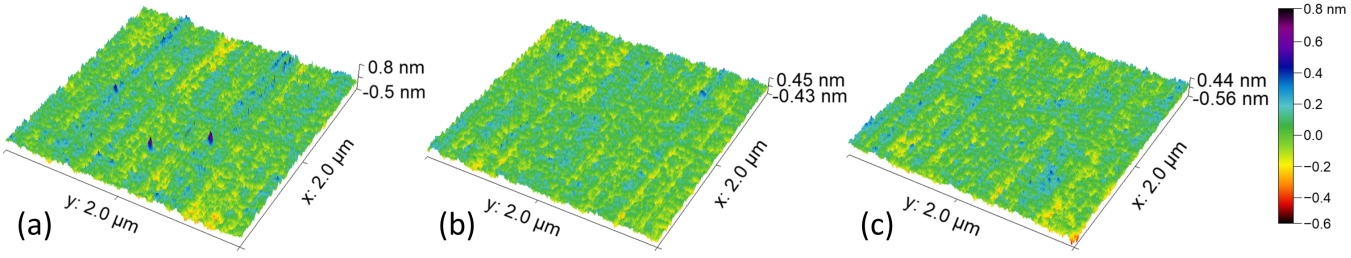
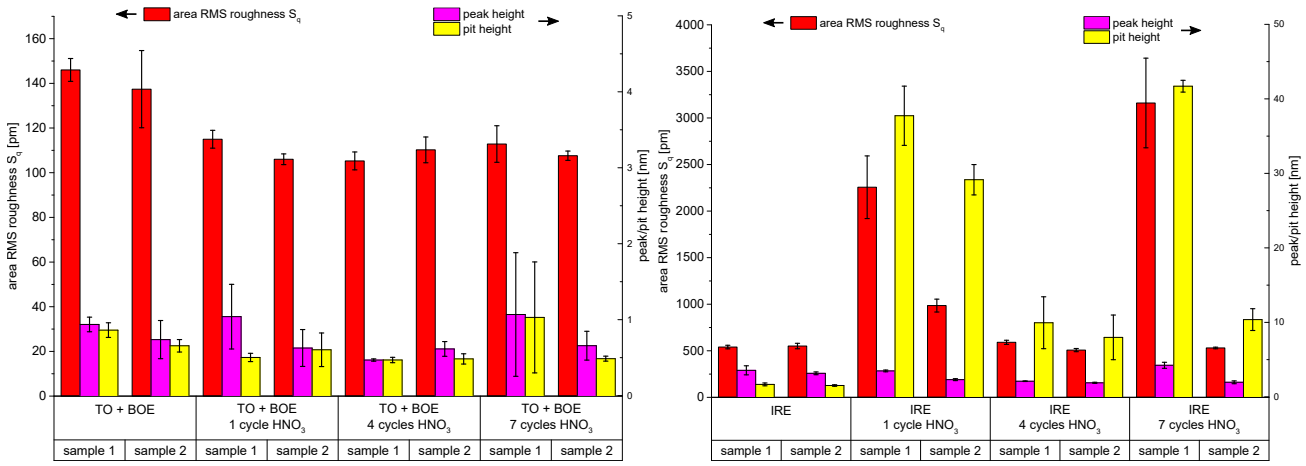


Figure 4: TO and BOE etched Si samples, which were subsequently digitally etched by oxidizing in HNO_3 (69.6 % HNO_3 and DI-water in a ratio 59:41) at 108 °C for 10 min and etching in 1 % HF. Surface of samples etched for a) one cycle, b) four cycles and c) seven cycles.

Table 2: ICP-PECVD process for the deposition of SiO_2 at 350 °C.

Step	t [s]	p [mTorr]	P_{RF} [W]	P_{ICP} [W]	N_2 [sccm]	O_2 [sccm]	He [sccm]	10 % SiH_4 [sccm]
Deposition	30	100	7	50	0	60	150	25
H reduction 1	180	30	0	600	0	100	100	0
H reduction 2	240	30	0	1000	0	100	100	0



(a) (b)

Figure 5: Comparisson of the RMS roughness S_q (red bar corresponding to the left y-axis), peak height (magenta, right axis) and pit height (yellow, right axis) after thinning down Si by a) TO and BOE etching with b) IRE after thinning down and digital etching for one, four and seven cycles. For each bar an individual sample was fabricated.

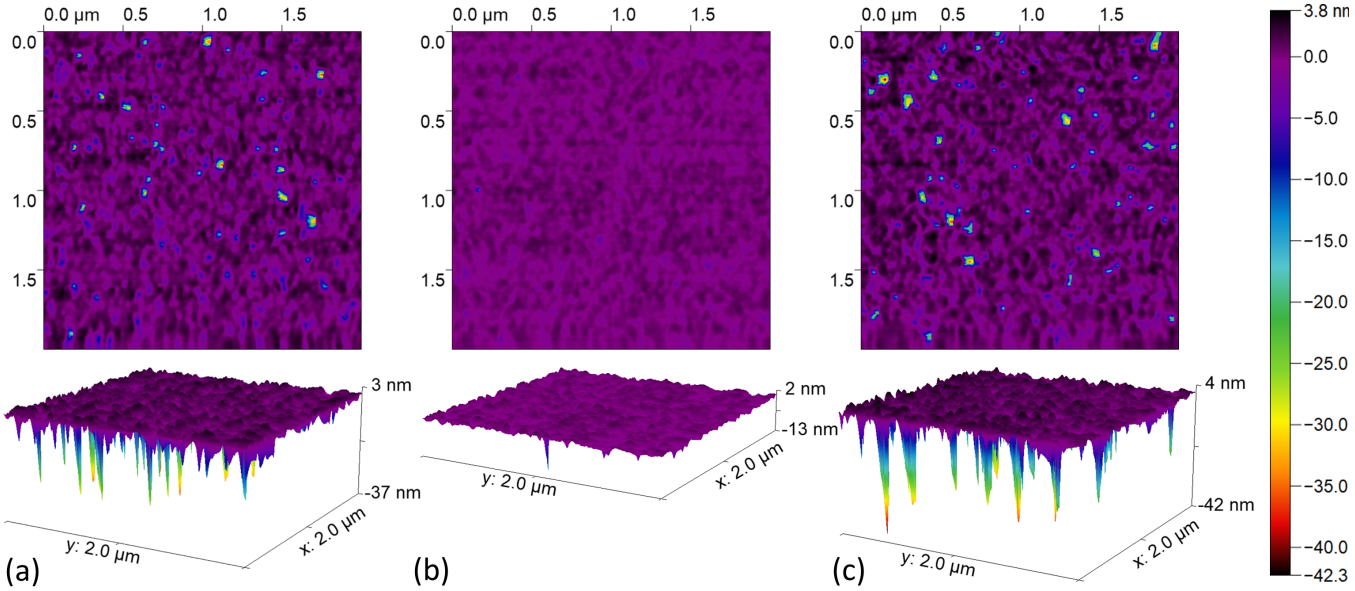


Figure 6: IRE etched Si samples, which were subsequently digitally etched by oxidizing in HNO_3 (69.6 % HNO_3 and DI-water in a ratio 59:41) at 108 °C for 10 min and etching in 1 % HF. Surface of samples etched for a) one cycle, b) four cycles and c) seven cycles.

Table 3: 3 steps of the ICP-DRIE process at 10 °C.

Step	t [s]	p [mTorr]	P_{HF} [W]	P_{ICP} [W]	SF_6 [sccm]	C_4F_8 [sccm]
Deposition	2	20	0	1750	5	100
Breakthrough 1	2	35	55	1750	250	5
Etching	4	50	0	2950	500	5

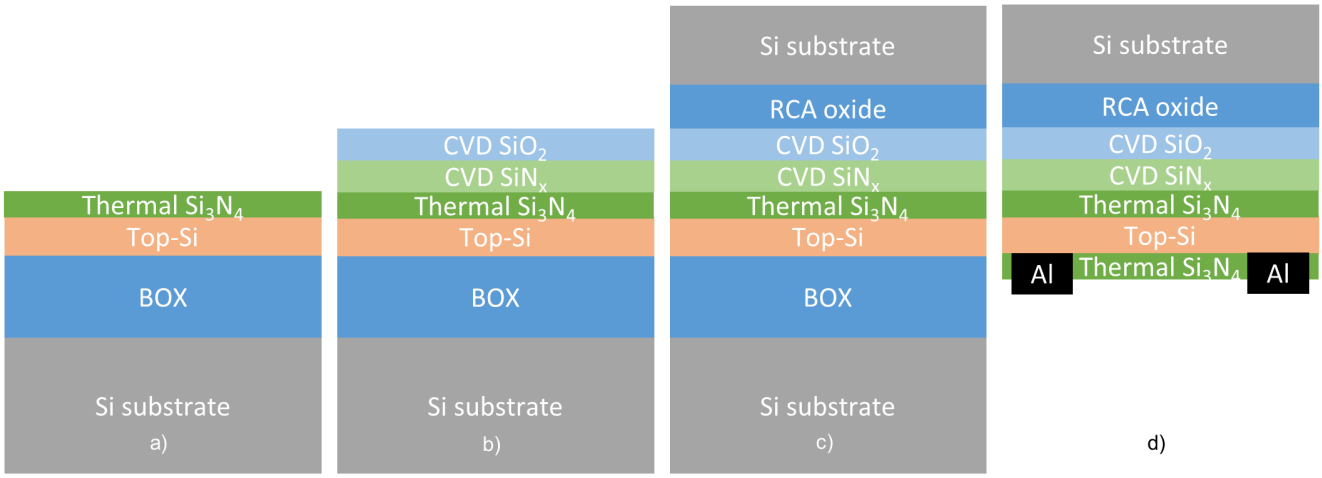


Figure 7: Selected schematic cross sections during fabrication of Si-NWs embedded in Si_3N_4. The layers are not to scale. a) Sample after thinning down of the top-Si and with the first layer of thermal Si_3N_4. b) After the deposition of 24 nm SiN_x and 80 nm SiO_2 by ICP-PECVD. c) After polishing the CVD deposited SiO_2 and RCA cleaning, the SOI sample is bonded to a piece of bulk-Si . d) After removing the SOI-substrate by ICP DRIE and the BOX with BOE, nitridation in an RTP and deposition of contacts directly onto the Si-NW.

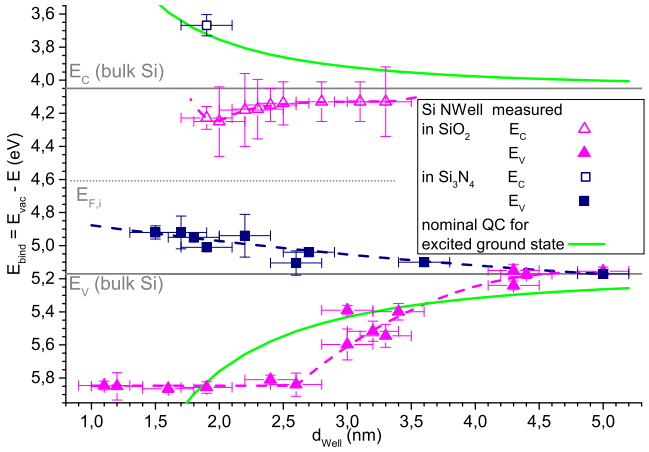
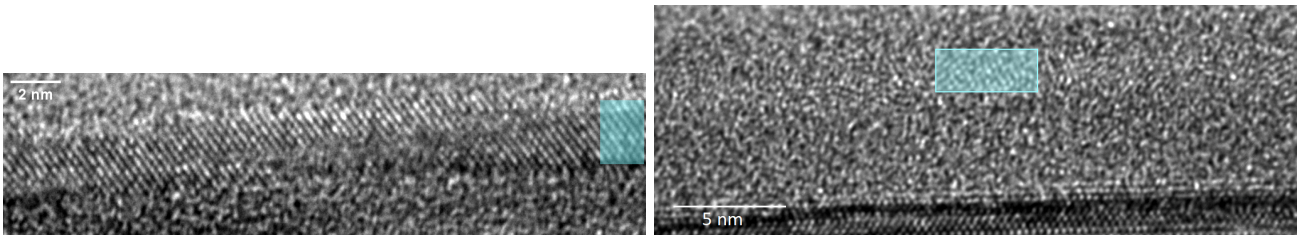


Figure 8: Electronic structure of the valence (UPS) and conduction (XAS-TFY) band of Si-NWs thinner than 5 nm embedded in SiO_2 (magenta squares) and the valencen band for Si nano crystals in Si_3N_4 (blue triangles) with respect to the vacuum energy. The dashed lines only act as a guide to the eye. The measured energies are shifted with respect to the binding energies expected by only taking quantum confinement and the respective partition of the exciton binding energy (solid green line) into account. Binding Energies for the valence and conduction band of Si-NWs in SiO_2 are higher than the energies of bulk-Si (solid grey lines), indicating n-type behavior, while the binding energy of the valence band edge of Si NWs in Si_3N_4 are lower than respective energies of bulk-Si, indicating p-type behavior. For more details refer to [10–13]. The data was acquired during multiple beam times and originally published here [11–13].



(a) (b)

Figure 9: HR-TEM cross section of Si embedded in Si_3N_4. a) Fabricated across 15 × 15 mm^2 by direct-bonding and etching through the Si-substrate and BOX with a thickness of (1.9 ± 0.3) nm, view along ⟨100⟩. b) Crystallized amorphous Si deposited by PECVD embedded in PECVD deposited Si_3N_4, resulting in poly-crystalline Si and a notable fraction of amorphous Si (cyan area) [modified and adapted under common license from [10]].

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Data availability
Data available on request.

Conflict of interest
The authors declare no conflicts of interest.

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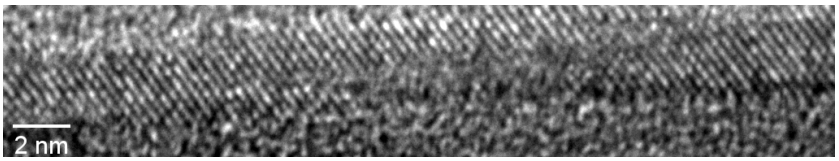

Starting from silicon on insulator the fabrication of ultrasmall crystalline Si-nanowells embedded in Si_3N_4 homogenously across 15 × 15 mm^2 samples via direct-bonding has been demonstrated. The fabricated samples will be used to investigate the nanoscale electronic structure shift induced by anions at surfaces (NESSIAS), measuring the position of the conduction and valence band using UPS and XAS at a synchrotron.

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