A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology

A. R. Cabrera-Galicia *, A. Ashok *, P. Vliex *, A. Kruth *, A. Zambanini *, S. van Waasen *†
* Central Institute of Engineering, Electronics and Analytics, Electronics Systems (ZEA-2),
Forschungszentrum Jülich GmbH, 52428 Jülich, Germany
Email: {a.cabrera.galicia, a.ashok, p.vliex, a.kruth, a.zambanini, s.van.waasen }@fz-juelich.de
† Faculty of Engineering, Communication Systems, University Duisburg-Essen, 47057 Duisburg, Germany

***Abstract*—High performance ICs (Integrated Circuits) operating at cryogenic temperatures will be a fundamental part of future quantum computers, providing precise manipulation of a large number of qubits [1], [2]. However, these ICs will need regulated and stable supply voltages in situ for optimum operation due to their mixed signal nature [3], [4]. Accordingly, this paper presents the design and cryogenic electrical characterization of a voltage regulator with an integrated voltage reference. Together, the circuits can generate a regulated voltage of 1.15 V with up to 10 mA of output current capability at 6 K. The investigated circuits exploit two cryogenic MOS transistor phenomena, the threshold voltage (V_{th}) saturation and the transconductance (g_m) increase. The circuits were developed in 22 nm FDSOI technology.**

***Index Terms*—CMOS, fully depleted silicon-on-insulator (FDSOI), cryogenics, voltage reference, voltage regulator, quantum computing.**

I. Introduction

The use of quantum physics phenomena at cryogenic temperatures, via the manipulation of a large number of qubits performed by a Quantum Computer (QC), promises to speed up the finding of solutions to computational challenges faced in drug design, cryptography and logistics. In addition, it has been demonstrated that ICs (Integrated Circuits) will be an important part of such a system and its scalability [1], [2]. However, the ICs belonging to a QC need a stable and defined supply voltage for proper operation due to their mixed signal nature [3], [4]; e.g. the phase noise of RF oscillators is highly dependent on their power supply quality [5]. This need will be challenging to satisfy in a large scale QC since the supply signals, going from the supply sources in the lab to the ICs inside the cryostat, are prone to supply voltage ripples, ground loops, electromagnetic interference from neighboring lines and dynamic load currents. A potential solution to this problem is the use of low noise supply sources with four-terminal sensing capability. However, this approach will not be practical in large scale QCs, where the number of interface connections between the lab equipment and the cryostat coldest area will be important assets. Alternatively, a regulated voltage could be generated inside the cryostat and be used to supply the ICs of the QC, while maintaining the power integrity of the system.

Hence, this paper presents the design and cryogenic electrical characterization of a voltage regulator and an integrated voltage reference that together can produce a regulated voltage at 6 K. Both circuits exploit two cryogenic MOS transistor phenomena, the threshold voltage (V_{th}) saturation and the transconductance (g_m) increase. The circuits have a verified operating range from 6 K to 50 K and were developed in a 22 nm FDSOI technology.

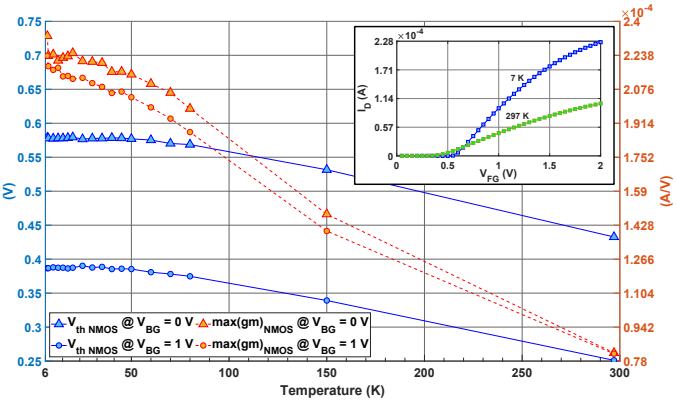


Fig. 1. V_{th} and maximum g_m of I/O NMOS ($W = 1\,\mu\text{m}$, $L = 0.32\,\mu\text{m}$) measured over temperature. Inset displays the I_{D} versus V_{FG} curve for 297 K and 7 K, at $V_{\text{DS}} = 0.1\,\text{V}$ and $V_{\text{BG}} = 0\,\text{V}$.

II. Cryogenic V_{th} Saturation and g_m Increase

As part of the circuit design methodology, an I/O NMOS transistor ($W = 1\,\mu\text{m}$, $L = 0.32\,\mu\text{m}$) was characterized versus temperature; details on the cryogenic DC characterization are reported in [6]. The circuits in this paper employ I/O transistors due to their higher voltage driving capability, in contrast to core transistors. For the device under test, Fig. 1 shows the evolution of its V_{th} and maximum g_m along temperature.

As expected, the device V_{th} increases with temperature reduction [7], [8]. However, V_{th} saturation starts at 60 K, with an average value of 578 mV. This phenomenon also occurs when the back gate of the device is set to 1 V, with a V_{th} saturation of 387 mV. The cryogenic V_{th} increase and saturation is attributed by [9] to the ionization energy increase and the carrier freeze-out. Furthermore, [10] argues that the cryogenic V_{th} behavior is due to the temperature dependence of the bulk Fermi potential and the density of interface traps. The V_{th} saturation has been reported for other technologies, among them a commercial 28 nm bulk CMOS technology [10]. While the cryogenic V_{th} saturation on 22 nm FDSOI technology is reported in [11], to the best of the authors knowledge, it has not being utilized

for the design of cryogenic analog circuits. Regarding the device g_m, its maximum value increases by 184 % at 7 K, compared to 297 K. A similar situation occurs when the device back gate is set to 1 V, but with a slight reduction of the g_m maximum value. The g_m increase at cryogenic temperatures is linked to the carriers mobility increase due to reduced phonon scattering; a phenomenon expected in NMOS and PMOS devices [10], [11].

III. Circuit Design and Electrical Evaluation

A. Voltage Reference

Cryogenic V_{th} saturation is employed as working principle by the voltage reference circuit shown in Fig. 2. The circuit is composed of beta-multiplier and self-bias V_{GS} current sources, that together bias a diode connected NMOS device to yield the reference voltage (V_{Ref}). The voltage reference circuit is simple and does not employ post-fabrication techniques to improve its V_{Ref} drift over temperature. It relies on the fact that a constant current biases and saturates the diode connected NMOS (M_{REF}), while the circuit is operated inside the V_{th} saturation temperature region. This is a common situation for ICs intended to be used in large scale QCs, since they are placed close to the physical quantum bits at environmental temperatures between 10 K and 4 K. Although self-heating is a concern at cryogenic temperatures, its effect is also proportional to the electrical power dissipated by the devices [12], [13]. Due to its low power dissipation, estimated to be 70 µW during the circuit design flow, a negligible self-heating is expected from this reference. Additionally, start-up circuits are used to prevent the current sources from latch-up. They can either operate autonomously or be manually triggered through configuration bits set via a JTAG interface.

A prototype chip micrograph is shown in Fig. 3(a); the voltage reference, voltage regulator and JTAG interface are included in the chip. The cryogenic experimental setup is displayed in Fig. 3(b). Inside it, prototype chips are mounted on PCBs specially designed for good thermal coupling with the cryostat cold head. In order to measure and control the PCB temperature, a sensing diode is attached to the PCB and monitored during the electrical tests. Due to the cryostat cooling power limitation, the lowest PCB temperature is 6 K. The measured response from a prototype reference circuit to a supply voltage (V_{Sup}) sweep is shown in Fig. 4 at 6 K. In specific, the output voltage (V_{Ref}) and supply current consumption (I_{Sup}), indicating that the circuit starts operating at V_{Sup} = 1.25 V with V_{Ref} = 576 mV and I_{Sup} = 38.3 µA. Fig. 5 shows the measured V_{Ref} over temperature, together with the V_{th} extracted from the I/O NMOS (Section II). As can be observed, V_{Ref} from sample 1 follows a trend similar to the one of the I/O NMOS V_{th} and deviates on average by 2.5 mV from it at temperatures between 6 K to 50 K. In total, 5 ICs containing a reference circuit were tested. The responses of these samples are shown in Fig. 5 and they differ slightly between each other, but all follow the I/O NMOS V_{th} trend over temperature. These measurements demonstrate the prototype reference practicality at environmental temperatures between 50 K and 6 K.

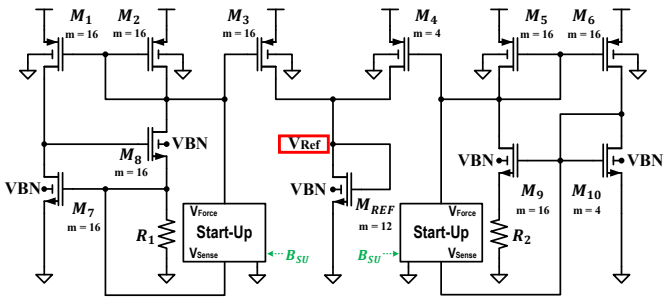
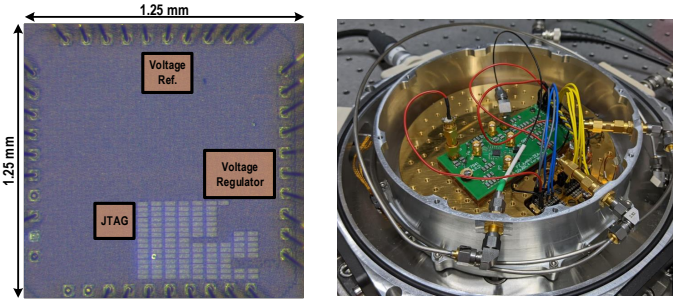


Fig. 2. Voltage reference based on cryogenic V_{th} saturation.



(a) (b)

Fig. 3. (a) Micrograph of a prototype chip. (b) Experimental setup: PCB with prototype chip, mounted onto the cryostat cold head.

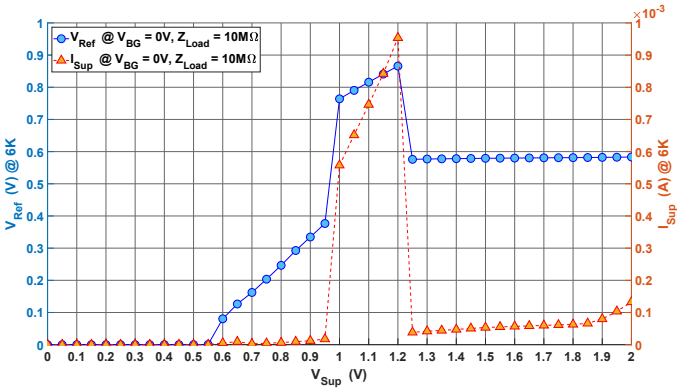


Fig. 4. Measured output voltage and current consumption of voltage reference (sample 1) with respect to supply voltage (V_{Sup}), at 6 K.

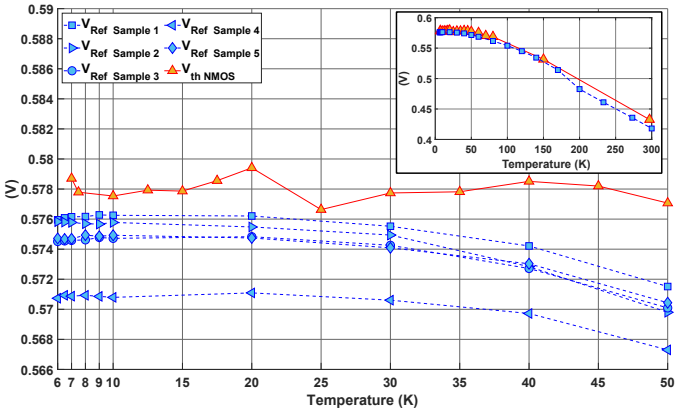


Fig. 5. Measured output from voltage reference over the temperature range of interest (6 K to 50 K), with V_{Sup} = 1.25 V and V_{BG} = 0 V; results correspond to 5 sample chips. Extracted V_{th} from I/O NMOS (W = 1 µm, L = 0.32 µm) is added for comparison. Inset displays sample 1 data over a wider temperature range (6 K to 300 K).

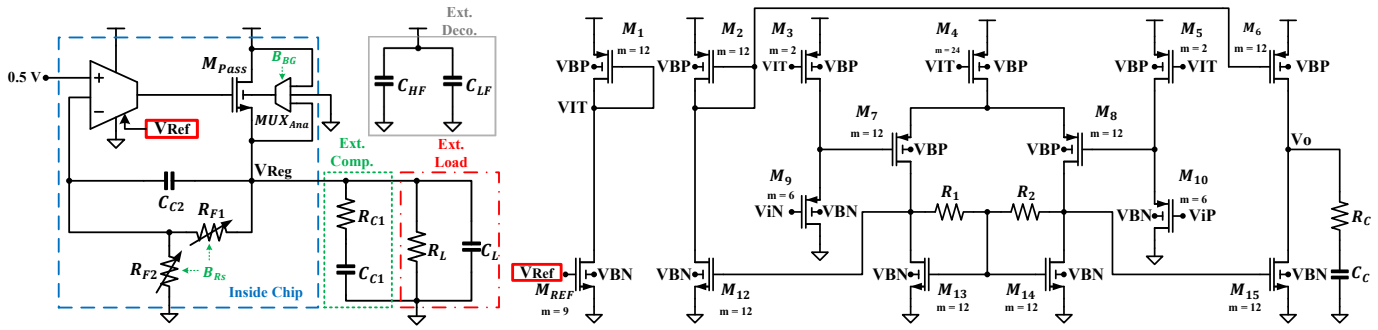


Fig. 6. Cryogenic voltage regulator. (a) The regulator is composed of an error amplifier, an NMOS pass element, a multiplexer and a resistive feedback network. Off-chip compensation elements (metal film based R_{C1} and polyphenylene-sulphide based C_{C1}), with stable electrical characteristics over temperature, are used to guarantee stability at cryogenic temperatures. (b) Differential amplifier used by regulator; its tail current is biased by cryogenic reference (Fig. 2).

B. Voltage Regulator

A circuit diagram describing the voltage regulator, designed for cryogenic temperatures, is shown in Fig.6(a). The regulator employs an NMOS pass element whose back-gate terminal connection can be shifted through an analog multiplexer controlled via JTAG. In this way it is possible to compensate for the V_{th} increase experienced by the pass element at cryogenic temperatures and to reduce the supply voltage level required by the regulator to start its operation; threshold voltage tuning via the back-gate terminal is a characteristic offered by FDSOI MOS devices [14]. Although the use of an NMOS pass element will lead to a higher dropout voltage in contrast to a PMOS, it will also provide a superior power supply rejection ratio (PSRR); a requirement needed to supply high performance analog circuits [5], [15]. Additionally, the feedback resistors values (R_{F1} and R_{F2}) can be modified for output voltage tuning via JTAG programming. Moreover, a cryogenic-stable off-chip compensation network, made up of a metal film resistor ($R_{C1} = 6.25\,\Omega$) and a polyphenylene-sulphide film capacitor ($C_{C1} = 47\,\text{nF}$), guarantees the regulator stability at cryogenic temperatures [4].

The differential amplifier of the regulator, shown in Fig.6(b), employs voltage followers for level shifting at their inputs and resistive local common mode feedback at its core; its open loop gain (A_{DA}) is approximated by Eq. 1 [16]. Since the regulator loop gain (A_{LG}) is proportional to A_{DA} (Eq. 2), the load regulation (LR) and PSRR are also depending on A_{DA} via A_{LG} (Eq. 3 and 4) [15]. As A_{DA} is proportional to the g_m of the MOS devices, it is expected that at cryogenic temperatures its magnitude increases due to the g_m increase with temperature reduction (Section II), resulting in an improvement of the regulator LR and PSRR.

$$A_{DA} \approx g_{m_{7,8}} \cdot (R_{1,2} || r_{o_{7,8}} || r_{o_{13,14}}) \cdot g_{m_{12,15}} \cdot Z_{\text{out}} \quad (1)$$

$$A_{LG} \approx A_{DA} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \quad (2)$$

$$\text{LR} \approx \frac{1}{g_{m_{\text{M Pass}}} \cdot A_{LG}} \quad (3)$$

$$\text{PSRR} \approx \frac{1}{g_{m_{\text{M Pass}}} \cdot r_{o_{\text{M Pass}}} \cdot A_{LG}} \quad (4)$$

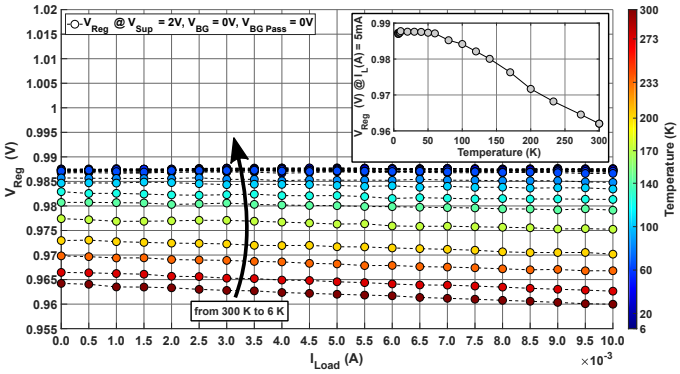
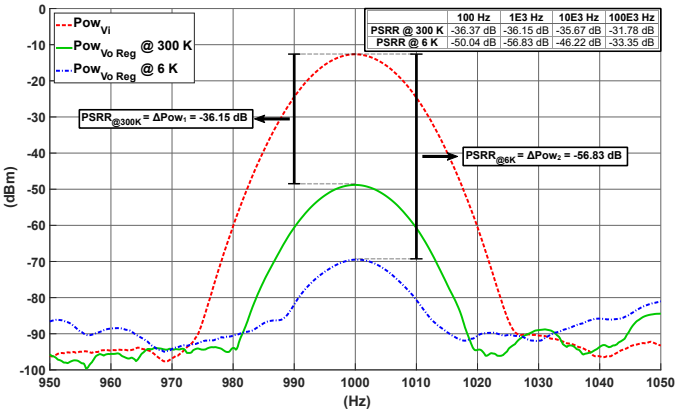


Fig. 7. Measured regulator output voltage (V_{Reg}) in relation to I_{Load} and temperature, at $V_{IN\ Ref} = 0.5\,\text{V}$, $R_{F1} = R_{F2}$, $V_{BG} = 0\,\text{V}$ and $V_{Sup} = 2\,\text{V}$. Inset displays the measured V_{Reg} at $I_{Load} = 5\,\text{mA}$, between 300 K and 6 K.

Fig. 7 shows the measured response of the prototype regulator in relation to load current (I_{Load}) and temperature, with $V_{IN\ Ref} = 0.5\,\text{V}$, $R_{F1} = R_{F2}$, $V_{BG} = 0\,\text{V}$ and $V_{Sup} = 2\,\text{V}$. $V_{IN\ Ref}$ is set to $0.5\,\text{V}$ by means of an external voltage source in order to evaluate the regulator performance in regard to temperature. The mean regulator output voltage (V_{Reg}) is $962\,\text{mV}$ at $300\,\text{K}$ and it increases to $987\,\text{mV}$ at $6\,\text{K}$. These changes signal to an increase in A_{LG} that reduces the regulator error and sets V_{Reg} closer to $1\,\text{V}$, the ideal output value; due to the amplifier input offset voltage, $V_{Reg} \neq 1\,\text{V}$. Similarly, the regulator LR changes from $424\,\text{mV/A}$ at $300\,\text{K}$, to $30\,\text{mV/A}$ at $6\,\text{K}$; an improvement in the form of a $92.92\,\%$ decrease.

The regulator PSRR is shown in Fig. 8 for $1\,\text{kHz}$, at $300\,\text{K}$ and $6\,\text{K}$. At $300\,\text{K}$, the measured PSRR is $-36.15\,\text{dB}$, while at $6\,\text{K}$ it is $-56.83\,\text{dB}$, corresponding to an improvement of $20.68\,\text{dB}$. The inset in Fig. 8 indicates the measured PSRR for additional frequencies. Based on the measurements previously described and Eq. (1) - (4), it can be inferred that the g_m increase is the main factor for the cryogenic improvement of the regulator LR and PSRR. Furthermore, Fig. 9 shows the regulator response to a voltage supply sweep at $6\,\text{K}$, with different pass element back-gate configurations. With the back-gate set to ground, the regulator needs $V_{Sup} = 1.75\,\text{V}$ to start operation. In contrast, by setting the back-gate to the supply rail, the regulator needs $V_{Sup} = 1.5\,\text{V}$ to operate. A reduction of $250\,\text{mV}$ is obtained. The regulator has an idle



	100 Hz	1E3 Hz	10E3 Hz	100E3 Hz
PSRR @ 300 K	-36.37 dB	-36.15 dB	-35.67 dB	-31.78 dB
PSRR @ 6 K	-50.04 dB	-56.83 dB	-46.22 dB	-33.35 dB

Fig. 8. Measured regulator PSRR via spectrum analysis at 1 kHz, for 300 K and 6 K, with $V_{\text{IN Ref}} = 0.5\,\text{V}$, $R_{\text{F1}} = R_{\text{F2}}$, $V_{\text{BG}} = 0\,\text{V}$ and $V_{\text{Sup}} = 2\,\text{V}$.

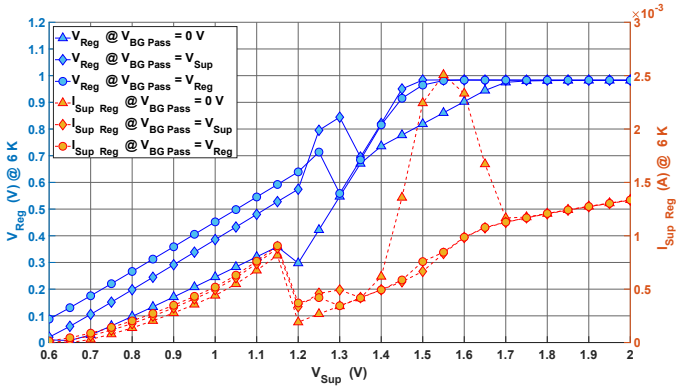


Fig. 9. Measured regulator output voltage (V_{Reg}) and supply current ($I_{\text{Sup Reg}}$) in relation to supply voltage (V_{Sup}) and several back gate settings for the NMOS pass element, at 6 K.

power consumption of 3.3 mW, produced by the enforced operation of the pass element in saturation due to cryogenic stability concerns. An improvement on power consumption can be attained by incorporating cryogenic simulation models into the regulator design flow. Unfortunately, cryogenic simulation models were not available for the development of the prototype chip presented in this paper. Despite this, the regulator is able to operate at temperatures between 300 K and 6 K.

C. Unified System for Cryogenic Voltage Regulation

Once verified the cryogenic characteristics of the reference and regulator circuits, their unified operation for voltage regulation is evaluated at 6 K with $V_{\text{IN Ref}} = V_{\text{Ref}} = 576\,\text{mV}$, $V_{\text{Sup}} = 2\,\text{V}$, $V_{\text{BG}} = V_{\text{Sup}}$, $R_{\text{F1}} = R_{\text{F2}}$ and $Z_{\text{Load}} = 220\,\Omega$; one supply rail biases both circuits. The transient response measured from the system to a supply voltage pulse is shown in Fig. 10 and it is stable. The system delivers the regulated output voltage after 27 ms due to slow response from the voltage reference circuit. Under static supply conditions, $V_{\text{Reg}} = 1.15\,\text{V}$ and $I_{\text{Sup}} = 6.54\,\text{mA}$. The measured LR of the system is $320\,\text{mV/A}$, a value bigger than the result presented in Section III-B for 6 K, due to $V_{\text{IN Ref}} \neq 0.5\,\text{V}$.

IV. Conclusions

The design and cryogenic characterization of a voltage reference and a voltage regulator, is reported in 22 nm FDSOI.

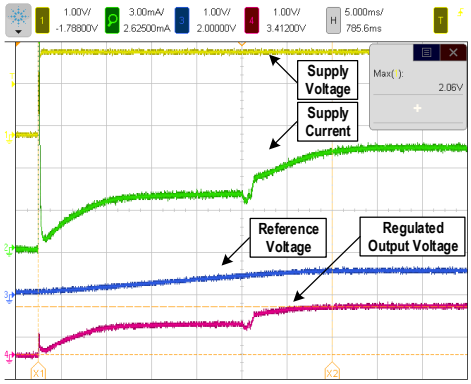


Fig. 10. Measured transient response from the unified system for voltage regulation to a supply pulse with 2 V amplitude, at 6 K.

TABLE I
VOLTAGE REFERENCE COMPARISON WITH STATE OF THE ART.

	Najafizadeh, et al., EDL, 2009	Homulle, et al., SSCL, 2018	van Staveren, et al., ESSCIRC, 2019		Voltage Reference in this work
Technology	SiGe BiCMOS	40 nm CMOS	40 nm CMOS		22 nm FDSOI
Reference Device	SiGe HBT	Thick oxide DTMOS	PMOS	DTMOS	NMOS
Operative Temp. Range	0.7 K – 293 K	4 K – 300 K	4 K – 300 K	4 K – 300 K	6 K – 50 K
VSup min.	3.3 V	1.8 V	0.97 V	0.9 V	1.25 V
VRef	1.156 V @ 0.7 mK	0.81 V @ 4 K	0.71 V @ 4 K	0.6 V @ 4 K	0.576 V @ 6 K
Power Consumption	130.35 µW	132 µW	7.37 µW	7. 26 µW	47.88 µW
Line Regulation	Not provided	8.3 %/V	1.2 %/V	1.1 %/V	1.652 %/V @ Z_{LOAD} = 10MΩ, VSup = [1.25 V, 2 V]
Temperature Coefficient	160 ppm/K	834 ppm/K	539 ppm/K	436 ppm/K	300 ppm/K @ Temp = [6 K, 50 K]
PSRR	Not provided	-23.4 dB @ 4 K	Not provided	Not provided	-46.14 dB @ 6K, 1 kHz
Area	Not provided	0.0004 mm²	0.009 mm²	0.009 mm²	0.006 mm²

TABLE II
VOLTAGE REGULATOR COMPARISON WITH STATE OF THE ART.

	Homulle, et al., Cryogenics, 2018		Voltage Regulator in this work
Technology	Discrete components based design		22 nm FDSOI
Pass Element	NMOS (TSM2314)		NMOS
Nominal VSup	VDD = 3.3 V (Error Amp.) VIN = 1.5 V (Pass Element)		2 V
Error Amp.	AD8605	TLV271	Custom
VReg	1.0086 V @4 K, V_{REF} = 0.6 V, Z_{LOAD} = 100Ω	1.0106 V @4 K, V_{REF} = 0.6 V, Z_{LOAD} = 100 Ω	0.987 V @6 K, V_{REF} = 0.5 V, VBGPass = 0V, I_{LOAD}= 5mA
Idle Power Consumption	4.46 mW @4 K	0.1 mW @4 K	3.3 mW @6 K
Max. Load Current	300 mA @4 K	300 mA @4 K	10 mA @6 K
Load Regulation	1.59 mV/A @4 K, I_{LOAD} = [0 A, 300 mA]	0.81 mV/A @4 K, I_{LOAD} = [0 A, 300 mA]	22 mV/A @6 K, I_{LOAD} = [0 A, 10mA], V_{REF}= 0.5 V, VBGPass=0V, VSup = 2 V
PSRR	-75.1 dB @4 K, V_{REF} = 0.6 V, Z_{LOAD} = 100Ω, 1 kHz	-76.4 dB @4 K, V_{REF} = 0.6 V, Z_{LOAD} = 100 Ω, 1 kHz	-56.83 dB @6 K, V_{REF} = 0.5 V, VBGPass = 0V, VSup = 2 V, 1 kHz
Area	Not provided	Not provided	0.075 mm²
Build-in VRegTuning	No	No	Yes

The circuits make an effective use of the cryogenic V_{th} saturation and g_m increase experienced by the MOS devices, as demonstrated in Section III. A comparison between the circuits in this paper and the state of the art is given in Tables I and II [4], [17], [18], [19]. The reference is simple and has a competitive temperature coefficient of 300 ppm/K, when operated between 50 K and 6 K. The regulator LR and PSRR fall behind the state of the art values. However, the regulator in this paper operate with lower V_{Sup} and, excluding the compensation network, its components are integrated on chip. Furthermore, with the circuits unified operation it is possible to generate a regulated voltage of 1.15 V at 6 K with

maximum output current capability of $10\,\mathrm{mA}$. Finally, the studied circuits served as exploration vehicles to gain insight into the design and electrical characterization of cryogenic analog integrated circuits, allowing the design of optimized cryogenic circuits in the future.

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