Evaluation of Cryogenic Models for FDSOI CMOS Transistors

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Scalable quantum computers demand innovative solutions for tackling the wiring bottleneck to control an increasing number of qubits. Cryogenic electronics based on CMOS technologies are promising candidates which can operate down to deep-cryogenic temperatures and act as a communication and control interface to the quantum layer [1,2]. However, the performance of transistors used in these circuits is altered significantly when cooling from room temperature to cryogenic temperatures, which motivates accurate cryogenic modeling of transistors.

We will report on cryogenic models tailored specifically for fully depleted silicon-on-insulator (FDSOI) transistors. We performed extensive DC characterization of transistors with subsequent modeling using the BSIM-IMG 102-9.6 model, which is the first version with a built-in cryogenic extension [3]. The preliminary models effectively represent the DC device behavior from 7 K up to room temperature. These models are used in industry standard EDA and simulation software, like Cadence Spectre. With the presented cryogenic models, we will show simulations at cryogenic temperatures. We will also compare the simulation results with the measured performance of a test chip in the temperature range from 7 K up to room temperature.

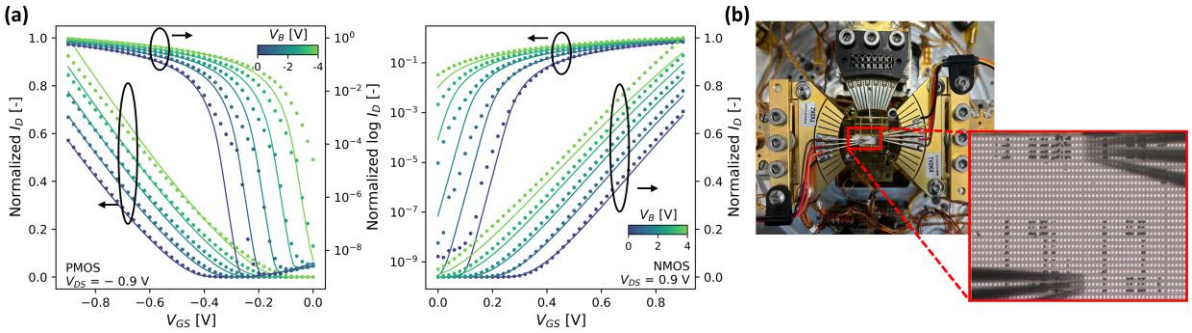

Fig. 1: (a) *Measured (markers) and modeled (lines) transfer characteristics of a short-channel PMOS and NMOS transistor for different back gate bias (V_B) at T = 7 K. (b) Measurement setup inside the cryogenic chamber along with a micrograph of the die.*

References

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3. Hu, Chenming, et al, Woodhead Publishing, 2019.

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