Effect of Transistor Transfer Characteristics on the Programming Process in 1T1R Configuration

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***Abstract*— The one-transistor-one-resistor (1T1R) structure has been widely used in the context of novel neuromorphic applications. It can effectively control the state variability in redox-based resistive random access memory (ReRAM) and suppress the leakage current in ReRAM arrays. Since the transistor size has a direct impact on the electrical behavior, matching the characteristics of the two components in the 1T1R structure is a crucial step at the beginning of the device design. In this article, we focus on valence change mechanism (VCM)-type ReRAM devices and investigate the effect of the transistor transfer characteristics on the programming characteristics of 1T1R structures. By comparing the electrical behavior of three types of 1T1R structures with different transistor sizes during a gradual SET switching algorithm, we analyze how the applied voltage is distributed between the ReRAM cell and the transistor. Furthermore, the relationship among the transistor size, the operating region, and the bias conditions is explored based on the JART VCM v1b compact model. Finally, we discuss the effects of these factors on the programming characteristics of 1T1R structures and provide design suggestions regarding transistor size and bias conditions.**

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***Index Terms*— Bias conditions, one-transistor-one-resistor (1T1R), programming algorithm, redox-based resistive random access memory (ReRAM), transistor sizes, voltage division.**

I. Introduction

REDOX-BASED resistive random access memory (ReRAM) has recently received increasing attention for the potential as artificial synapses in neuromorphic computing [1], [2], [3], [4]. As the basic working elements of ReRAM arrays, one-transistor-one-resistor (1T1R) structures can be programmed to different resistance levels, since the transistor can act as an effective current compliance regulated by the gate voltage. To achieve multibit information storage and improve the accuracy of inference tasks, the programming method by a stepwise increase in the gate voltages has been widely used to fine-tune the conductive levels of the ReRAM cells [5], [6], [7]. By adjusting the growth increment of the voltage steps, the pulsewidth, and the starting voltage, the programming method can be optimized to achieve a balance between energy consumption, programming time, and accuracy [8], [9].

However, among the numerous 1T1R structures reported so far, the transfer characteristics of the transistors vary [10], [11], [12]. This directly translates into different voltage parameters for programming. Considering that transistors with different *W/L* ratios have different transfer characteristics, it is necessary to investigate the influence of transistor transfer characteristics on the electrical performance of 1T1R structures [13].

In this article, 1T1R structures with three different *W/L* ratio transistors are investigated. The influence of the transistor characteristics on the switching behavior of the valence change mechanism (VCM)-type ReRAM devices is discussed by extracting the intrinsic voltage drop in the memristive device versus the current. Furthermore, the evolution of the electrical characteristics of the three types of 1T1R structures during the SET process is compared using a predefined programming verify algorithm. Furthermore, the JART VCM v1b compact model is used in the 1T1R structures based on which the relationship between bias condition in the SET process and device

TABLE I
DIMENSIONAL INFORMATION FOR THE TRANSISTORS

Transistor Type	Width	Length	*W/L*
T-1	10 µm	500 nm	20
T-2	10 µm	10 µm	1
T-3	220 nm	500 nm	0.44

conductance is matched. Finally, the performance of three types of 1T1R structures is discussed regarding resistance ratio and variability control. Suggestions on the *W/L* ratio are given for transistor size design according to the requirements of different applications.

II. EXPERIMENT AND METHODOLOGY

A. Device Information

The 1T1R structures used in this study are our previously reported Pt/HfO_2/TiO_x/Ti-based VCM cells [4], [14], [15], [16] connected in series with n-type transistors in a 0.18-μm CMOS technology, which are fabricated in collaboration with X-FAB semiconductor foundries GmbH. The Pt electrode is called the active electrode due to its higher metal work function and forms a Schottky-type contact with the HfO_2 switching layer, while the other electrode is called ohmic electrode (OE). In this work, the active electrode of the VCM cell connects with the transistor. There are three *W/L* ratio transistors involved in this work, 20 ($W = 10$ μm, $L = 500$ nm), 1 ($W = 10$ μm, $L = 10$ μm), and 0.44 ($W = 220$ nm, $L = 500$ nm). All the dimensional information for the transistors are detailed in Table I. Next, we will refer to each of the three types of transistors as T-1, T-2, and T-3. Both the width and length of the transistor channel affect the transistor's ability to control the flow of charge carriers, which in turn affects its electrical behavior [17]. A wider channel allows more charge carriers to flow, increasing the transistor's current-carrying capacity. A shorter channel allows for faster switching times and can further reduce the resistance encountered by the carriers. However, the shorter channel may introduce nonideal behavior, such as channel length modulation and short-channel effects. In short, when the same gate voltage is applied, the allowed current values are expected to be T-1 > T-2 > T-3.

B. Calculation of Intrinsic ReRAM Voltage

The experiment was performed using the aixACCT Systems, aixMATRIX measurement tool, used in single-cell mode comprising four arbitrary waveform generators [18]. The biasing scheme for switching the 1T1R structures is shown in Fig. 1(a). 1T1R structures with n-type transistors cannot be operated with negative voltages because the bulk is always grounded when the transistor is in operation. To switch the VCM cell from a high resistive state (HRS) to a low resistive state (LRS), i.e., SET process, a positive voltage (V_{1T1R}) is applied to the OE, while the drain is grounded. In this configuration, the voltage at the source terminal equals the voltage drop over the transistor $V_{TR,SET}$. The electrical characteristics of the transistor follow its transfer characteristics because the channel is fully controlled by the gate voltage. For the reversed process, i.e., the RESET operation, a positive voltage is applied to the drain (V_{1T1R}), while the OE is grounded.

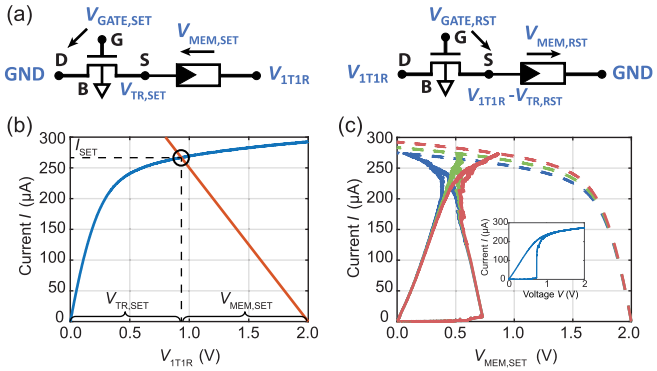

Fig. 1. (a) SET and RESET bias scheme of the 1T1R structure. (b) Transistor load line concept including the transistor characteristic (blue curve) and the load line (red curve). (c) Method for determining the effective gate voltage. Transistor characteristics (dashed lines) and the corresponding derived current versus cell voltage curves (solid lines). The three dashed lines correspond to the effective gate voltage plus 10 mV (red curve), the effective gate voltage (green curve), and the effective gate voltage minus 10 mV (blue curve). (inset) The *I–V* sweep curve of the SET part for cell voltage calculation.

In this configuration, the control of the channel via the gate voltage is weakened because the voltage at both the drain and the source node is nonzero. In other words, the transistor exhibits the body effect and its transfer characteristics become more complex [19]. In this article, only the calculation of the intrinsic voltage of the VCM cell during the SET process is discussed.

The intrinsic voltage of the VCM cell in the 1T1R structure can be calculated based on the transistor load line concept, as shown in Fig. 1(b) [19], [20]. Considering the VCM cell as the load of the transistor, the intersection of the transistor transfer characteristics and the load line is the operating current of the 1T1R structure. The abscissa of the intersection equals $V_{TR,SET}$, and the difference between the x-intercept of the load line and the abscissa of the operating current is the intrinsic voltage value on the VCM cell. According to this concept, the divided voltage over the transistor and the VCM cell can be calculated if the respective transfer characteristic curve and the actual current value of the transistor are known. However, the transistor characteristics cannot be measured after 1T1R integration. Therefore, it is necessary to estimate them based on the measurements of single transistor structures. In addition, the actual effective gate voltage in the 1T1R structures often shows a minor deviation from the applied voltage due to process or test conditions, which can cause a large error in the calculation results.

The effective gate voltage can be determined by plotting the SET current over the intrinsic voltage curve for the same *I–V* sweep curve at different assumed gate voltages, as shown in Fig. 1(c). The three solid curves in Fig. 1(c) depict the current over the cell voltage calculated from the same *I–V* sweep curve (shown in the inset) based on different transistor transfer characteristics (dashed lines). Although all the three curves exhibit snap-back shapes, it is generally accepted that the voltage value corresponding to the green dashed line refers to the effective gate voltage of the transistor [21]. This is because the cell voltage should remain constant when the transistor operates as current compliance after abrupt SET

TABLE II
COMPACT MODEL PARAMETERS FOR THE HfO_x DEVICES

$A_{det} = \pi r^2 = 1.96 \cdot 10^{-15}$ m^2	$r_{det} = 25$ nm
$N_{disk,\,min,\,det} = 0.0002 \cdot 10^{26}$ m^{-3}	$N_{disk,\,max,\,det} = N_{plug} = 20 \cdot 10^{26}$ m^{-3}
$l_{cell} = 3$ nm	$l_{det} = 0.4$ nm
$l_{plug} = 2.6$ nm	$a = 0.25$ nm
$R_{series} = 1.37$ kΩ ($I = 0$ µA)	$R_{series} = 1.46$ kΩ ($I = 700$ µA)
$R_{line} = 719$ Ω ($I = 0$ µA)	$R_{line} = 810$ Ω ($I = 700$ µA)
$R_{TiOx} = 650$ Ω	$\Delta W_A = 1.1$ eV
$\nu_0 = 5 \cdot 10^{12}$ Hz	$\mu_n = 4 \cdot 10^{-6}$ m^2/Vs
$R_{th0,\,SET} = 3 \cdot 10^6$ K/W	$R_{th0,\,RESET} = 1 \cdot 10^6$ K/W
$e\phi_{Bn0} = 0.18$ eV	$e\phi_n = 0.1$ eV
$R_{th,\,line} = 90471.47$ K/W	$R_0 = 719.24$ Ω
$\alpha_{line} = 3.92 \cdot 10^{-3}$ 1/K	$C_{th} = 1 \cdot 10^{-14}$ J/K
$e = 1.6 \cdot 10^{-19}$ C	T_0 293 K
$A^* = 6.01 \cdot 10^5$ A/m^{2}K^2	$z_{Vo} = 2$
$k_B = 1.38 \cdot 10^{-23}$ J/K	$\varepsilon_0 = 8.854 \cdot 10^{-12}$ As/Vm
$\varepsilon_{\phi_B} = 5.5 \cdot \varepsilon_0$	$\varepsilon = 17 \cdot \varepsilon_0$
$h = 6.626 \cdot 10^{-34}$ Js	$m^* = 9.11 \cdot 10^{-31}$ kg

occurred, rather than changing drastically as shown by the blue and red solid curves. It should be noted that the gate voltage corresponding to the blue and red dashed line differs from the effective gate voltage by only 10 mV. This phenomenon indicates that the effective gate voltage value obtained by this method can accurately reflect the actual gate voltage of the transistor in the 1T1R structures. In addition, it shows that a minor deviation of the gate voltage can cause a huge error in the calculation results of the cell voltage. The compensation value of the gate voltage is defined as the difference between the applied gate voltage and the effective gate voltage. By selecting different applied gate voltages for multiple 1T1R structures, the compensation value is found to remain constant for the same structure. Different 1T1R structures have different compensation values. Therefore, it is valid to use the compensation values for the same 1T1R structure to calculate the cell voltage for different gate voltages.

C. Simulation Model

For the simulations, we used the physics-based JART VCM v1b compact model which was shown to be able to describe various filamentary VCM systems like ZrO_x and HfO_x [15], [19], [22]. The device stack structure is approximated by the model structure. The active electrode interface is modeled as a Schottky diode with the SET direction current being described via thermionic field emission and the RESET direction being described by thermionic emission. The switching layer is split into a disk region near the active electrode interface and a plug region near the OE. The disk region has a variable resistance, modulated by the concentration of oxygen vacancies N_{disk}. The plug region is represented as a constant resistance. The OE and the resistances of the metal contact lines are modeled as current-dependent resistances. All the model parameters are detailed in Table II. For explanation of the physical meaning behind the parameters, we refer the reader to [15].

The model version used for this article differs from the version presented in [15] in two ways. On one hand, we have added a dynamical temperature model which has also been used by other VCM compact models [23], [24]. This dynamical temperature model slows down the SET process as a change in the device power is not instantaneously transferred into a temperature change but rather with a thermal time

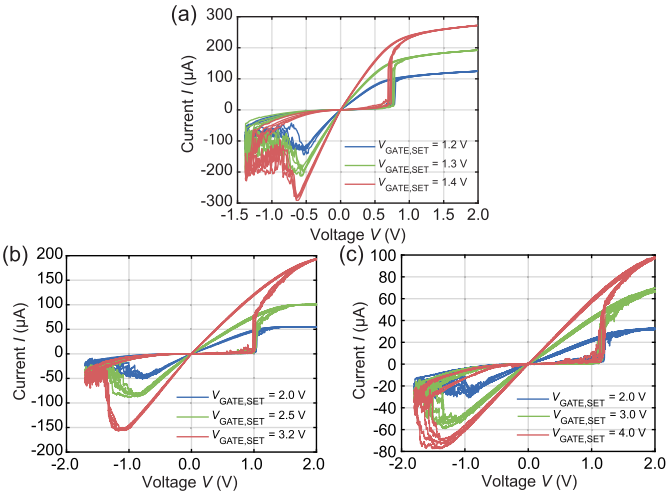

Fig. 2. Multilevel *I–V* characteristics of 1T1R structures with (a) T-1, (b) T-2, and (c) T-3.

constant made up of the thermal resistance R_{th} and the thermal capacitance C_{th}. This first change is physically reasonable and improves the numerical behavior of the model. The second change is that the thermal resistance in the SET direction is changed from a constant value to a function of N_{disk} as shown in (1). This second change also reduces the abruptness of the SET process and allows for better matching of the 1T1R characteristic as will be shown and further discussed in Section V. For all the simulations shown here, the model is only used as a deterministic model without variability

$$R_{th,SET} = R_{th0,SET} - \frac{N_{disk} \cdot (R_{th0,SET} - R_{th0,RESET})}{N_{max} - N_{min}}. \quad (1)$$

III. MULTILEVEL *I–V* SWEEPS OF 1T1R STRUCTURES

Fig. 2(a)–(c) shows the multilevel *I–V* sweeps of three types of 1T1R structures at a ramp rate of 1000 V/s. Three fixed gate voltages for the SET process ($V_{GATE,SET}$) are applied to each type of structure to provide different current compliance values (I_{cc}). There are five representative curves from a larger measurement set in each I_{cc}. The curves in each figure are from one 1T1R structure and different cycles. The *I–V* sweeps in Fig. 2(a) are from the 1T1R structure with T-1. The blue, green, and red curves correspond to $V_{GATE,SET}$ of 1.2, 1.3, and 1.4 V, respectively. $V_{GATE,RESET}$ is 5.0 V for all the measurements. The transistor works as current compliance after an abrupt SET occurred for all three I_{cc} levels. It should be noted that the 1T1R structure exhibits good linearity in both high and low conductance states within a small voltage range, which is critical for reading them in subsequent pulse measurements. The maximum currents in both the SET and RESET processes show good symmetry, which is in accordance with the universal switching behavior reported in [25].

The *I–V* sweep curves shown in Fig. 2(b) and (c) are from the 1T1R structures with T-2 and T-3, respectively. $V_{GATE,SET}$ in (b) is 2.0, 2.5, and 3.2 V, and in (c) is 2.0, 3.0, and 4.0 V. $V_{GATE,RESET}$ equals the sum of the RESET stop voltage and $V_{GATE,SET}$, which is 3.7, 4.2, and 4.9 V in (a), and 3.8, 4.8, and 5.0 V in (b). The maximum operating voltage of the transistors

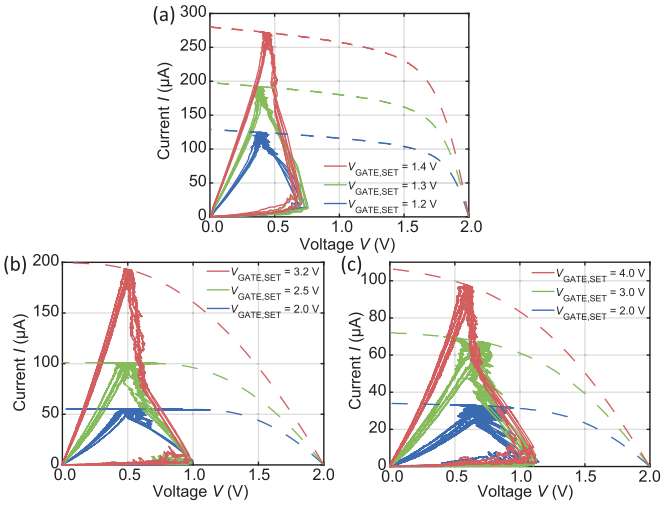

Fig. 3. Multilevel SET current over intrinsic voltage characteristics of 1T1R structures with (a) T-1, (b) T-2, and (c) T-3.

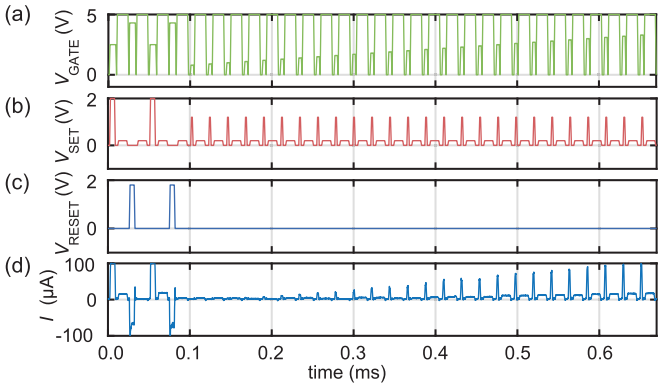

Fig. 4. (a)–(c) Defined voltage stimuli of the SET algorithm with two preparation cycles, program verify, and increasing Gate voltage. (d) Exemplary current response of the voltage stimuli shown above.

is 5.0 V. Compared with the previous results, these two types of transistors deliver a smaller range of current. In addition, only the blue curves in both the figures ($V_{GATE,SET} = 2.0$ V) show a well-controlled I_{cc} behavior. Whereas for the other two groups of curves, the current values keep increasing after the SET event until reaching I_{cc}. These phenomena indicate that the transistor continues to allow a larger current after the SET event, causing the conductance of the VCM cell to increase further. Overall, both the 1T1R structures in (b) and (c) show good linearity at multilevel states and symmetric maximum current levels. The maximum RESET current shown in the red curves in (b) and (c) is smaller than the maximum SET current. In both the sets of measurements, the gate voltage during RESET was near or at the maximum voltage of the transistor (5.0 V). Therefore, this exception is believed to be related to the limited conduction level of the transistor.

To further analyze the influence of the transistor transfer characteristics on the switching behavior of 1T1R structures, we calculated the voltage division of the transistor and the VCM cell according to the load line concept (see Section II-B). By subtracting the voltage drop over the transistor, the intrinsic I–V characteristics are derived from Fig. 2 and shown in Fig. 3. Here, only the branch in SET polarity is shown (solid lines), since the applied calculation is only valid in this regime. The corresponding transistor transfer characteristics are drawn as dashed lines. Fig. 3 shows a snap-back after the abrupt SET occurs, similar to the behavior reported by Fantini et al. [21]. This is caused by a significant reduction in the resistance of the VCM cell, whose intrinsic voltage decreases significantly, while more of the applied SET voltage is distributed to the transistor, allowing the current to increase. After the snap-back occurred, the intrinsic current–voltage characteristics of the 1T1R structures exhibit two types of behavior. One type, as shown in the blue curves of Fig. 3(a)–(c), is where the intrinsic voltage and current values remain at a fixed area in the coordinates. This is because as the applied SET voltage increases, the voltage dropped to the VCM cell keeps constant, and the current is limited by the transistor. In the other type, as shown by the green and red lines in Fig. 3(a)–(c), the intrinsic voltage remains approximately constant while the current continues to increase until it reaches its maximum value. This indicates that the transistor continues to allow the current increasing due to its characteristics until the applied voltage reaches to maximum.

Based on the above observations, we found that the transfer characteristic of the transistor not only determines the current range but also influences the selection of the voltage parameters, and ultimately makes a difference in the supply of I_{cc}. Since the VCM cells have a specific operating current range, the choice of $V_{GATE,SET}$ and the SET voltage (V_{SET}), which determines the transistor dividing voltage, must be carefully considered to match the electrical characteristics of the transistor and the VCM cell.

IV. Impact of Transistor Characteristics and Biasing Conditions on 1T1R Structures

To better understand the evolution of the voltage distribution during the SET process, we defined an SET algorithm as shown in Fig. 4(a)–(c). The algorithm consists of two initial preparation cycles, which end in a RESET condition, and 26 SET pulses. The SET pulses are 1-μs long with constant voltage. The amplitudes of the SET pulses (V_{SET}) are 2.0 and 1.2 V for 1T1R structures with T-1 and T-2, while 1.8 and 1.2 V for those with T-3. During the SET process, a series of gradually increasing $V_{GATE,SET}$ is applied with values starting at 0.8 V for all the transistors, while ending at 1.3 V for T-1, 3.3 V for T-2, and 4.8 V for T-3. Each SET pulse is followed by a READ pulse with 0.2 V in the same polarity as the SET voltage and 10-μs pulsewidth. During readout, a high gate voltage ($V_{GATE,READ}$) of 5.0 V is applied to ensure that the channel is sufficiently conductive. Fig. 4(d) shows an example of the current response corresponding to the applied voltage in Fig. 4(a)–(c). This algorithm is executed 200 times on 1T1R structures with each of the three transistor geometries.

Fig. 5(a) and (b) shows the statistics of the 200-cycle SET algorithm test for 1T1R structures with T-1. $V_{GATE,SET}$ in this experiment ranges from 0.8 to 1.3 V. The curves of $V_{TR,SET}$ and the cell voltage ($V_{MEM,SET}$) are obtained based on the median values of the SET current. Similar to a box plot, the darker shade represents the voltage values calculated based on the 25th and 75th percentiles of the SET current, and the lighter area is derived from the fifth and 95th percentiles of the SET

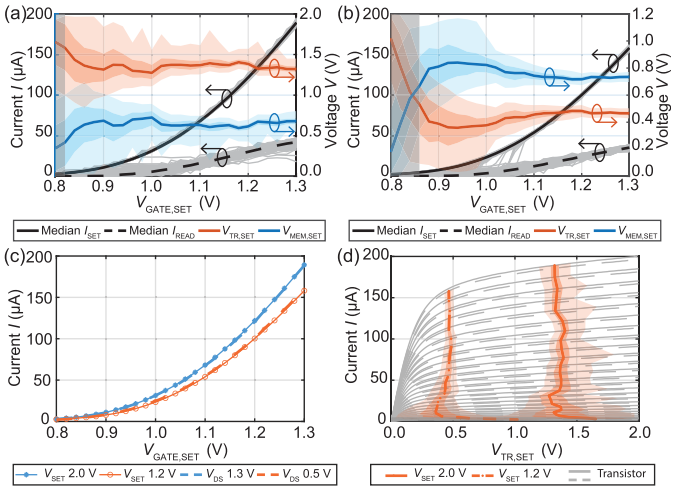

Fig. 5. Statistics for 1T1R structures with T-1. Evolution of the extracted $V_{MEM,SET}$ and $V_{TR,SET}$ corresponding to the SET and READ currents (gray lines) at V_{SET} (a) 2.0 and (b) 1.2 V. (c) Comparison between SET currents and transistor input characteristics. (d) Correlation among SET currents (red lines), $V_{TR,SET}$, and transistor transfer characteristics (gray lines).

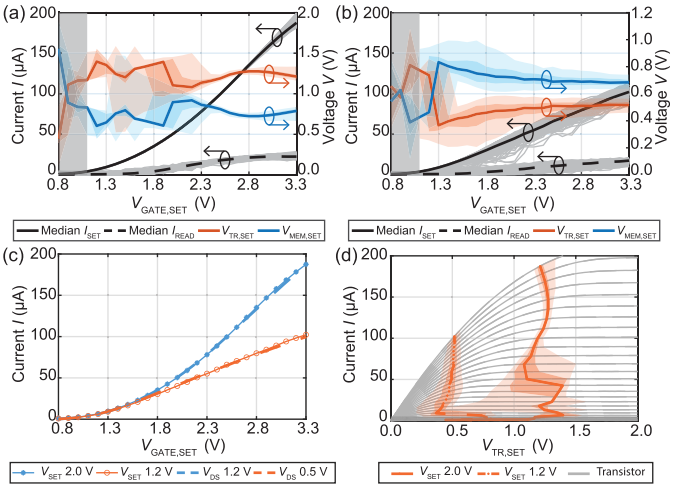

Fig. 6. Statistics for 1T1R structures with T-2. Evolution of the extracted $V_{MEM,SET}$ and $V_{TR,SET}$ corresponding to the SET and READ currents (gray lines) at V_{SET} (a) 2.0 and (b) 1.2 V. (c) Comparison between SET currents and transistor input characteristics. (d) Correlation among SET currents (red lines), $V_{TR,SET}$, and transistor transfer characteristics (gray lines).

current. Note that the wide area (95 percentile) may be not an actual device cycle-to-cycle variability, but is derived from the calculation. This is because $V_{TR,SET}$ obtained from the flat saturation region of the transistor can have a relatively large error. The area where the SET current is less than 5 μA is represented by the gray color on the left side of the figure. The voltage plots within this range may not be analyzed because the cell is not switched and the transistor is operated below its threshold voltage V_{th}.

As shown in Fig. 5(a), the SET current (black solid line) exhibits a nonlinear increase with $V_{GATE,SET}$. The READ current shows cycle-to-cycle variation, but its median (black dashed line) gradually increases with $V_{GATE,SET}$. In Fig. 5(b), the amplitude of the SET current is overall lower than that in (a), which is due to the smaller V_{SET}. In addition, there are some abruptly increased gray SET current curves for $V_{GATE,SET}$ between 1.0 and 1.1 V, indicating that a low V_{SET} shifts the switching characteristics to the voltage-limited regime and makes the SET process more probabilistic. Despite the different V_{SET} levels, $V_{MEM,SET}$ keeps constant at about 0.7 V. V_{SET} values mainly affect the voltage dropping over the transistor, which is about 1.3 V in (a), but around 0.5 V in (b). In other words, a high V_{SET} puts more stress on the transistor. Since the voltage shared by the transistor remains constant during SET processes, the SET current of the 1T1R structures coincides with the transistor input characteristics, as shown in Fig. 5(c). This means that it is possible to estimate the SET characteristics of 1T1R structures from the transistor input characteristics. Fig. 5(d) shows the load line curves of the transistor. The gray lines in the background show the characteristics of transistors from different V_{SET}-level experiments. The red lines (solid one for V_{SET} 2.0 V, dashed one for V_{SET} 1.2 V) represent SET currents. Their surrounding colored areas in the figure is derived in the same way as in Fig. 5(a) and (b). It shows that for both V_{SET} levels, the transistors are always operating in the saturation regime and therefore can effectively suppress the current variability during the SET process.

Fig. 6(a) and (b) shows the statistics of the 200-cycle SET algorithm test for 1T1R structures with T-2. $V_{GATE,SET}$ in this experiment ranges from 0.8 to 3.3 V. According to Fig. 6(a), the gray SET current curves from each cycle largely overlap with their median curve, and only show slight variation when $V_{GATE,SET}$ is increased to 3.3 V. However, in Fig. 6(b), the SET current shows a significantly higher variability when $V_{GATE,SET}$ is at the middle range. Furthermore, the SET current range at 1.2 V V_{SET} is also significantly smaller than its counterpart at V_{SET} of 2.0 V. In terms of voltage distribution, the curves and shaded areas in Fig. 6(a) are not smooth, which is attributed to computational errors caused by the flatter saturation region of the transistors with a *W/L* ratio of 1. Similarly, $V_{MEM,SET}$ in both the cases is finally stabilized at about 0.7 V. V_{SET} values mainly affect the voltage drop over the transistor.

A comparison of the two sets of SET currents and transistor input characteristics is shown in Fig. 6(c). The curves of the SET currents overlap the input characteristics of the transistors. Moreover, all these curves show linearity when $V_{GATE,SET}$ is larger than 2.0 V due to the wider range of gate voltages applied to the transistor with a *W/L* ratio of 1. However, there is a tradeoff in the range of applied gate voltages. According to the transistor load line curves shown in Fig. 6(d), when V_{SET} is 2.0 V (solid red line), the operating region of the transistor is initially in the saturation region, but gradually transitions to the linear region as the gate voltage rises. This causes the current regulation capability of the transistor to slowly decrease and the variation in the SET current to increase. As a comparison, when the applied V_{SET} is 1.2 V (red dashed line), the transistor operates purely in the linear region. This explains the higher SET current variability and the much smaller SET current range than its counterpart.

The statistics of the 200-cycle SET algorithm test for 1T1R structures with T-3 are shown in Fig. 7(a) and (b). $V_{GATE,SET}$ in this experiment ranges from 0.8 to 4.8 V. According to

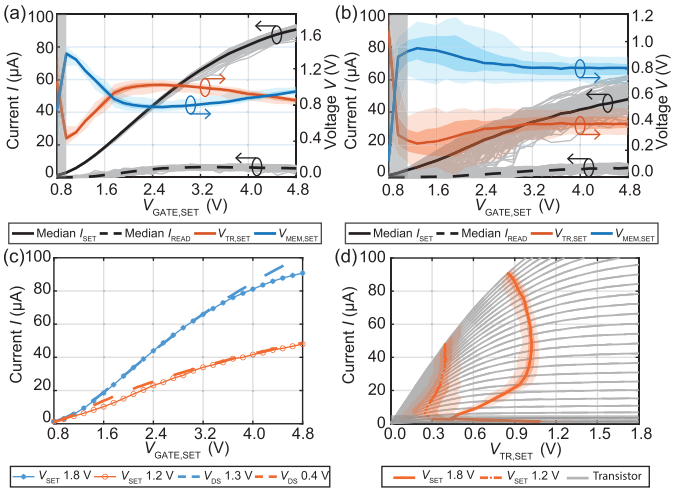

Fig. 7. Statistics for 1T1R structures with T-3. Evolution of the extracted $V_{MEM,SET}$ and $V_{TR,SET}$ corresponding to the SET and READ currents (gray lines) at V_{SET} (a) 1.8 and (b) 1.2 V. (c) Comparison between SET currents and transistor input characteristics. (d) Correlation among SET currents (red lines), $V_{TR,SET}$, and transistor transfer characteristics (gray lines).

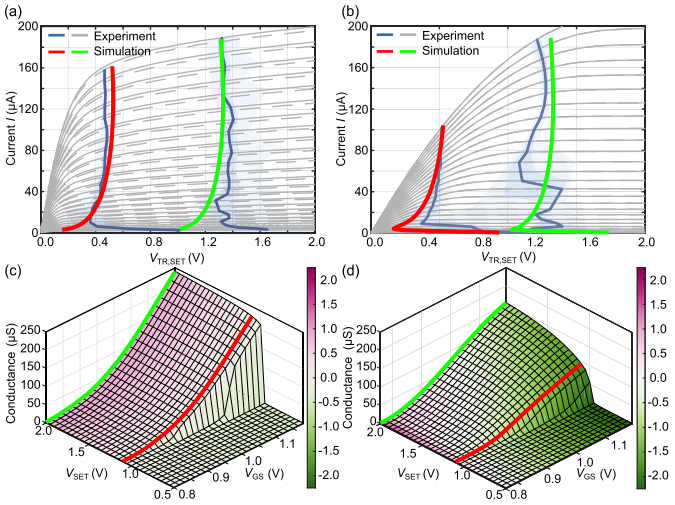

Fig. 8. (a) and (c) Simulation results for the 1T1R structure with T-1. (b) and (d) Simulation results for the 1T1R structure with T-2. The fit of the simulation results to the experimental load line curves is shown in (a) and (b) as solid red and green lines. The experimental transistor characteristics are shown in gray and blue and are taken from Figs. 5(d) and 6(d). In (c) and (d), the update behavior and transistor working regions are shown for the same SET algorithm as shown in Fig. 4 but at different V_{SET}.

Fig. 7(a), the cycle-to-cycle variation in the SET current gradually increases with increasing $V_{GATE,SET}$, while this variation becomes more obvious in (b). It should be noted that even when V_{SET} is 1.8 V, the maximum SET current is still less than 100 μA, while this value is less than 60 μA when V_{SET} is 1.2 V. This indicates that due to the transistor characteristics, the current value of the VCM cell is limited to a small current range throughout the SET pulse train. Therefore, the SET behavior and the resulting conductance of the VCM cell might be different from the other two types of 1T1R structures. First, the cell voltage is higher, above 0.8 V. It is speculated that the 1T1R structures with T-3 require a higher voltage to drive the SET process due to the limited transferred current. In addition, as shown by the black dashed line in (a), the maximum read current is at the middle of the pulse train after $V_{GATE,SET}$ of around 3.2 V, and gradually decreases thereafter. This indicates that unlike the other two transistor sizes, further increasing the gate voltage of the transistor does not help reduce the resistance of the VCM cell when a large V_{SET} is applied. Another difference can be observed by comparing the SET current and the transistor input characteristics as shown in Fig. 7(c). For the data with V_{SET} of 1.8 V, there is a visible difference between two blue current curves when the $V_{GATE,SET}$ is higher than 3.5 V. From the load line plot in Fig. 7(d), for the curve at V_{SET} of 1.8 V (solid red line), the operating region of the transistor gradually shifts from the saturation region to the linear region as the gate voltage is increased, resulting in a decrease in current gain. This explains why the slope of the SET current in Fig. 7(a) gradually becomes flatter as the gate voltage rises above 3.5 V, as well as the deviation between the blue current curves in Fig. 7(c). For the data with V_{SET} of 1.2 V (red dashed line), the operating region of the transistor is mainly in the linear region, which is less capable of controlling the current compared with the saturation region. Therefore, the current shows a larger variation during the SET process. The simulation study of the bias conditions in the next section does not cover this type of 1T1R structure due to the smaller conductance range and larger current variation which might not be favorable for practical applications.

V. Simulation Results

To gain a better understanding of the impact of different transistors, we performed simulations to test the 1T1R structures under different working conditions. First, we verified that the compact model we used, the JART VCM v1b model, can also describe the behavior of VCM cells in 1T1R structures. For that purpose, we simulated the same SET algorithm as was measured experimentally and plotted the simulation results of the current at the end of each switching pulse on top of the experimental results in Fig. 8(a) and (b) as red solid lines for $V_{SET} = 1.2$ V and as green solid lines for $V_{SET} = 2.0$ V, respectively. For the simulations of the 1T1R structure with T-1 [Fig. 8(a) and (c)], the 1T1R structure was initialized with a resistance of around 700 kΩ consistent with the experimental range of 500–900 kΩ. To match the current level of the experimental transistor at the end of the SET algorithm pulse train, the maximum gate voltage was reduced from 1.3 V in the experiment to 1.20 V for $V_{SET} = 2.0$ V and to 1.18 V for $V_{SET} = 1.2$ V. This deviation can be explained by the variability observed in the experiments, while the simulations operate with deterministic models for the transistor and the VCM cell. For T-2 transistor, the 1T1R structure was initialized at 250 kΩ, again consistent with the experimental range of 230–270 kΩ. We also had to reduce the final gate voltage levels to match the current at the end of the SET algorithm from 3.3 V in the experiment to 3.00 V at $V_{SET} = 2.0$ V and to 2.95 V for $V_{SET} = 1.2$ V. With these small modifications, we can see a good agreement between the experiment and simulation for the voltage division between the transistor and VCM cell.

After we have verified that the SET algorithm experiment can be modeled sufficiently well, we performed a parameter study of V_{SET} voltage to investigate its effect on the

updating behavior. For this, V_{SET} was varied between 0.5 and 2.0 V while all other parameters were kept constant. The maximum gate voltage was chosen as 1.18 and 2.95 V in Fig. 8(c) and (d), respectively, corresponding to the minimum gate voltages from the above load line fitting. For identification, we have given V_{SET} values that were used to fit the VCM model as red and green solid lines. The conductance is calculated based on the current flow during the read operations between subsequent SET pulses which was performed at the same voltage levels as in the experiment. In Fig. 8(c) and (d), the color indicates the voltage difference from the current operating point to the transition point between the saturation and linear regions of the transistor. A positive voltage indicates that the transistor is operating in the saturation region while a negative voltage indicates that the transistor operates in the linear region. A voltage of zero indicates that the transistor is operating right at the transition between the linear region and saturation region. Higher absolute values indicate that the operating point is further away from the transition region, i.e., the transistor is operating deep in the linear or saturation region. For a better comparison between the results of the two transistors, we have adapted the same color scale for both the transistors. Initially, for both the cases the conductance does not change for $V_{SET} \leq 1$ V indicating that the VCM cells stay in the HRS and do not switch. At higher V_{SET} voltages, the simulations in Fig. 8(c) and (d) show a clear difference between the two transistors. The 1T1R structure with T-1 shows a conductance change behavior that is almost independent of V_{SET} while the conductance evolution of the 1T1R structure with T-2 shows a strong dependence on V_{SET} voltage. For the second transistor, shown in Fig. 8(d), a higher V_{SET} results in stronger switching, resulting in a higher conductance at the same $V_{Gate,SET}$. The difference in the conductance evolution behaviors can be explained by the operation modes of the transistor, i.e., whether they are operating more as a resistor in the linear region or more as a current compliance in the saturation region. From the color scale, it can be seen that T-1 operates exclusively in the saturation region if any switching is observed, while T-2 changes from the saturation region to the linear region as $V_{Gate,SET}$ is increased. If the transistor operates as a current compliance, it can adapt its resistance to keep the current flow constant. Through this adaptation, the voltage divider between the VCM cell and the transistor is kept such that the current through the 1T1R structure does not change. This results in the conductance evolution not depending on V_{SET}. If the transistor operates in the linear region, it behaves more like an ohmic resistor which allows for higher current flows as V_{SET} is increased. This results in different conductance levels based on V_{SET}. The further the transistor operating point is inside the linear region (indicated by a lower negative voltage on the color bar), the more the transistor operates as an ohmic resistor. On the opposite side, the higher the voltage on the colorbar, the more the transistor behaves like a current compliance.

VI. Discussion

In the SET algorithm, three types of 1T1R structures share one common feature—a relatively constant cell voltage. The higher cell voltage shown in the 1T1R structures with T-3 may result from small current limitations. However, the values (0.7–0.8 V) of the other two types of 1T1R structures remained consistently higher than the ones calculated based on the structure of VCM cell with a series resistor (around 0.4 V) [14], [26]. This difference can be explained by the SET kinetics of the VCM cell [4]. Compared with the sweep rate used in the voltage sweep (0.67 V/s), the frequency of voltage in the pulse test used here is higher by more than six orders of magnitude. Consequently, a larger cell voltage is required to switch the VCM cell. Similar outcomes were reported by Degraeve et al. [27] as well. Hence, the applied V_{SET} of the 1T1R structure must be configured while taking into account the pulse frequency to guarantee that the chosen voltage is sufficient for the cell voltage. In this work, the minimum V_{SET} required for switching was investigated by simulation. As shown in Fig. 8(c) and (d), the VCM cells do not switch, regardless of $V_{GATE,SET}$ value, when V_{SET} is below a certain threshold (1.0 V in both the cases).

Furthermore, a relationship between the bias conditions ($V_{TR,SET}$ and V_{SET}) necessary for maintaining a transistor operating in the saturation region can be deduced. According to the transfer characteristics of the transistor, the applied voltage must meet the subsequent conditions, $V_{TR,SET} > V_{GATE,SET} - V_{th}$. V_{th} is the transistor threshold voltage. For 1T1R structures, the voltage shared by the transistor is equal to V_{SET} minus the cell voltage, $V_{TR,SET} = V_{SET} - V_{MEM,SET}$. In this article, we found that $V_{MEM,SET}$ remained within a specific range. Therefore, for the transistor to operate in the saturation region, $V_{GATE,SET}$ and V_{SET} must satisfy the following relationship: $V_{SET} > V_{GATE,SET} - V_{th} + V_{MEM,SET}$. It follows that there is a lower limit to V_{SET} for a given $V_{GATE,SET}$. For the transistor T-1 in the experiment, assuming V_{th} of 0.8 V, the minimum V_{SET} is 1.2 V when the maximum $V_{GATE,SET}$ is 1.3 V. Both the measured data and simulation results in Fig. 8(a) and the parameter study of V_{SET} in Fig. 8(c) well demonstrate this concept. There certainly exists an upper limit to V_{SET}, determined by the power supply capability of peripheral circuits and the maximum voltage of the transistor.

On the other hand, the transistors with different sizes allow the 1T1R structures to be operated within a considerably distinct current range. A larger upper current limit permits a higher conductance of the VCM cell at the same voltage amplitude, thereby resulting in a greater read window for the 1T1R structures. According to Fig. 8(c) and (d), the transistor T-1 has a larger conductance upper limit than its counterpart. For the other two transistors, increasing the gate voltage is the typical method for a larger current. However, as previously discussed, to achieve saturation region operation of the transistor for a given V_{SET}, there is an upper limit to $V_{GATE,SET}$. Increasing $V_{GATE,SET}$ in exchange for high current can lead to the transistor progressively operating in the linear region during the SET process and not acting as current compliance, which might weaken current control, decrease current gain, and even diminish the SET effect. In addition, the transistor T-1 has certain drawbacks. First, due to channel length modulation, the transferred current of transistor T-1 in the saturation region

keeps increasing while transistor T-2 shows flat characteristics which is advantageous for current control. Second, transistor T-1 is more sensitive to $V_{\mathrm{GATE,SET}}$ leading to a larger cycle-to-cycle variability. Finally, transistor T-2 offers the option of a wide range of $V_{\mathrm{GATE,SET}}$, allowing for enhanced linearity of the SET process. For these reasons, tailoring transistors with appropriate *W/L* ratios to meet the different requirements of the actual application must be considered in the device design.

VII. Conclusion

In this article, we investigated the effect of the transistor transfer characteristics on the programming behavior of 1T1R structures by calculating the intrinsic cell voltage in 1T1R structures for different transistor sizes. The results indicate that the intrinsic cell voltage remains constant during the programming algorithm with fixed applied SET voltage. The amplitude of the applied SET voltage determines the voltage drop over the transistor. Therefore, the electrical behavior of the transistor is determined by both the applied SET voltage and the gate voltage. Transistors with a broad range of transfer currents can operate within the saturation region during SET. For transistors with a smaller current range, increasing the gate voltage causes the switching path to move from the saturation region to the linear region. This weakens the variability control and hence the SET effect. Finally, we examined the correlation between the transistor's saturation state, bias conditions, and size, along with the findings from the simulations based on the JART VCM v1b compact model. To optimize the design of 1T1R structures, we provided design rules for proper selection of the transistor *W/L* ratio and the operation parameters so that the SET event of the VCM cell overlaps with the transistor's saturation region.

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