

Sensing dot with high output swing for scalable baseband readout of spin qubits

Eugen Kammerloher,^{1,*} Andreas Schmidbauer,² Laura Diebel,² Inga Seidler¹, Malte Neul,¹ Matthias Künne,¹ Arne Ludwig,³ Julian Ritzmann,³ Andreas Wieck,³ Dominique Bougeard,² Lars R. Schreiber^{1,4,†} and Hendrik Bluhm^{1,4}

¹*RWTH Aachen University, Jülich Aachen Research Alliance (JARA) Institute for Quantum Information, Aachen 52074, Germany*

²*Fakultät für Physik, Universität Regensburg, Regensburg 93040, Germany*

³*Applied Solid State Physics, Ruhr-Universität Bochum, Bochum 44801, Germany*

⁴*ARQUE Systems GmbH, Aachen 52074, Germany*



(Received 13 May 2024; accepted 18 July 2024; published 15 August 2024)

A crucial requirement for quantum computing—in particular, for scalable quantum computing and error correction—is fast and high-fidelity qubit readout. For semiconductor-based qubits, one limiting factor for local low-power signal amplification is the output swing of the charge sensor. We demonstrate GaAs and Si asymmetric sensing dots (ASDs) specifically designed to provide a significantly larger response compared to conventional charge-sensing dots. Our ASD design features a drain reservoir strongly decoupled from the sensor dot, which mitigates negative feedback effects found in conventional sensors. This results in a boosted output swing of 3 mV, which exceeds the response in the conventional regime of our device by more than a factor of 10. The enhanced output signal paves the way for employing very low-power readout amplifiers in close proximity to the qubit.

DOI: [10.1103/PhysRevApplied.22.024044](https://doi.org/10.1103/PhysRevApplied.22.024044)

I. INTRODUCTION

Spin qubits based on gate-defined quantum dots (QDs) use proximal charge sensors [1,2] and, more recently, dispersive gate-sensing techniques [3–5] for readout of the quantum state after spin-to-charge conversion [6,7]. The proximal charge sensors can be quantum point contacts or sensing dots (SDs), with the latter being the most sensitive sensor for spin-qubit readout. The focus of new readout circuits is shifting toward scalability, as high-fidelity, scalable readout is a key requirement for quantum computers with more than just a few qubits.

The state-of-the-art readout technique is based on rf reflectometry [8], which satisfies the requirement of high fidelity and provides the largest bandwidths to date. Depending on the qubit scaling strategy, rf reflectometry may be the method of choice, as there are solutions to miniaturize at least parts of the necessary rf components [9] or use multiplexing techniques [10–12] in, e.g., the context of a crossbar qubit architecture [13]. However, the overall readout periphery is complex and the necessary rf components are currently on the centimeter scale.

Baseband readout, using optimized transistor circuits in close proximity to the qubit, may prove decisive for scaling strategies where readout and some control functionality are integrated near each qubit—as, e.g., proposed for the spider-web array [14]. Single-shot readout using a high-electron-mobility-transistor (HEMT) amplifier has been demonstrated [15] and the performance has been improved for amplifiers adjacent to the sample [16–18]. Increasing the SD output signal would allow an even lower total power consumption, and thus more simultaneous qubit readouts or a higher readout fidelity using the baseband-readout approach, since the power requirement is determined by the amplifier gain and sensitivity. In conventional sensing dots, however, the output swing is limited by negative feedback, due to a large drain capacitance, analogous to the Miller effect in classical electronics [19].

In this study, we introduce a proximal charge sensor designed specifically to create an asymmetric sensing dot (ASD) by utilizing additional electrodes to sculpt the electrostatic potential of an SD. Our main goal is to investigate the performance of this gate concept for ASD realization. We perform voltage-bias transport measurements, observing a significant reduction in dot and drain capacitive coupling in Coulomb diamonds. We find qualitatively similar results in remote-doped GaAs/(Al,Ga)As and undoped Si/Si-Ge devices, supporting the universality of the concept. Additionally, we use the ASD for charge sensing

*Contact author: kammerloher@physik.rwth-aachen.de

†Contact author: lars.schreiber@physik.rwth-aachen.de

in a nearby double quantum dot (DQD) tuned into a multielectron regime.

By focusing on the realization and investigation of the ASD gate concept, we aim to establish a foundation for further research into the potential of this sensor design for scalable baseband-readout quantum circuits. The ASD allows for a trade-off between the expanded footprint of the sensor gate layout, owing to additional gate electrodes, and its boosted signal output. Recent investigations into the qubit shuttling architecture have eased the requirements on the former aspect [20–25]. On the other hand, for dense architectures similar to the crossbar network [13], this approach is likely not suitable.

II. ASD CONCEPT

In Fig. 1(a), we illustrate the electric potential of a biased SD. The ladder of QD energy levels can be shifted by the gate voltage V_G , while a bias V_D is applied to the drain D . Measuring the transport current through the device while driving these voltages produces a characteristic diamond-shaped pattern due to Coulomb-blockade effects. A section of these diamonds is depicted in Fig. 1(b), where current flows only in the gray regions. According to a constant-interaction model [26], the positive and negative slopes of the Coulomb diamonds are $C_G/(C_\Sigma - C_D)$ and $-C_G/C_D$, where C_Σ is the total capacitance to ground of the dot and C_G and C_D are the capacitance to the swept gate electrode and drain reservoir, respectively. In the SD, the drain D is separated from the dot by a sharp tunneling barrier, similar to the source S , as depicted by the top sketch in Fig. 1(b).

The ASD concept presented in this study is focused on modifying the drain barrier such that the tunneling rate remains comparable to that of the conventional SD, while significantly reducing the drain capacitance to increase the maximum output voltage. To achieve this, the barrier is subdivided into a compound barrier with a sharp tunnel barrier region I and an additional slowly decreasing barrier region II, termed the slide. Region II physically separates the drain reservoir further from the dot, resulting in $C_{D,ASD} \ll C_{D,SD}$, while region I controls the tunneling at the working point. The top sketch in Fig. 1(d) shows the new SD configuration, where the asymmetric arrangement of the source and drain is visible; hence the name ASD.

In Fig. 1(c), we display the electric potential of a biased ASD. An equivalent shift ΔV_Q on the V_G axis now results in a greatly enhanced shift $e\Delta V_{ASD}$ for the ASD compared to $e\Delta V_{SD}$. Therefore, an essential figure of merit for the ASD is the magnitude of the blue slope $-C_G/C_D$ in Fig. 1(d), where larger values indicate a higher output voltage swing of the sensor when configured for charge sensing.

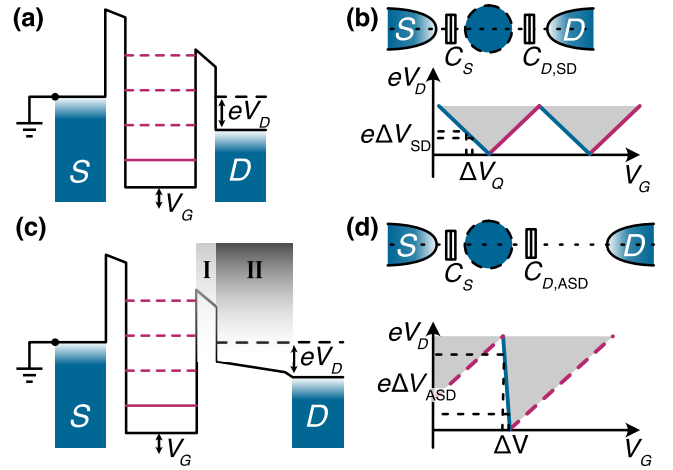


FIG. 1. Visualization of the SD and the ASD concepts. (a),(c) A schematic electric potential with an applied bias of V_D between the source S and the drain D for the SD and ASD, respectively. The ladder of the levels of the dots can be energetically shifted by the gate voltage V_G . In the SD [panel (a)], the drain D is separated from the dot by a sharp tunneling barrier. In the ASD [panel (c)], the barrier is a compound barrier with a sharp tunnel barrier region I controlling tunneling and an additional intermediate barrier region II, termed the slide. (b),(d) Schematic Coulomb diamonds for both sensors. No current flow occurs in the white regions due to Coulomb blockade. Single-electron transport current flows in the light-gray regions. The blue and red lines mark the edges of the diamond-shaped Coulomb-blockade regions. An equivalent shift ΔV_Q on the V_G axis results in an enhanced shift $e\Delta V_{ASD}$ for the ASD compared to $e\Delta V_{SD}$ in current-bias mode. The upper insets show schematically a top view of the potential. The source and drain electron reservoirs have a tunnel and capacitive coupling to the quantum dot (blue circle).

III. EXPERIMENTAL RESULTS

In Fig. 2(a), we display a false-colored scanning-electron-microscope (SEM) image of a double quantum dot (DQD) integrated with an ASD on the left. The ASD is incorporated into our GaAs qubit design, utilizing a doped MBE-grown GaAs/(Al,Ga)As heterostructure, which features a 2DEG 90 nm beneath the interface (for heterostructure details, see Appendix A) [27,28].

The yellow-colored gates DA1–DA3 define an SD, while the orange-colored gates DA4–DA6 control the dot-drain transition. The purple-colored gates are used to define and manipulate the nearby DQD. The source reservoir (labeled $\boxtimes$ II) has a common distance from the SD (red circle) used for conventional SDs, while the drain reservoir ($\boxtimes$ I) is asymmetrically formed. A dashed line illustrates a possible electron path connecting the source and drain of the sensor. Supported by numerical electrostatic simulations, we have developed device designs optimizing the drain-barrier potential region for a slow and monotonically declining transition to the drain reservoir, effectively creating a micron-scale electron slide with sharp tunnel barriers

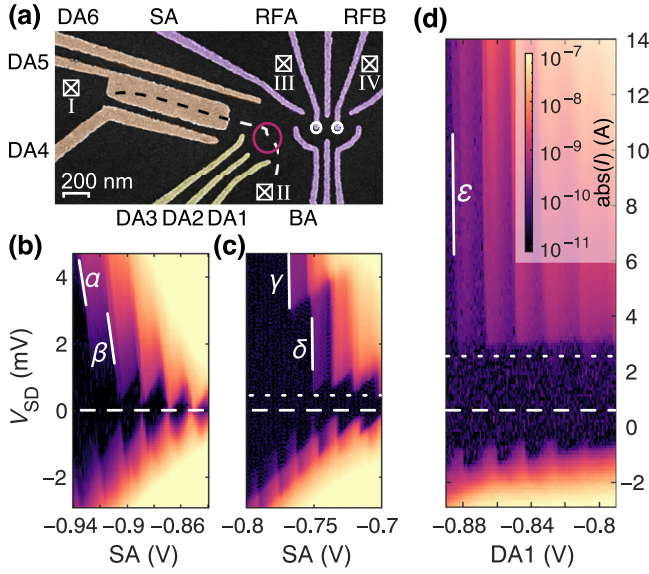


FIG. 2. The device layout and a Coulomb-diamond comparison in GaAs/(Al,Ga)As. (a) A false-colored SEM image of a GaAs ASD device. Labels $\boxtimes$ I and $\boxtimes$ II mark the drain and source reservoirs, connected by a dashed line, representing a possible electron trajectory through the sensor. A red circle indicates the sensor dot position. The white circles denote the position of a DQD, which may host qubits. (b) Conventional SD with nearly symmetric source and drain reservoirs is tuned, with gates DA4–DA6 turned off (0 V). The white dashed horizontal line signifies zero bias. The white lines indicate negative slopes $\alpha = -0.25$ V/V and $\beta = -0.30$ V/V of a linear fit to the 100-pA contour. (c) The ASD is tuned up with an asymmetric source-drain configuration using gates DA4–DA6. The white dashed horizontal line denotes zero bias and the dotted line shows a bias window $0 \leq V_{SD} \lesssim 360$ μ V with no current flow due to the high drain-barrier opacity. The white lines represent negative slopes $\gamma = -3.96$ V/V and $\delta = -2.29$ V/V of a linear fit to the 100-pA contour. (d) ASD Coulomb diamonds with a nearby tuned-up DQD for charge sensing. The white dashed horizontal line marks zero bias and the dotted line indicates a bias window $0 \leq V_{SD} \lesssim 2.9$ mV with no current flow.

defining the SD [29]. A detailed discussion on the modeling and simulation methods is published in Ref. [30]. Transport at the optimal working point is still possible, while the capacitive coupling of the dot and drain is significantly reduced.

To experimentally validate the ASD concept, we compare Coulomb diamonds of the sensor tuned for conventional operation with nearly symmetric source and drain barriers (gates DA4–DA6 set to 0 V) in Fig. 2(b) with a tuned-up ASD in Fig. 2(c) (for details of the measurement setup, see Appendix B). The sensor is operated in the multielectron Coulomb-blockade regime with a voltage bias V_D applied to ohmic contact $\boxtimes$ II (drain), while the current is measured with a transimpedance amplifier at $\boxtimes$ I (source).

Typical values of V_D do not exceed a few hundred microvolts for conventional SD operation. In the following, values of V_D can easily exceed several millivolts, since the compound drain barrier of the ASD only becomes transparent at higher bias voltages. In Fig. 2(b), we show typical Coulomb diamonds, when operating the device in a conventional way without using the additional gate electrodes, which are symmetric around zero bias. Gate SA not only shifts the dot minimum but also modifies the tunneling rates of the dot barriers; thus the diamond features become smeared out for higher tunneling rates at more positive voltages. At more negative voltages, transport is blocked close to zero bias, as the barriers become opaque. The slope of the diamond can be evaluated at different current levels. Here, we choose 100 pA, which is a compromise between low-current operation and a sufficient signal-to-noise ratio. In Fig. 2(b), we fit a line at the 100-pA contour and find a maximum slope of $\beta = -0.30$ V/V for the SD. Note that for a conventional SD, the slope remains nearly constant even at higher bias values.

In Fig. 2(c), we show equivalent measurements with the sensor tuned to the ASD regime. The Coulomb diamonds change distinctively from the conventional case and the positive and negative bias configurations are no longer symmetric. A bias dependence of the Coulomb lines is observed for slopes γ and δ of the ASD, compared to α and β for the SD. At higher bias, a maximal slope of $\gamma = -3.96$ V/V at the 100-pA contour is observed [31]. The steepening of the Coulomb diamonds indicates the desired reduction of C_D by a factor of $C_{D,SD}/C_{D,ASD} \approx 13$, compared to the maximal slope in Fig. 2(b). Additionally, we observe a bias window in Fig. 2(c), where transport is blocked ($0 \leq V_{SD} \leq V_T$, where $V_T \lesssim 360$ μ V), in between the dashed and dotted white lines. We find in Fig. 2(d) that when a nearby DQD is also tuned up, V_T can be of the order of several millivolts, which results in low visibility of the typical Coulomb-blockade features near zero bias. Gate DA1 is used instead of SA to avoid mistuning the DQD, which is less sensitive to this gate electrode. Further details of the ASD tuning and characteristic features are discussed in Appendix C.

To test the adaptability of our ASD concept, we have also realized a device in a MBE-grown Si/Si-Ge heterostructure, featuring a 10-nm-thick Si quantum well (QW) separated from the interface by a Si_{0.65}Ge_{0.35} spacer [32] (for the heterostructure details, see Appendix A). Transferring the ASD from a remote-doped GaAs/(Al,Ga)As to an undoped Si/Si-Ge heterostructure requires a full redesign of the gate pattern: first, Si/Si-Ge requires an accumulation gate also above the slide region; and, second, the gate pattern has to be shrunk down to compensate for the 3-times-larger effective electron mass. Therefore, we adapted the gate layout via a simulation-guided design to host the ASD and a nearby DQD [30]. A false-colored SEM image of this gate layout is shown

in Fig. 3(a). The sensor dot is formed by the light-yellow-colored gates, from which gate PS serves as the plunger gate for the sensor quantum dot levels. Gates SL, SR, and ST (colored orange) form the potential slide [region II in Fig. 1(c)] and the purple-colored gates may be used to tune two tunnel-coupled QDs in the vicinity of the sensor dot. Current through the sensor is defined by ohmic contacts $\boxtimes$ I and $\boxtimes$ II, while contacts $\boxtimes$ III and $\boxtimes$ IV serve as electron reservoirs for the DQD. Tuning the electrostatic potential to form a sensor QD below gate PS, we record a series of Coulomb-blockade measurements to test the tunability of the slide-potential region II. Starting from a conventional symmetric configuration in Fig. 3(b), the slide is then activated by only reducing the voltage on gate SR, while simultaneously increasing the voltage on

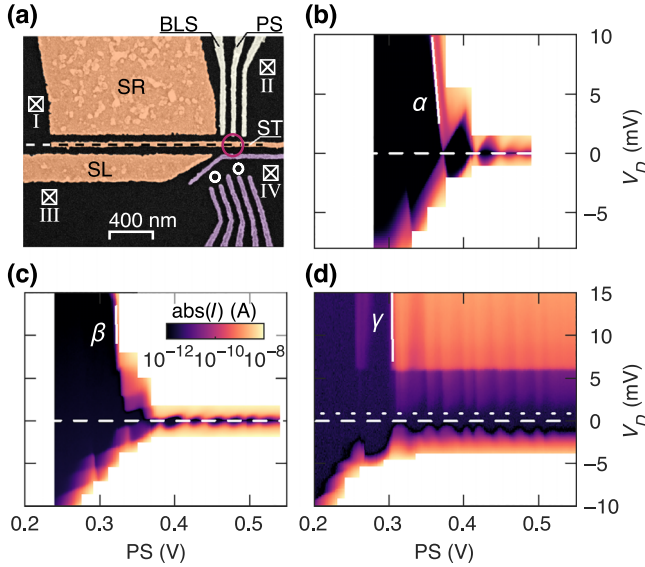


FIG. 3. The device layout and a Coulomb-diamond comparison in Si/Si-Ge. (a) A false-colored SEM image of an ASD device in Si/Si-Ge similar to the one measured. A global top gate isolated by Al_2O_3 is not shown. The light-yellow-colored gates (including BLS and PS) define the sensor QD in the vicinity of the purple-colored gates, which can be used to form a DQD. The potential slide for the ASD operation of the SD is formed by the orange-colored gates (SR, SL, and ST). The drain and source reservoirs are labeled $\boxtimes$ I and $\boxtimes$ II for the sensor current path and $\boxtimes$ III and $\boxtimes$ IV for the DQD current path. (b)–(d) A Coulomb-diamond measurement series tuning the SD from a symmetric to an asymmetric configuration. To do so, the gate potential of SR is decreased step-wise from 0.34 V in (b) to 0.24 V in (c) to 0.215 V in (d) and simultaneously the gate potential of BLS is adjusted to maintain the same tunnel rate for transport through the SD. The measurements are performed by varying the drain potential V_D at the reservoir $\boxtimes$ I while keeping the reservoir $\boxtimes$ II at 0 V for different potentials at PS, which serves as the plunger gate for the sensor quantum dot levels. The white lines indicate the negative slopes of the corresponding Coulomb diamonds. Linearly fitting the 50-pA contour leads to slopes of $\alpha = -0.68$ V/V for (a), $\beta = -3.2$ V/V for (b), and $\gamma = -8.0$ V/V for (d).

gate BLS to retain the same tunnel rate [keeping region I in Fig. 1(b) constant] for transport through the sensor. In Figs. 3(b)–3(d), we have decreased the voltage on gate SR from 0.34 V to 0.24 V and 0.215 V, respectively. Similar to the observation in GaAs, for the most negative SR configuration, a blockade region with a threshold voltage of $V_T = 1$ mV emerges [33].

The series in Figs. 3(b)–3(d) clearly shows that the negative Coulomb-diamond edges become steeper as the voltage applied to gate SR decreases (for simulations of this behavior, see our related publication [30]). For all three diamonds shown here, we have determined these negative Coulomb-diamond slopes by fitting the 50-pA contour, which represents the best compromise between a low-current operation of the device and a sufficient signal-to-noise ratio. The slopes in Figs. 3(b)–3(d) represent the steepest slopes that we have found for each configuration [34]. Starting from $\alpha = -0.68$ V/V for the most symmetric configuration, we reach $\beta = -3.2$ V/V for the intermediate configuration and finally $\gamma = -8.0$ V/V for the most asymmetric configuration, corresponding to a 12-fold reduction of $C_{D,ASD}$.

Hence, we have shown that the ASD concept is equally efficient across material platforms. Integrating ASDs into a DQD environment, we have demonstrated a controllable reduction of $C_{D,ASD}$ both in Si and in GaAs while being able to maintain a tunneling rate that is useful for operation of the sensor quantum dot. In the proof-of-principle experiments discussed in Figs. 2 and 3, we have reached a maximal reduction of $C_{D,ASD}$ by a factor of 13 in GaAs and a factor of 12 in Si, implying an increase by the same factor of the voltage swings produced by these ASDs, compared to conventional SD operation.

IV. ASD CHARGE SENSING

We demonstrate charge-sensing operation with the ASD by defining a DQD in the center of the GaAs device, using the purple-colored gates shown in Fig. 2. For charge sensing, it is crucial to reconfigure the ASD for current bias to take advantage of the high output-voltage swing. In our case, a constant current source supplies 500 pA through the drain, while the source is grounded. We tune the ASD to a sensitive position and record a charge-stability diagram of the DQD using gates RFA and RFB, as shown in Fig. 4(a) (for the tuning details, see Appendix D).

The voltage drop V_D across the ASD is monitored with a voltmeter, as shown in Fig. 4(b). In Fig. 4(c), we display the voltage swing across the interdot transition of the DQD [dashed line in Fig. 4(a)], corresponding to a qubit state change when the DQD is used as an ST qubit. We observe a voltage swing of 3 mV. The voltage swing is expected to be an order of magnitude larger than that of a conventional SD in this configuration due to the one-order-of-magnitude difference in slopes β and γ seen in Fig. 2.

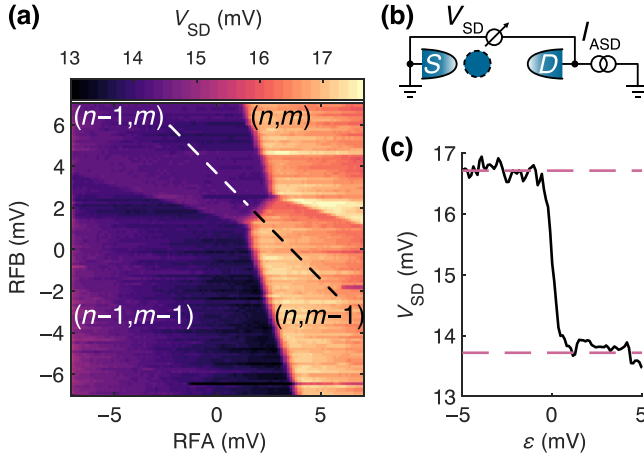


FIG. 4. Charge sensing with current-biased ASD. (a) The ASD is configured for charge sensing of a nearby multielectron DQD with a $I_{ASD} = 500$ pA current bias. The charge-stability diagram is recorded with the ASD, using the voltage drop V_D across the sensor as the signal (median adjustment per scan-line). (b) A schematic of the ASD wiring. (c) A cut on the detuning axis ϵ , which corresponds to the dashed line on the left panel (linear background subtracted). A voltage swing of 3 mV is observed.

These slopes provide a measure of sensor sensitivity, as discussed in Figs. 1(c) and 1(d).

In the ASD, the electrons entering the drain have a high energy, due to the higher voltage swing, which leads to phonons with larger energy that can enhance back action via inelastic tunneling events between the adjacent ASD and host qubit [35]. The exact impact merits further investigation, since the drain reservoir is located more distantly from the host qubit than in conventional sensing dots. It should further be noted that the sensor can be tuned into an opaque regime and only be active during a readout operation, thus reducing the effect of back action. The ASD charge-sensing technique offers an enhanced signal output but requires more chip space and a complex gate design, unlike the latched readout, which provides high readout fidelity without specific gate-design constraints but is limited to certain qubit systems [36,37]. Combining the ASD with latched readout could enhance sensor back-action mitigation due to the extended lifetime of a latched state. This integration promises improvements in qubit-state measurement, balancing the strengths of both techniques.

V. CONCLUSIONS AND OUTLOOK

In conclusion, we have presented a proximal charge sensor specifically designed for the formation of ASDs as the main goal of this study. Our findings showcase the successful implementation of an ASD gate concept that is adaptable across various material systems. This is evidenced by the drain-capacitance reduction by factors of 12

and 13, respectively, in both undoped Si/Si-Ge and doped GaAs devices when compared to conventional SD operation. It is worth noting that the GaAs device serves as a demonstrator and we anticipate that the ASD is more likely to be relevant for Si-based spin-qubit architectures, where nuclear fluctuations play a less significant role and CMOS processing techniques can be employed. The next experimental step involves integrating the ASD with published work on transistors [15–17] and examining the extent to which the ASD affects the host qubit, considering the higher-energy electrons generated during sensor operation compared to conventional SDs [35,38].

ACKNOWLEDGMENTS

This work was funded by the Army Research Office (ARO) under Contract No. W911NF-17-1-0349, entitled “A scalable and high performance approach to readout of silicon qubits,” and by the German Research Foundation (DFG) within the project 289786932 (BO 3140/4-1 and SCHR 1404/2-1). The device fabrication has been done at the HNF—Helmholtz Nano Facility of the Research Center Jülich GmbH [39].

APPENDIX A: GaAs/(Al,Ga)As AND Si/Si-Ge HETEROSTRUCTURE

The GaAs/(Al,Ga)As device has been fabricated on an MBE-grown heterostructure (sample B14722). The layer stack has been grown at a constant temperature of 695°C. A 35-nm $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$ layer has been grown on the GaAs substrate, followed by an additional 50-nm Si-modulation-doped $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$ layer. A 5-nm Si-doped GaAs cap has been used to finalize the structure; thus the 2DEG has been formed 90 nm below the interface. The ohmic contacts to the 2DEG have been thermally activated by a rapid anneal at 460°C of a gold-germanium alloy. The mobility of the 2DEG, as obtained by Hall measurements at a temperature of 4.2 K, is of the order of $1.47 \times 10^6 \text{ cm}^2/(\text{Vs})$ at an electron density of $1.82 \times 10^{11} \text{ cm}^{-2}$. A single layer of metal gates has been fabricated by means of electron-beam lithography.

The Si/Si-Ge device has been fabricated on a solid-source MBE-grown heterostructure. A relaxed virtual substrate consisted of a graded buffer grown at 500°C up to a composition of $\text{Si}_{0.65}\text{Ge}_{0.35}$ on a Si substrate without intentional miscut and a layer of constant composition $\text{Si}_{0.65}\text{Ge}_{0.35}$. It has provided the basis for a 10-nm natural-Si QW, grown at a substrate temperature of 350°C. The QW has been separated from the interface by 35 nm of $\text{Si}_{0.65}\text{Ge}_{0.35}$. The structure has been protected by a 1.0-nm naturally oxidized Si cap. The implanted ohmic contacts to the QW have been thermally activated by a rapid anneal at 700°C. The mobility of the 2DEG formed in the QW, as obtained by Hall measurements at a temperature of

1.5 K, is of the order of $1.1 \times 10^6 \text{ cm}^2/(\text{Vs})$ at an electron density of $6.6 \times 10^{11} \text{ cm}^{-2}$ and is limited by remote impurity scattering. A 10-nm layer of Al_2O_3 grown by atomic layer deposition has been used to insulate the first metal gate layer and the underlying heterostructure. The metal gates have been fabricated by means of electron-beam lithography. A second gate layer, insulated from the first gates by 50 nm of Al_2O_3 , has been used to induce a two-dimensional electron gas in the QW via the field effect. A Co magnet has been deposited on top of the device. Biased cooling, using voltages of -0.5 V at the gates of the first metal layer and -4.8 V applied to global gate of the second metal layer, has been employed for the Si/Si-Ge devices from room temperature to 300 mK, to inhibit leakage between the gate layers.

APPENDIX B: MEASUREMENT SETUP

Here, we briefly present the measurement setups used in this work. We show the GaAs case only, with only minor variations for the Si-Ge setup. In Figs. 5(a) and 5(b), we depict the schematic for the voltage- and current-bias cases, respectively. In Fig. 5(a), a Basel Instruments SP983c TIA has been used to measure the current through the SD. All voltage signals, including the SD bias V_{SD} , have been generated using our home-made DecaDAC voltage source. In Fig. 5(b), a Keithley 2400 source measurement unit (SMU) has been used to supply a constant current and measure the resulting voltage swing V_{SD} .

APPENDIX C: CHARACTERISTIC FEATURES OF THE ASD COULOMB DIAMONDS

In Fig. 6, we discuss several features of the ASD Coulomb diamonds in more detail. We focus on $V_D > 0$,

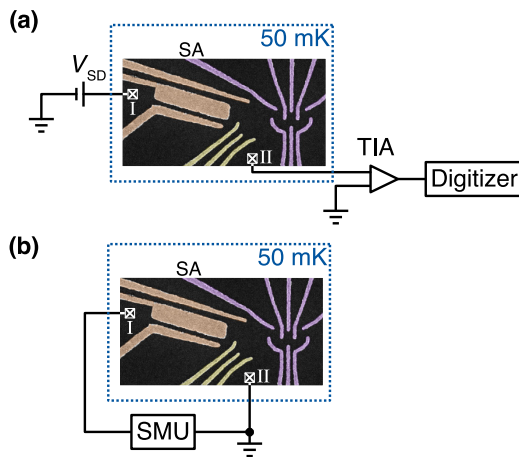


FIG. 5. The measurement setup. (a) A schematic diagram of the voltage-bias setup and the GaAs SEM image. (b) A schematic diagram of the current-bias setup. The source measurement unit (SMU) is configured for current bias and measures the voltage V_{SD} across the device.

since the ASD has a preferential bias direction and the behavior for $V_D < 0$ is unimportant for the intended mode of operation. The regions in the Coulomb-diamond plot where transport is possible are colored in gray. The blue slope is the desired working point for readout and the corresponding chemical potentials of the reservoirs and the last occupied energy level of the QD are depicted in the blue inset. The red energy level in the QD is close to the chemical potential of the source. Tunneling through the thin barrier in region I is possible at sufficiently high bias, after which the electron passes through region II and relaxes down into the drain reservoir. Along the opposing diamond edge, the energy level in the dot is close to the chemical potential of the drain, as illustrated in the red inset. However, tunneling through the barrier in region I in addition to the barrier in region II becomes exponentially difficult; hence the current flow degrades when approaching the dashed red slope from the left. The black inset depicts low-bias configurations, below the dashed black line. The inset shows a state in which the dot energy level is inside the bias window and can potentially contribute to the current flow; however, tunneling is nearly impossible, due to the combined barrier thickness of regions I and II. The compound drain barrier is only transparent above a threshold V_T , when a sufficiently large gradient is formed in region II by the bias voltage. Since the ASD compound drain barrier is exceedingly sensitive to gate-voltage changes on nearby structures, compensation for these changes can reduce the operational bias-voltage space to even higher values of V_T . Additionally, any disorder effects that create local minima in region II may result in an even higher value of V_T to compensate.

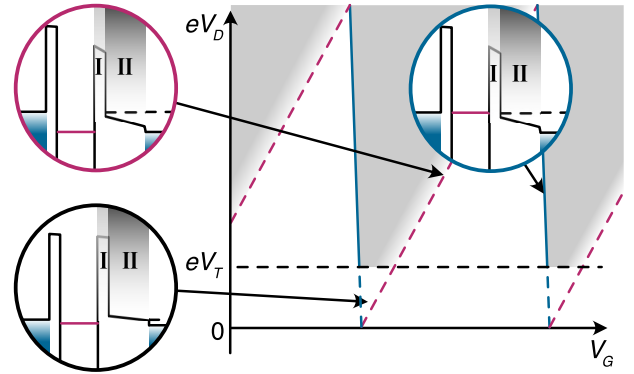


FIG. 6. The characteristic features of ASD Coulomb diamond. A schematic of the Coulomb diamonds expected for the ASD. A single-electron current flows in the light-gray regions separated by a blue solid line and a red dashed line from the Coulomb-blockade regions (white). The white current-free region is extended by the threshold voltage V_T (black dashed line). The three insets, in black, red, and blue frames, depict details of the ASD potential at the corresponding (V_G, V_D) operation points, marked by arrows.

APPENDIX D: ASD TUNING

The ASD can be tuned under voltage or current bias. Tuning under voltage bias involves slope evaluation of the Coulomb-diamond features, to find the desired regime. Tuning under current bias is closer to the intended mode of operation and lends itself to routine use and automation, since the output-voltage swing can be directly measured and easily optimized by a parameter sweep.

In the following, the tuning of the GaAs device is discussed under voltage bias initially. For an untuned device, gate electrodes SA and BA should be set below their pinch-off value and provide a fixed barrier, so that current can only flow from $\boxtimes$ I to $\boxtimes$ II. Gate DA6 is set to the same voltage as gate SA and can be used later, for fine tuning the sensor and to compensate for unrelated tuning operations performed on the nearby qubit. A useful starting point for ASD tuning is the diagram of the slide gate electrode (DA5) versus the slide barrier-gate electrodes (DA3 and DA4, while DA6 is kept fixed), shown in Fig. 7. Two parallel conducting channels are observed: conduction below DA5 (marked as region II) and undesired leakage below DA3 or DA4 far away from the ASD (region III). The dashed lines represent the conduction onset for these channels. The gate voltages marked with a white star provide starting values for DA3–DA5 when tuning the ASD. Here, the lever arms of DA3–DA5 are similar, indicating barrier formation close to the desired first sensor barrier between DA3 and DA6. Some line structure can be observed, indicating a disorder dot situated in the channel. The simulations suggest that a dot can arise between DA5 and DA3, at certain gate-voltage combinations, even without an additional disorder potential, due to the gate geometry. The second sensor barrier is defined in the following step.

Sweeping DA1 versus DA3 reveals Coulomb lines of the sensing dot [Figs. 8(a) and 8(b)]. At a low voltage bias of $V_D = 100 \mu\text{V}$ in Fig. 8(a), the sensor has a disorder dot in series, which further modulates the Coulomb blockade.

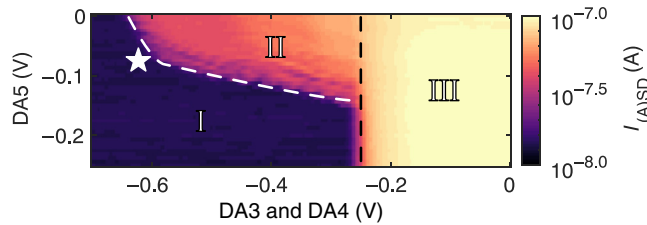


FIG. 7. A diagram of the slide gate versus the barriers. This measurement reveals several distinct features in a voltage-bias ($V_D = 100 \mu\text{V}$) measurement by sweeping gates DA3–DA5. Region III, at voltages where the barriers do not suppress the 2DEG below the gates, is undesired leakage. In region II, where a channel exists below DA5, some line structure can be observed, indicating a disorder dot situated in the channel. In region I, current flow is fully suppressed. A white star marks a useful voltage starting point for tuning.

blockade. Raising the bias voltage to 1 mV in Fig. 8(b) nearly suppresses the disorder dot. The strong influence of V_D indicates the position of the disorder dot to be in the channel below DA5 or between DA5 and DA3. To further tune the sensor in voltage-bias mode, we measure Coulomb diamonds. The negative diamond slope can be evaluated and optimized for a higher magnitude at different settings of DA1–DA6. However, finding suitable gate voltages is a very device-layout-specific process, due to the strong capacitive interdependence of the sensor gates and may require several parameter sweeps, while evaluating line features in Coulomb-diamond plots at each iteration. In the following, the sensor is tuned further in current-bias mode, which is the more expedient approach.

The sensor is now reconfigured for a current bias of $I_{\text{ASD}} = 500 \text{ pA}$ with a voltage compliance of $V_D \leq 50 \text{ mV}$ and, otherwise, the same parameters. In Fig. 8(c), the voltage drop across the sensor is depicted. The voltage drop is of the order of tens of millivolts for this sensor configuration and saturates at the compliance value below the dashed line, when transport is fully blocked. The derivative in the sweep direction in Fig. 8(d) reveals a structure

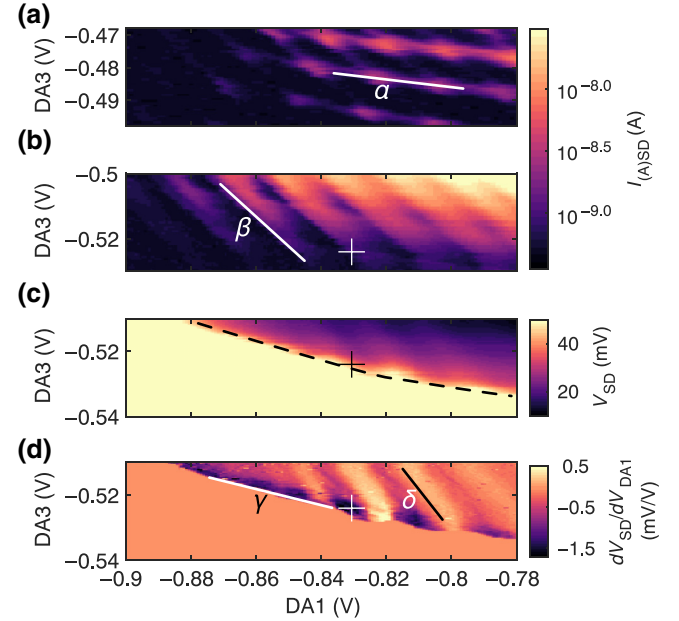


FIG. 8. Sensor wall-to-wall diagrams. (a) At a voltage bias of $V_D = 100 \mu\text{V}$, the sensor dot has a disorder dot in series, which further modulates the current Coulomb blockade. Slope α is -0.13 V/V . (b) At a voltage bias of $V_D = 1 \text{ mV}$, the disorder dot is nearly suppressed, revealing the Coulomb lines of the sensor. Slope β is -0.95 V/V . (c) The sensor is reconfigured for a current bias of $I_{\text{ASD}} = 500 \text{ pA}$ and $V_D \leq 50 \text{ mV}$ compliance, with a otherwise unchanged gate-voltage configuration. (d) The derivative in the sweep direction of (c) reveals the Coulomb line structure and areas with large voltage swings. The maximum voltage swing is marked with a cross. Slopes γ and δ are -0.26 V/V and -1.10 V/V .

similar to the Coulomb lines in Fig. 8(b), where slope β is similar to δ . Gate DA3 has a strong influence on the transport, since it controls the compound drain barrier. We observe regions of maximum voltage swing close to the full blockade (one such region marked with a white cross), which is the desired working point of the ASD for charge sensing. Voltage changes on nearby structures can shift the working point and can require compensation on the ASD gates, since the sensitive regions are small in extent.

-
- [1] M. Field, C. G. Smith, M. Pepper, D. A. Ritchie, J. E. Frost, G. A. Jones, and D. G. Hasko, Measurements of Coulomb blockade with a noninvasive voltage probe, *Phys. Rev. Lett.* **70**, 1311 (1993).
 - [2] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer, *Science* **280**, 1238 (1998).
 - [3] J. I. Colless, A. C. Mahoney, J. M. Hornibrook, A. C. Doherty, H. Lu, A. C. Gossard, and D. J. Reilly, Dispersive readout of a few-electron double quantum dot with fast rf gate sensors, *Phys. Rev. Lett.* **110**, 046805 (2013).
 - [4] A. West, B. Hensen, A. Jouan, T. Tanttu, C.-H. Yang, A. Rossi, M. F. Gonzalez-Zalba, F. Hudson, A. Morello, D. J. Reilly, and A. S. Dzurak, Gate-based single-shot readout of spins in silicon, *Nat. Nanotechnol.* **14**, 437 (2019).
 - [5] G. Zheng, N. Samkharadze, M. L. Noordam, N. Kalhor, D. Brousse, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, Rapid gate-based spin read-out in silicon using an on-chip resonator, *Nat. Nanotechnol.* **14**, 742 (2019).
 - [6] J. M. Elzerman, R. Hanson, J. S. Greidanus, L. H. Willems van Beveren, S. De Franceschi, L. M. K. Vandersypen, S. Tarucha, and L. P. Kouwenhoven, Few-electron quantum dot circuit with integrated charge read out, *Phys. Rev. B* **67**, 161308R (2003).
 - [7] A. C. Johnson, J. R. Petta, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot, *Phys. Rev. B* **72**, 165308 (2005).
 - [8] D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Fast single-charge sensing with a rf quantum point contact, *Appl. Phys. Lett.* **91**, 162101 (2007).
 - [9] A. C. Mahoney, J. I. Colless, S. J. Pauka, J. M. Hornibrook, J. D. Watson, G. C. Gardner, M. J. Manfra, A. C. Doherty, and D. J. Reilly, On-chip microwave quantum Hall circulator, *Phys. Rev. X* **7**, 011007 (2017).
 - [10] J. M. Hornibrook, J. I. Colless, A. C. Mahoney, X. G. Croot, S. Blanvillain, H. Lu, A. C. Gossard, and D. J. Reilly, Frequency multiplexing for readout of spin qubits, *Appl. Phys. Lett.* **104**, 103108 (2014).
 - [11] J. M. Hornibrook, J. I. Colless, I. D. Conway Lamb, S. J. Pauka, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly, Cryogenic control architecture for large-scale quantum computing, *Phys. Rev. Appl.* **3**, 024010 (2015).
 - [12] S. Schaal, S. Barraud, J. J. L. Morton, and M. F. Gonzalez-Zalba, Conditional dispersive readout of a CMOS single-electron memory cell, *Phys. Rev. Appl.* **9**, 054016 (2018).
 - [13] R. Li, L. Petit, D. P. Franke, J. P. Dehollain, J. Helsen, M. Steudtner, N. K. Thomas, Z. R. Yoscovits, K. J. Singh, S. Wehner, L. M. K. Vandersypen, J. S. Clarke, and M. Veldhorst, A crossbar network for silicon quantum dot qubits, *Sci. Adv.* **4**, 1 (2018).
 - [14] J. M. Boter, J. P. Dehollain, J. P. van Dijk, Y. Xu, T. Hensgens, R. Versluis, H. W. Naus, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. Vandersypen, Spiderweb array: A sparse spin-qubit array, *Phys. Rev. Appl.* **18**, 024053 (2022).
 - [15] I. T. Vink, T. Nooitgedagt, R. N. Schouten, L. M. K. Vandersypen, and W. Wegscheider, Cryogenic amplifier for fast real-time detection of single-electron tunneling, *Appl. Phys. Lett.* **91**, 23 (2007).
 - [16] L. A. Tracy, D. R. Luhman, S. M. Carr, N. C. Bishop, G. A. Ten Eyck, T. Pluym, J. R. Wendt, M. P. Lilly, and M. S. Carroll, Single shot spin readout using a cryogenic high-electron-mobility transistor amplifier at sub-Kelvin temperatures, *Appl. Phys. Lett.* **108**, 63101 (2016).
 - [17] M. J. Curry, M. Rudolph, T. D. England, A. M. Mounce, R. M. Jock, C. Bureau-Oxton, P. Harvey-Collard, P. A. Sharma, J. M. Anderson, D. M. Campbell, J. R. Wendt, D. R. Ward, S. M. Carr, M. P. Lilly, and M. S. Carroll, Single-shot readout performance of two heterojunction-bipolar-transistor amplification circuits at millikelvin temperatures, *Sci. Rep.* **9**, 1 (2019).
 - [18] A. R. Mills, C. R. Guinn, M. J. Gullans, A. J. Sigillito, M. M. Feldman, E. Nielsen, and J. R. Petta, Two-qubit silicon quantum processor with operation fidelity exceeding 99%, *Sci. Adv.* **8**, 1 (2022).
 - [19] P. Horowitz and W. Hill, *The Art of Electronics* (Cambridge University Press, New York, 2015), 3rd ed.
 - [20] V. Langrock, J. A. Krzywda, N. Focke, I. Seidler, L. R. Schreiber, and Ł. Cywiński, Blueprint of a scalable spin qubit shuttle device for coherent mid-range qubit transfer in disordered Si/SiGe/SiO₂, *PRX Quantum* **4**, 020305 (2023).
 - [21] I. Seidler, T. Struck, R. Xue, N. Focke, S. Trellenkamp, H. Bluhm, and L. R. Schreiber, Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture, *npj Quantum Inf.* **8**, 100 (2022).
 - [22] R. Xue, M. Beer, I. Seidler, S. Humpohl, J.-S. Tu, S. Trellenkamp, T. Struck, H. Bluhm, and L. R. Schreiber, Si/SiGe QuBus for single electron information-processing devices with memory and micron-scale connectivity function, *Nat. Commun.* **15**, 2296 (2024).
 - [23] T. Struck, M. Volmer, L. Visser, T. Offermann, R. Xue, J.-S. Tu, S. Trellenkamp, Ł. Cywiński, H. Bluhm, and L. R. Schreiber, Spin-EPR-pair separation by conveyor-mode single electron shuttling in Si/SiGe, *Nat. Commun.* **15**, 1325 (2024).
 - [24] M. Volmer, T. Struck, A. Sala, B. Chen, M. Oberländer, T. Offermann, R. Xue, L. Visser, J.-S. Tu, S. Trellenkamp, Łukasz Cywiński, H. Bluhm, and L. R. Schreiber, Mapping of valley-splitting by conveyor-mode spin-coherent electron shuttling, *npj Quantum Inf.* **10**, 61 (2024).
 - [25] M. Künne, A. Willmes, M. Oberländer, C. Gorjaew, J. D. Teske, H. Bhardwaj, M. Beer, E. Kammerloher, R. Otten, I. Seidler, R. Xue, L. R. Schreiber, and H. Bluhm, The

- SpinBus architecture: Scaling spin qubits with electron shuttling, *Nat. Commun.* **15**, 4977 (2024).
- [26] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, Spins in few-electron quantum dots, *Rev. Mod. Phys.* **79**, 1217 (2007).
- [27] S. J. MacLeod, A. M. See, A. R. Hamilton, I. Farrer, D. A. Ritchie, J. Ritzmann, A. Ludwig, and A. D. Wieck, Hybrid architecture for shallow accumulation mode AlGaAs/GaAs heterostructures with epitaxial gates, *Appl. Phys. Lett.* **106**, 012105 (2015).
- [28] P. Cerfontaine, T. Botzem, J. Ritzmann, S. S. Humpohl, A. Ludwig, D. Schuh, D. Bougeard, A. D. Wieck, and H. Bluhm, Closed-loop control of a GaAs-based singlet-triplet spin qubit with 99.5 gate fidelity and low leakage, *Nat. Commun.* **11**, 5 (2020).
- [29] E. Kammerloher, PhD dissertation, RWTH Aachen University, Aachen, 2022.
- [30] I. Seidler, M. Neul, E. Kammerloher, M. Künne, A. Schmidbauer, L. K. Diebel, A. Ludwig, J. Ritzmann, A. D. Wieck, D. Bougeard, H. Bluhm, and L. R. Schreiber, Tailoring potentials by simulation-aided design of gate layouts for spin-qubit applications, *Phys. Rev. Appl.* **20**, 044058 (2023).
- [31] On a side note: since $dV_{SD}/dV_{SA} > 1$, the ASD has voltage gain and can be used as an ultralow-power low-stray-capacitance voltage amplifier in principle, with the limitation of a narrow dynamics range.
- [32] A. Wild, J. Kierig, J. Sailer, J. W. Ager, E. E. Haller, G. Abstreiter, S. Ludwig, and D. Bougeard, Few electron double quantum dot in an isotopically purified ^{28}Si quantum well, *Appl. Phys. Lett.* **100**, 143110 (2012).
- [33] Even lower voltages on SR led to yet higher V_T .
- [34] Interpolation of the data sets along the plunger gate (PS) direction has been used to compensate for the lower measurement resolution on this gate.
- [35] G. Granger, D. Taubert, C. E. Young, L. Gaudreau, A. Kam, S. A. Studenikin, P. Zawadzki, D. Harbusch, D. Schuh, W. Wegscheider, Z. R. Wasilewski, A. A. Clerk, S. Ludwig, and A. S. Sachrajda, Quantum interference and phonon-mediated back-action in lateral quantum-dot circuits, *Nat. Phys.* **8**, 522 (2012).
- [36] S. A. Studenikin, J. Thorgrimson, G. C. Aers, A. Kam, P. Zawadzki, Z. R. Wasilewski, A. Bogan, and A. S. Sachrajda, Enhanced charge detection of spin qubit readout via an intermediate state, *Appl. Phys. Lett.* **101**, 233101 (2012).
- [37] P. Harvey-Collard, B. D’Anjou, M. Rudolph, N. T. Jacobson, J. Dominguez, G. A. Ten Eyck, J. R. Wendt, T. Pluym, M. P. Lilly, W. A. Coish, M. Pioro-Ladrière, and M. S. Carroll, High-fidelity single-shot readout for a spin qubit via an enhanced latching mechanism, *Phys. Rev. X* **8**, 021046 (2018).
- [38] D. Harbusch, D. Taubert, H. P. Tranitz, W. Wegscheider, and S. Ludwig, Phonon-mediated versus Coulombic back-action in quantum dot circuits, *Phys. Rev. Lett.* **104**, 196801 (2010).
- [39] W. Albrecht, J. Moers, and B. Hermanns, HNF—Helmholtz Nano Facility, *JLSRF* **3**, A112 (2017).