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ABSTRACT

Digital phase-locked loops (PLLs) are essential feedback circuits for synchronizing signals in digital communication systems. While amplitude and phase vary continuously in analog oscillators, the amplitude remains constant in digital oscillators with dynamical variations manifesting exclusively through changes in the timing of signal transitions. In this work, we introduce a novel analytically solvable event-based model for *phase-locking* in digital PLLs that leverages the discrete nature of digital signals. By employing a sampled control strategy, we demonstrate one-to-one and higher ratios of frequency locking under positive and negative feedback. By discretizing the continuous control signal, we drive a discrete iterative map, which we then use to derive analytical expressions for bifurcation curves, analogous to Arnold's tongue in analog oscillators. This mathematical framework provides an analytical approach for the analysis of synchronization and phase-locking in digital oscillators. Furthermore, the event-based control presented in this work for digital oscillators paves the way for energy-efficient circuit design and optimized control strategies for future digital communication systems.

This paper extends the fundamental concept of phase locking by developing an event-based model tailored specifically for digital oscillators. Unlike conventional continuous-time approaches, which periodically update the control value, the event-based methods update the control value only when an event occurs. This approach aligns seamlessly with the discrete nature of digital oscillators, yielding significant advantages such as reduced unnecessary control actions and lower power consumption. The event-based model proposed here focuses on the transition times of the digital signal to incorporate a sampled control approach, which can be used to discretize the continuous control signal. This enables the formulation of the system dynamics as a fully discrete dynamical system whose evolution can be captured through an iterative map. This approach leads to the identification of Arnold's tongue, unveiling the regions and types of frequency locking in digital oscillators. This solvable framework provides a comprehensive understanding of the behavior of digital PLLs, offering valuable insights for optimized circuit design and control strategies.

I. INTRODUCTION

Digital oscillators are fundamental components of modern electronics, playing a pivotal role in a wide range of applications, from telecommunications and data processing to electronic devices. Maintaining accurate phase relationships with a reference clock in these systems is crucial to ensuring reliable performance. The concept of phase locking is utilized across all of these applications and adapted to the specific functional requirements in each case. Although the implementations can vary, the core principle of phase-locking remains the same, ensuring consistent phase alignment.[1–4] Phase-locked loops (PLLs), feedback circuits that generate an output signal phase-locked to a reference, play a crucial role in achieving this objective. PLLs are employed for numerous purposes, including clock generation in a microprocessor,[5–7] frequency synthesis in cell phones,[8] signal modulation in communication systems, and synchronization in digital audio and video devices.[9]

Traditionally, PLLs have been extensively studied in the context of analog oscillators, with Adler's pioneering work laying the foundation for this area.[10] However, the transition to digital technology

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necessitates reevaluating the phase-locking mechanism. Unlike analog oscillators, where both amplitude and phase exhibit continuous dynamics, digital oscillators maintain a constant amplitude, manifesting all dynamical effects through discrete transition events. Precise phase alignment in digital oscillators is particularly critical because even minor phase discrepancies can severely impact data transmission and processing accuracy. Maintaining synchronized clocks is crucial but often challenging in distributed computing environments, where issues such as sampling jitter, lost samples, and communication delays can significantly degrade the performance of the network.[11,12] Consequently, effective phase locking mechanisms are critical for maintaining synchronization across digital communication networks.

Event-based sampling presents a promising alternative to conventional time-triggered control in digital systems. By updating the control only at the event times rather than at fixed intervals, event-based methods can reduce unnecessary control actions and power consumption, offering a promising approach for modern digital systems. Some designs have been proposed for PLLs that use event-based sampling to enhance synchronization precision in digital systems. For instance, in Ref. 13, a hybrid phase-locked loop with a sample-and-hold phase detector was introduced.

In the rest of the paper, we will introduce the novel event-based control model for hybrid PLLs that integrates digital signals with an analog first-order low-pass filter. By focusing on the transition times that characterize the dynamics of digital signals, we establish a mathematical framework for analyzing phase-locking in digital oscillators. Considering both positive and negative feedback, we explore how the oscillator evolves in response to discrete control. The discrete nature of digital oscillators allows us to model their dynamics as a discrete itterative map. By identifying the boundaries of the discrete map, we derive Arnold's tongue, which is traditionally used to describe synchronization in analog systems but has been underexplored in the digital domain.

II. EVENT-BASED MODELS

We propose a model with an event-based control to study phase-locking in PLL circuits where both the output and the reference signals are digital. The phase detector (PD) compares the output with the reference signal to detect mismatches. The frequency of the voltage-controlled oscillator (VCO) is controlled by an analog signal generated by a low-pass filter (LF). Figure 1 shows a schematic of the circuit under study and our approach to modeling it, which is also explained in Ref. 14. To leverage the discrete nature of digital signals, the control signal in our proposed model is sampled only when there is a transition event in the plant oscillator. This event-based sampling approach offers a compelling alternative to periodic sampling methods.[15,16] Unlike the traditional sampled-data techniques, which update the control signal at fixed intervals, event-based sampling updates it only at event times. We consider instantaneous output transfer as feedback. Assuming that the amplitude is constant, which can be well implemented in digital oscillators, a digital signal can be constructed by summing up Heaviside functions with opposite signs at consecutive transition times t_n, corresponding to the instances when the oscillator's output switches between zero and one,

$$x(t) = \sum_{n=0}^{\infty} (-1)^n H(t - t_n). \tag{1}$$

Note that $n = 0$ specifies the initial state of the oscillator. The sign of the power of -1 corresponds to the rising and falling edges of the signal, and it determines the transition direction, as indicated by the arrows in Fig. 1. Further details on constructing digital signals using Heaviside functions are provided in Appendix A.

As shown in Fig. 1, the output of the PD, x^{PD}, is the input for the low-pass filter. By filtering out the high-frequency components of the phase detector signal, the low-pass filter provides a low-frequency control to ensure smooth tuning of the frequency of
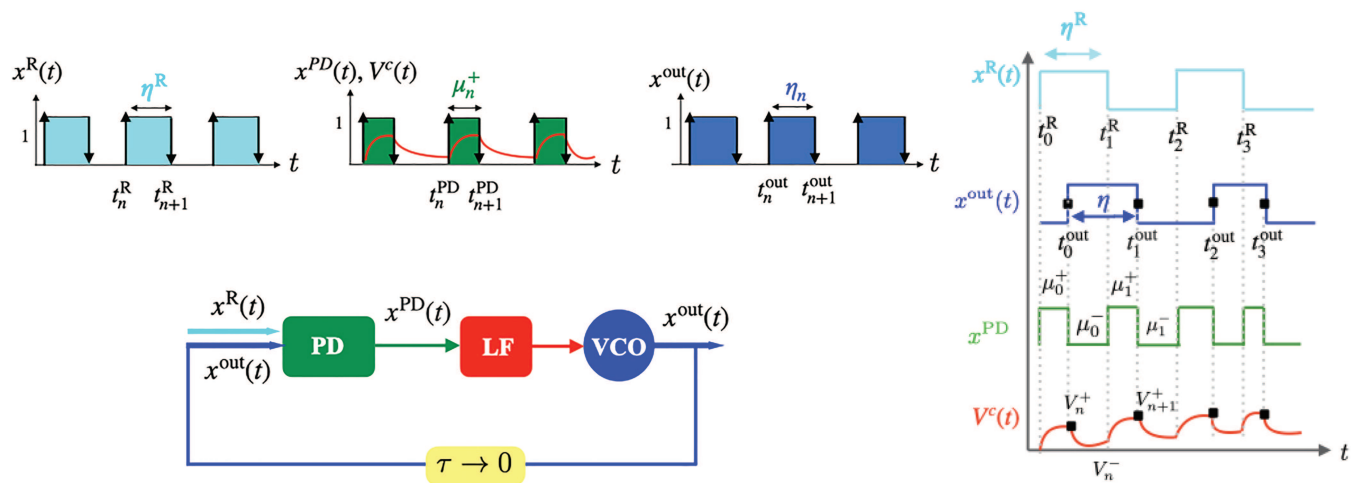
FIG. 1. Parts of a digital PLL: the phase detector (PD), low-pass filter (LF), and voltage-controlled oscillator (VCO). We consider the time delay, τ, to be negligible. The arrows indicate the direction of transitions $x^{\mathrm{R}}(t)$ is the reference signal, $x^{\mathrm{out}}(t)$ the output signal, $x^{\mathrm{PD}}(t)$ the phase detector signal, and $V^c(t)$ is the control signal.

the VCO. The response of the first-order LF, which is an RC circuit, to a digital PD signal x^{PD} can be described by the following first-order differential equation:

$$\frac{1}{\lambda}\frac{dV^c(t)}{dt} = -V^c(t) + x^{\text{PD}}(t). \tag{2}$$

The upper index c in V^c emphasizes that the control signal is a continuous function of time; and $\lambda = 1/RC$ represents the cutoff frequency of the filter. To discretize this continuous control signal, we consider a sample-and-hold type of control approach, which leads to event-based sampling in digital oscillators. In this scenario, the control signal is sampled at each transition event of the VCO. Equation (2) is solvable given the initial conditions. The sampled discrete control signal at the transition times, t_n, can be written as

$$V^c(t_n) = V^c(t)\delta(t - t_n), \tag{3}$$

where δ is the Dirac delta function, which is one at t_n and zero everywhere else. Note that $V^c(t_n)$ is the control signal $V^c(t)$ sampled at time t_n, with n being the nth transition event of the VCO's digital signal.

In most PLL circuits, the frequency response of the VCO to the control signal is considered to be linear,[3]

$$\omega(t) = \omega_0 + KV^c(t), \tag{4}$$

where ω_0 is the intrinsic frequency and K is the sensitivity of the VCO. We transform this frequency domain equation into a time domain representation, which allows us to perform our analysis on the transition times of the digital signal. By leveraging the inverse relation between period and frequency, $\omega/2 = \eta$, where η is the interval between two consecutive transition events (half the period of the oscillation), we rewrite Eq. (4) in terms of transition times. Here, the sampled control signal $V^c(t_n)$, as defined in Eq. (3), determines the duration of the state until the next transition,

$$\eta_{n+1} = \frac{1}{\eta_0 + KV^c(t_n)}. \tag{5}$$

Thus, the interval η between consecutive transitions is dynamically adjusted based on the sampled control signal. Conventionally, ω is defined as the steady state frequency, while our model involves an active control and transient dynamics, where $\eta_n \neq \eta_{n+1}$. The primary objective of the PLL with digital output is to generate a square wave that is phase-locked to the reference signal. The sampled value of the control signal $V^c(t_n)$ defines the duration of each interval between consecutive transitions. This event-based update rule determines how the VCO evolves and sets the timing of the next transition event in the output signal,

$$t_{n+1}^{\text{out}} = t_n^{\text{out}} + \eta_n. \tag{6}$$

The sequence of transition times, t_n^{out}, can be used to reconstruct the digital output signal according to Eq. (1), as previously described,

$$x^{\text{out}}(t) = \sum_{n=0}^{\infty} (-1)^n H\left(t - t_n^{\text{out}}\right). \tag{7}$$

The reference signal is deterministic, and its transition times follow the rule

$$t_{n+1}^{\text{R}} = (n+1)\eta^{\text{R}}, \tag{8}$$

where η^{R} is the interval between two consecutive edges of the reference signal. We drop the lower index for η for two reasons: First, we consider an exact reference, without cycle-to cycle variation. Second, we consider a reference with a 50% duty cycle, meaning that the high and low states of the signal are of equal duration. The reference signal can be built according to Eq. (1) based on the transition times t_n^{R},

$$x^{\text{R}}(t) = \sum_{n=0}^{\infty} (-1)^n H\left(t - t_n^{R}\right). \tag{9}$$

In the following sections, we study the effect of self-acceleration and self-inhibition, corresponding to positive and negative feedback. When positive feedback is implemented, the output of the PD is either zero or one. In the negative feedback case, the output of the PD is either zero or minus one.

III. POSITIVE FEEDBACK

When an XOR gate is used as a phase detector $\left(x^{\text{PD}^+}(t) = x^{\text{R}}(t) \oplus x^{\text{out}}(t)\right)$, the output is one when two inputs are different and zero when they are the same. The PD signal can be obtained using an XOR operation on x^{out} and x^{R} signals, defined in Eqs. (8) and (10). With XOR, the set of transition times in the phase detector can be written as:

$$\left\{t_n^{\text{PD}}\right\}_0^{\infty} = \left\{t_n^{\text{R}}\right\}_0^{\infty} \cup \left\{t_n^{\text{out}}\right\}_0^{\infty} - \left\{\left\{t_n^{\text{R}}\right\}_0^{\infty} \cap \left\{t_n^{\text{out}}\right\}_0^{\infty}\right\}. \tag{10}$$

The phase detector signal can be expressed as a function of the transition times in the PD signal, t_n^{PD}. In the case that XOR is used as a phase detector, the PD signal can be written as

$$x^{\text{PD}}(t) = \sum_{n=0}^{\infty} (-1)^n H\left(t - t_n^{\text{PD}}\right). \tag{11}$$

The solution of Eq. (2) can be written as a function of transition times of the PD signal, i.e., t_n^{PD}, and with the initial condition $V^c(t_0 = 0) = 0$ and the assumption that the first edge is a rising edge, the solution can be written as

$$V^c(t) = \sum_{n=0}^{\infty} (-1)^n \left(1 - e^{-\lambda\left(t - t_n^{\text{PD}}\right)}\right) H\left(t - t_n^{\text{PD}}\right). \tag{12}$$

This forms the foundation of our mathematical analysis. The event-based model with this type of phase detector can be summarized as

$$x^{\text{PD}}(t) = \sum_{n=0}^{\infty} (-1)^n H\left(t - t_n^{\text{PD}}\right).$$

$$\frac{1}{\lambda}\frac{dV^c(t)}{dt} = -V^c(t) + x^{\text{PD}}(t), \qquad V^c(t_n) = V^c(t)\delta(t - t_n). \tag{13}$$

$$\eta_{n+1} = \frac{1}{\eta_0 + KV^c(t_n)}, \qquad t_{n+1}^{\text{out}} = \eta_n + t_n^{\text{out}}.$$

We will now investigate feedback mechanisms for two cases: without a reference and with external entrainment.

A. Self-feedback with no reference

In this section, we focus on a closed-loop PLL without an external reference signal, where the PD receives only the VCO's output as input, thus forming a self-feedback loop. Figure 2 shows the numerical simulation results and the analytic solution for this case. In the simulation, the interval durations between transition events are computed according to Eq. (5), and the consecutive transition times are derived from Eq. (6). Using the notation presented in Fig. 1, the transition times of the output and PD signals can be expressed as

$$
\begin{aligned}
t_{n+1}^{\text{out}} &= t_n^{\text{out}} + \eta_n, \\
t_{n+1}^{\text{PD}} &= t_n^{\text{PD}} + \mu_n^+, \\
t_{n+2}^{\text{PD}} &= t_n^{\text{PD}} + \mu_n^+ + \mu_n^-,
\end{aligned}
\tag{14}
$$

μ^+ represents the interval between two consecutive edges in the PD signal where the amplitude is one, and μ^- is the interval between consecutive edges where the PD signal is zero. Since there is no external reference, μ_n is the same as η_n. Therefore, the phase detector's output is identical to its input, i.e., $x^{\text{out}}(t) = x^{\text{PD}}(t)$. Based on the transition times, the output signal (upper plot) and PD signal (lower plot) in Fig. 2 are generated according to Eqs. (11) and (7). The solid red lines result from numerical simulations of the control voltage obtained by solving the differential equation, Eq. (2), with a time step of $dt = 0.0001$, starting from the initial value $V_0 = 0$ and using the final value at each time interval as the initial value for the next interval. Figure 2 shows that the control signal reaches a two-state steady state after a short transient period. It is important to note that we intentionally use a short integration time to observe the underlying dynamics. However, for practical applications, the integration time needs to be large enough to provide a smooth control signal. To analytically solve the discrete control signal, we substitute the transition times from Eq. (14) into Eq. (12). Inserting η^+ and η^- results in a geometric series with a constant ratio between successive terms. Summing this geometric series yields the two solutions at the transition points,

$$
V^+ = \frac{1 - e^{-\lambda \eta^+}}{1 - e^{-\lambda(\eta^+ + \eta^-)}},
\tag{15}
$$

$$
V^- = \frac{e^{-\lambda \eta^-} - e^{-\lambda(\eta^+ + \eta^-)}}{1 - e^{-\lambda(\eta^+ + \eta^-)}}.
\tag{16}
$$

From Eq. (5), it is clear that the two-value control signal leads to a two-valued steady state: η^+, η^-, which can be obtained by substituting Eqs. (15) and (16) into Eq. (5),

$$
\eta^- = \left(\frac{1}{\eta_0} + K \frac{1 - e^{-\lambda \eta^+}}{1 - e^{-\lambda(\eta^+ + \eta^-)}} \right)^{-1},
\tag{17}
$$

$$
\eta^+ = \left(\frac{1}{\eta_0} + K \frac{e^{-\lambda \eta^-} - e^{-\lambda(\eta^+ + \eta^-)}}{1 - e^{-\lambda(\eta^+ + \eta^-)}} \right)^{-1}.
\tag{18}
$$

The interplay between the integration time of the LF and the sensitivity of the VCO defines the duty cycle and output frequency. Figure 3 illustrates the change in η^+ and η^- for different integration times of the LF and sensitivity of the VCO. The solid lines represent the result of numerical simulations when η^+ and η^- reach the steady state, while the black dots correspond to the analytical solution derived from Eqs. (17) and (18). The upper panel shows that for large λ, the output exhibits a non-fifty-percent duty cycle, meaning $\eta^+ \neq \eta^-$. Conversely, for small λ, η^+ and η^- converge, resulting in a 50% duty cycle. The free-running frequency of the VCO can be obtained from this plot as a function of its sensitivity, K, and the integration time of the LF. The strength of the VCO's reaction to an external signal determines the extent of its influence from the reference. The lower panel demonstrates that independent of the integration time of the LF, for a very large K, the oscillator reaches a state where $\eta^+, \eta^- = 0$, representing entrainment to the zero reference.
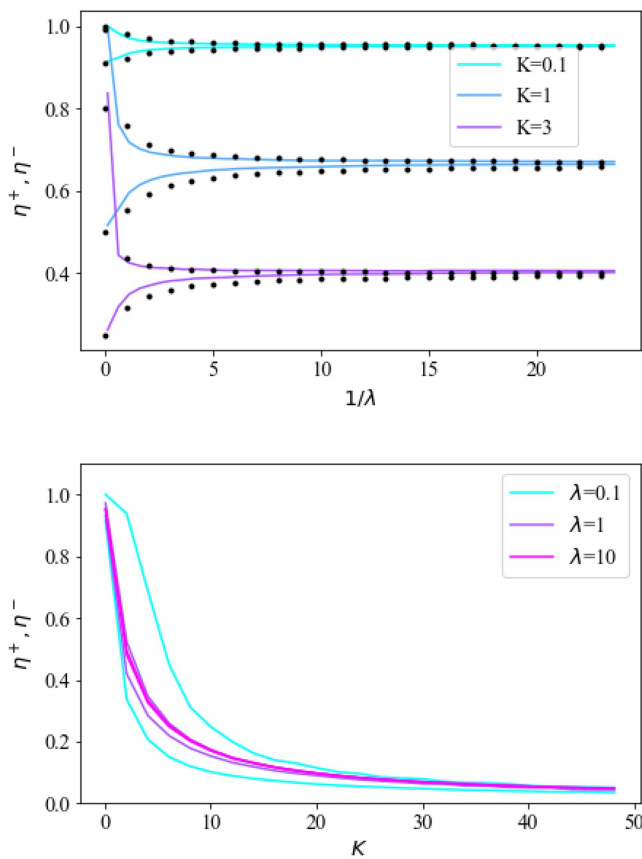
B. Entrained feedback loop

In the previous section, we examined how a VCO oscillates in a closed loop without an external signal. To understand phase-locking to an external reference, we now study the dynamics of the VCO response to an external entrainment with different intrinsic frequencies. With XOR used as the phase detector, the PD signal can be constructed using Eq. (11), which then can be used as an input into the Eq. (2) to give the control signal. The control signal is then sampled at the transition times of the VCO, according to Eq. (3) to update η as defined in Eq. (5). Note that since here there is a reference, one edge of the PD signal is contributed by VCO and the other by the reference. To be able to construct a formulation, we assume that the order of events does not change. The transition times of the output t^{out}, reference t^{R}, and the phase detector t^{PD}, can then be written as,

$$
\begin{aligned}
t_{n+1}^{\text{out}} &= t_n^{\text{out}} + \eta_n, \\
t_{n+1}^{\text{R}} &= t_n^{\text{R}} + \eta^{\text{R}}, \\
t_{n+1}^{\text{PD}} &= t_n^{\text{PD}} + \mu_n^+, \\
t_{n+2}^{\text{PD}} &= t_n^{\text{PD}} + \mu_n^+ + \mu_n^-,
\end{aligned}
\tag{19}
$$
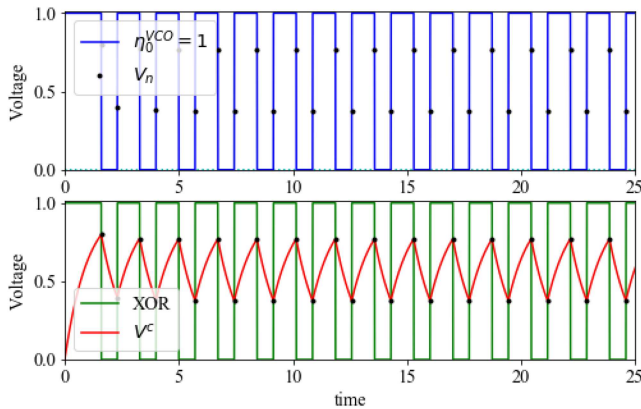
FIG. 2. Phase locking in a self-feedback loop. In this case, the reference is zero. The upper plot shows the output. In the lower plot, the PD signal is shown in green, and the control signal is in red. The black dots are the sampled values of the control signal at the transition points of the VCO signal.
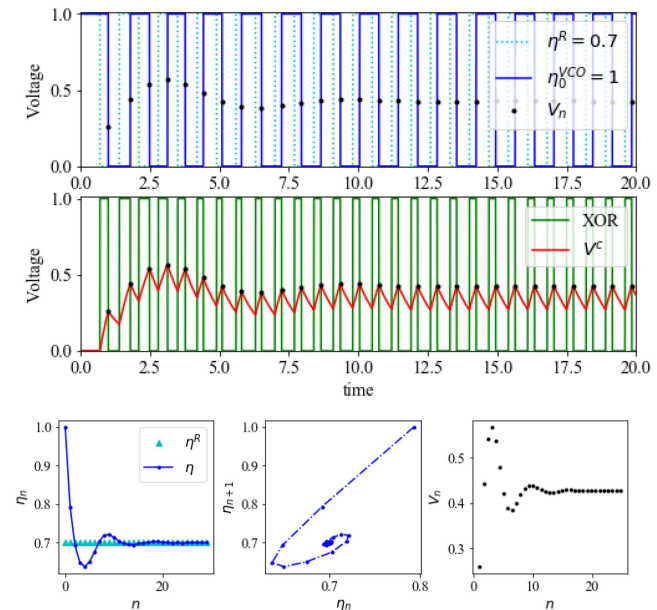
FIG. 4. Phase locking for $\eta^R = 0.7$, $\eta_0 = 1$, $K = 1$, and $\lambda = 1$. The upper plot shows the reference signal in light blue and the output signal in dark blue. The phase detector signal is shown in green, and the control signal is shown in red, which is obtained by numerical integration of Eq. (2). The black dots in both panels represent the value of the control signal at the update time of the VCO, i.e., $V(t_n)$ which is obtained analytically using Eqs. (21) and (22). The lower panels show the transition to the locked state.

FIG. 3. Upper plot: the effect of integration time of the LF on the duration of the output, i.e., η^+, η^-, for different values of the VCO sensitivity K in the zero reference case. Lower plot: The effect of the sensitivity of the VCO on the steady state of η^+ and η^- with different integration times in the zero reference case.

where μ^+ is the nonzero part of the PD signal and μ^- is the zero part, as shown in Fig. 1.

We argue that μ^+ is the counterpart of the phase mismatch in analog oscillators. For the $1:1$ locking case, μ^+ can be written as

$$\mu_{n+1}^+ = \eta^R - \eta_n + \mu_n^+. \tag{20}$$

Figure 4 shows an example simulation of the signals, where $\eta^R = 0.7$ and $\eta_0 = 1$, which are half the period of the reference and the VCO respectively. To maintain a consistent framework throughout the paper, we assume all signals start with a rising edge at zero, without an initial phase shift between the VCO and the reference. A similar analysis can be conducted for the opposite case or when the two signals initially start in opposite states. Note that the PD signal can differ depending on the initial conditions. The continuous control signal $V^c(t)$ is obtained from Eq. (2) for the detected PD signal. The sampled control, $V^c(t_n)$ on the nth event in the discrete formulation is represented by V_n, which is shown with the black dots on the control signal and on the VCO and separately in the lower right
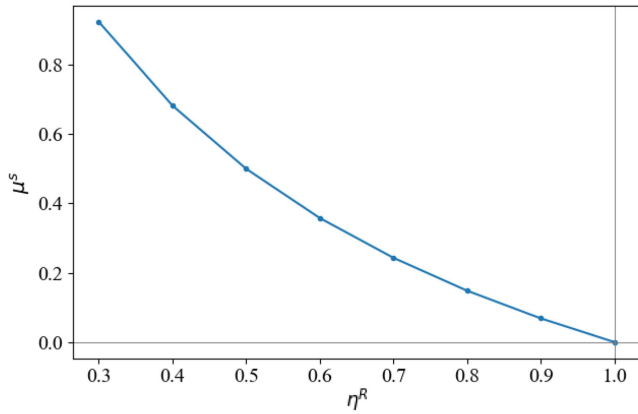
panel of Fig. 4. The sampled control signal determines the time of the upcoming event t_{n+1} according to Eq. (6).

Note that the sampling points of the control signal occur at the edges of the PD signal that are contributed by the VCO. Since the control signal is obtained by an RC circuit, the output represents charging when the input is nonzero and discharging otherwise. A schematic illustration is provided in Appendix B. The control signal exhibits transient dynamics and reaches a steady dynamics. The lower value of the control signal that occurs at the transition edge of the reference signal does not directly contribute but rather sets a lower limit for the control signal from which the charging starts again. In other words, the width of the PD signal's nonzero part sets the control signal's amplitude. This results in steady locking to the reference, as shown in the leftmost panel of Fig. 4.

Note that the plot of η_{n+1} vs η_n in Fig. 4 shows a steady state at the diagonal line, indicating $\eta_{n+1} = \eta_n$, where the system reaches a steady-state fixed point. In this state, the VCO follows the frequency of the reference, because of the control signal. In other words, the constant phase shift provides the required control for the VCO to maintain the lock. This state will be referred to as $1:1$ locking. Since they start in-phase with different intrinsic frequencies, the phase shift causes a frequency locking for a VCO with an intrinsic frequency different than the reference signal. Note that since there is active control, the VCO stays locked to the frequency of the reference signal through the control signal. Although there is a transient

FIG. 5. The steady-state value of μ^+ for different values of η^R in the entrained case.

FIG. 6. Phase locking with a cycle. The colors are the same as in Fig. 4. $K = 1$, $\lambda = 1$ for the case that $\eta^R = 0.51$ which is close to $\eta_0/2$.

dynamics, the control signal reaches a steady state caused by the phase shift between the two signals. Here, μ^+ is the required digital phase shift between two signals to keep them locked. Note that in synchronization models like the Kuramoto model, the phase difference between two oscillators, $\Delta\theta$, provides the modification in intrinsic frequency. For digital oscillators, μ^+ plays a similar role. Figure 5 shows how the steady-state nonzero shift between the two signals, μ^s, changes as a function of changes in the reference signal. The event-based control is defined in such a way that by detecting the mismatch between the reference and the output, the PD signal settles to a mismatch, the counterpart of the phase shift, pushing the system into a state in which a phase shift leads to frequency locking.

The control signal at the event times of the PD signal can be caluclated by doing a geometric sum. Further details are provided in Appendix C.
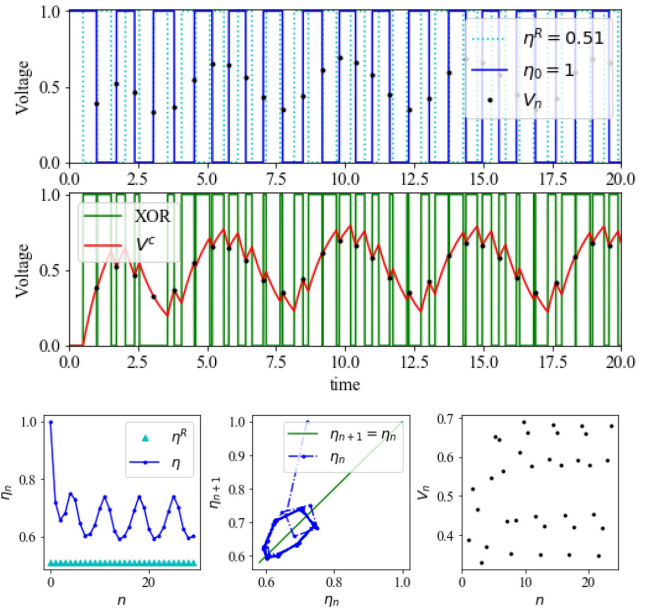
$$V^+ = \frac{1 - e^{-\lambda\mu^+}}{1 - e^{-\lambda\left(\mu^+ + \mu^-\right)}}, \tag{21}$$

$$V^- = \frac{e^{-\lambda\mu^-} - e^{-\lambda\left(\mu^+ + \mu^-\right)}}{1 - e^{-\lambda\left(\mu^+ + \mu^-\right)}}. \tag{22}$$

V^+ is the higher value of the control signal sampled at the transition edge of the VCO, and V^- is the control value at the edge contributed by the reference. Since the sampling always occurs at the same edge, it leads to $\eta^+ = \eta^-$. Using Eq. (5), we get

$$\eta^+ = \eta^- = \left(\frac{1}{\eta_0} + K\frac{1 - e^{-\lambda\mu^+}}{1 - e^{-\lambda\left(\mu^+ + \mu^-\right)}}\right)^{-1}. \tag{23}$$

As mentioned previously, η^+ and η^- are indirect functions of μ^-. This solution is valid only in the parameter region where the assumption of 1 : 1 locking holds, as shown in Fig. 4. In Fig. 6 we provide an example where the 1 : 1 locking condition does not hold, leading the system to a periodic state with a period higher than one. In this case, an oscillatory behavior in the control signal is observed.

More examples of entrainment to different reference clocks can be found in Appendix D.

The same approach as in the simulations of Fig. 4 is used in Fig. 7 for different values of K and η^R to illustrate how the sensitivity of the VCO and the frequency difference between the reference and the VCO affect the locking dynamics. In Fig. 4, $K = 1$, which is also the case in the middle row of Fig. 7. We also consider other values for K of $K = 0.5$ and 1.5. Note that we use different measures for locking: η/η^R and $\eta - \eta^R$. When $\eta - \eta^R = 0$ and $\eta/\eta^R = 1$, there is 1 : 1 locking between the VCO and the reference. We also plot the consecutive values of η in the last column of Fig. 7. In this case, locking with a cycle of length zero occurs when the steady state ends up on the diagonal line and remains there. Cycles with higher length also appear. As seen in the last column, a change in the sensitivity K alters the steady-state dynamics and the length of the cycle. For instance, when η^R is close to $\eta_0/2$, such as when $\eta^R = 0.55$, increasing K shifts the system's steady state from being a cycle of higher length to a cycle of length zero. For the case of $\eta^R > \eta_0$, $\eta^R = 1.1$ as an example, an increase in K reduces the length of the cycle as well as its enclosed area. In the following sections, we will address this in more detail to demonstrate that cycles with length higher than zero result from positive feedback. Applying negative feedback will drive the system to a state with a cycle of length one. Later, we will derive the boundaries of different dynamical regions and explore the parameter space by introducing a discrete map.

IV. NEGATIVE FEEDBACK

As we observed in previous sections, when $\eta_0 < \eta^R$, using XOR as a phase detector does not lead to 1 : 1 locking. To investigate the
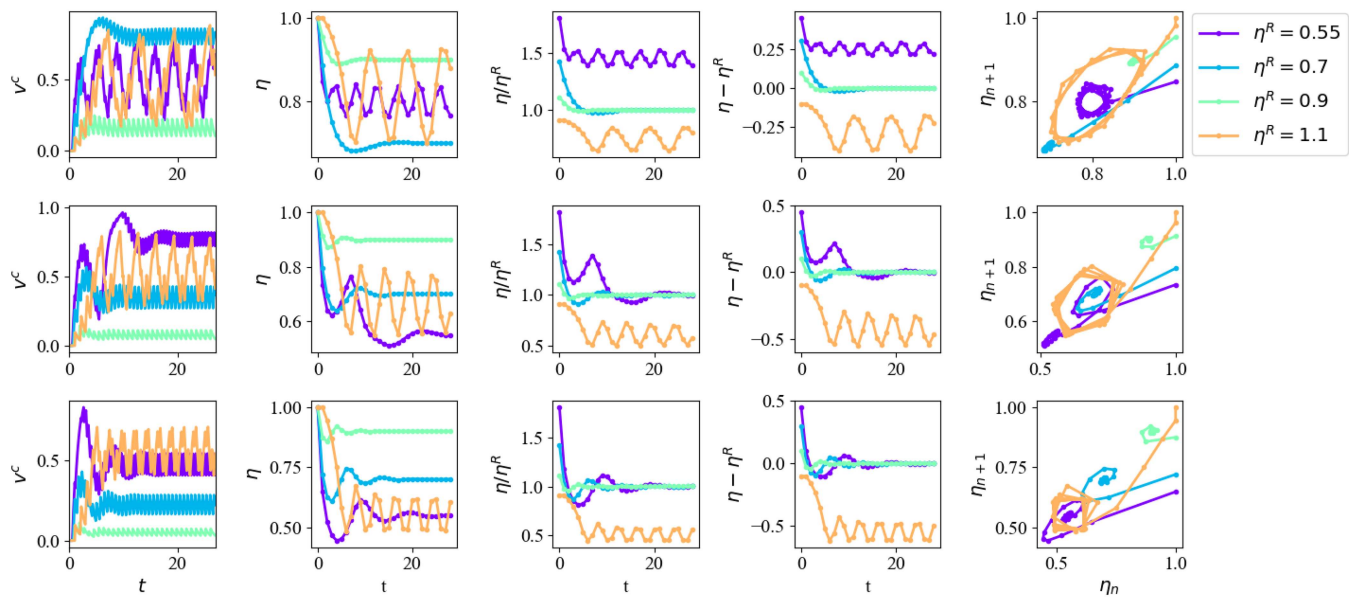
FIG. 7. The effect of K and η^R on the case of $\lambda = 1$ for a positive PD. In the first row, $K = 0.5$; in the second row, $K = 1$; and in the third row, $K = 1.5$. In all the simulations $\eta_0 = 1$.

possibility of achieving 1:1 locking under this condition, we explore the case in which the PD signal produces -1 and 0 as output whenever $\eta_0 < \eta^R$. The phase detector signal can then be represented as

$$x^{\mathrm{PD}^-}(t) = \sum_{n=0}^{\infty} (-1)^{(n+1)} H\left(t - t_n^{\mathrm{PD}}\right). \qquad (24)$$

Note that the power of (-1) differs from the definition given in Eq. (11). Figure 8 presents the simulation result for a VCO with $\eta^R = 1.2$ using a phase detector similar to XOR but with an amplitude of -1. As the evolution of η shows the system reaches a 1:1 locking state. Although under positive feedback this was not possible. To study the effect of the sensitivity of the VCO and the mismatch between the reference η and that of the VCO, we show simulation results for different values in Fig. 9. Clearly, the negative feedback leads the case of $\eta_0 < \eta^R$ to a 1:1 locking state and not the higher length limit cycle observed with positive feedback.

Figure 10 summarizes the phase locking $\langle \eta - \eta^R \rangle$ in the parameter space of η^R and K for the case where $\eta^R = 1$. The purple color indicates regions where $\langle \eta - \eta^R \rangle$ is small, which indicates 1:1 locking. Locking occurs in a region around η^R. For $\eta_0 < \eta^R$, positive feedback is applied, while for $\eta_0 > \eta^R$, negative feedback is needed to achieve a 1 : 1 locked state. To develop an intuition for the dynamics outside this locking region, we performed a simulation for the parameter values outside this region and observed higher orders of locking. Note that $\eta - \eta^R$ does not provide information about the cycles of length higher than one.

V. DISCRETE MAP

In order to obtain the bifurcation boundaries of the system for different types of locking, we develop an analytic approach based on a discrete map for different orders of locking. This allows us to
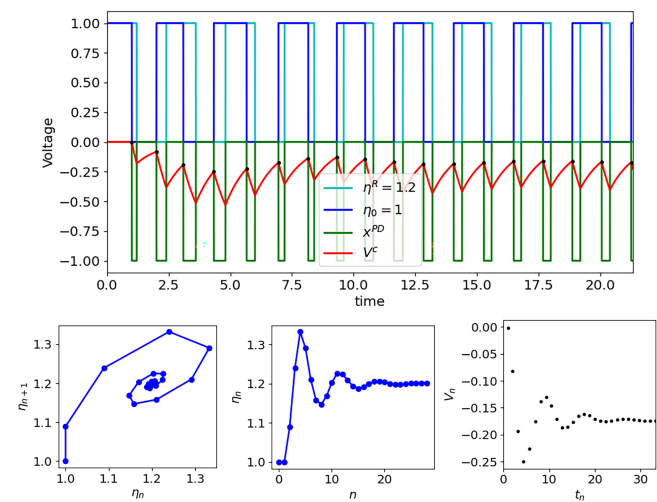
FIG. 8. In the first panel, the upper plot shows the reference signal in light blue and the output signal in dark blue. The lower part shows the phase detector signal in green and the control signal in red. The black dots are the VCO update times. For this case, $K = 1$, $\eta^R = 1.2$, $\lambda = 1$, and $\eta_0 = 1$. Discrete representation of numeric integration of the control signal, namely V_n, and η_n, which shows locking to the reference.
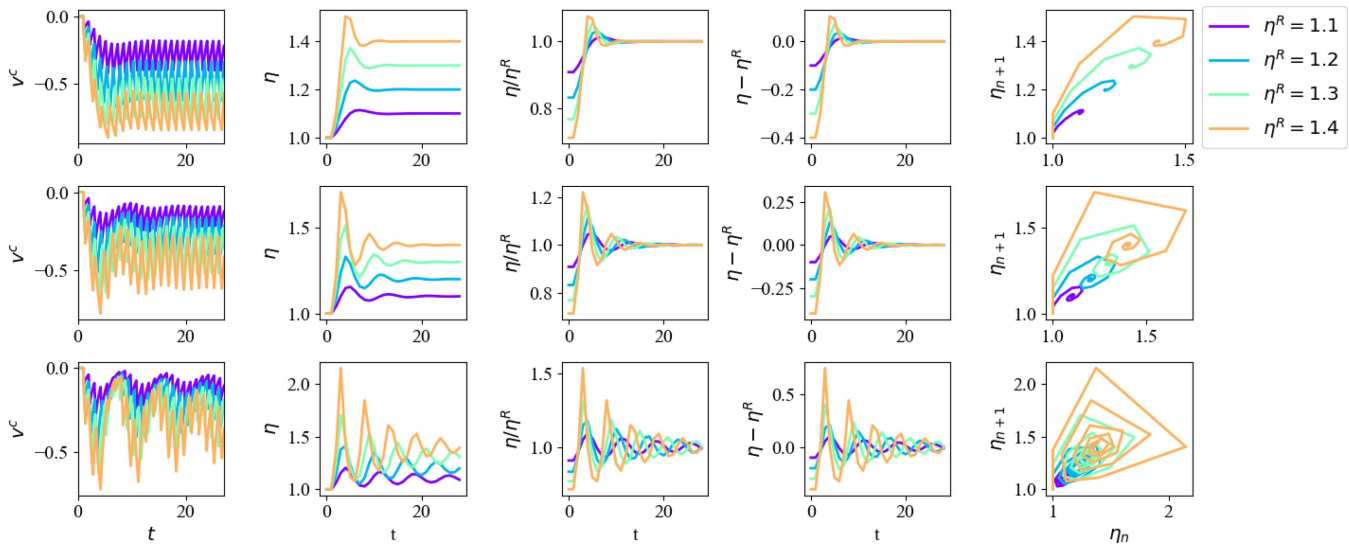
FIG. 9. Different values of K and η for the case of a negative PD with $\lambda = 1$. In the first row, $K = 0.5$; in the second row, $K = 1$; and in the third row, $K = 1.5$. In all the simulations $\eta_0 = 1$.

obtain the bifurcation boundaries of the system where the type of phase locking changes.

A. Positive feedback

1. Discrete map for 1:1 locking

In this section we aim to express the dynamics of the PLLs as a discrete map. Since the system has three elements, the state vector is

three-dimensional,

$$X_n = \begin{pmatrix} \mu_n^+ \\ \eta_n \\ V_n \end{pmatrix}. \tag{25}$$

Each dimension corresponds to one of the circuit elements: μ^+ for the PD, η for the VCO, and V for the LF. The dependence of μ_{n+1}^+ on μ_n in the 1:1 locking under positive feedback is represented by Eq. (20), and the dependence of η_{n+1} on η_n is given in Eq. (7). We need to consider a discretized version of the integral control to obtain the control at time t_{n+1}, i.e., $V^c(t_{n+1})$. This involves solving the first-order differential equation for the low-pass filter [Eq. (2)] in the interval between t_n and t_{n+1} using the value of the PD signal in that interval. A schematic illustration can be found in Appendix B, Fig. 13. The control signal for $t_n < t < t_{n+1}$ can be expressed as
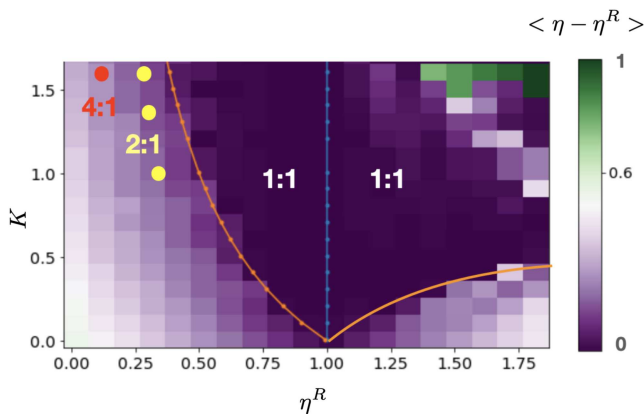
$$V^c(t|t_n < t < t_{n+1}) = V^c(t_n)e^{-\lambda(t-t_n)} + \lambda \int_{t_n}^{t_{n+1}} x^{\mathrm{PD}}(t)e^{-\lambda(t-t')}dt', \tag{26}$$

which is the solution of Eq. (2). In a discrete form, the control signal at time t_{n+1} can be written as

$$V_{n+1} = V_n e^{-\lambda(t_{n+1}-t_n)} + e^{-\lambda(t_{n+1}-t_{n+1})} - e^{-\lambda(t_{n+1}-t_n-\mu_n^-)}. \tag{27}$$

Using Eq. (6), this can be written in terms of η_n as

$$V_{n+1} = V_n e^{-\lambda\eta_n} + 1 - e^{-\lambda\mu_n^+}. \tag{28}$$

FIG. 10. A numerical simulation in the $\eta^R - K$ plane. The steady-state value of the duration of the output of the VCO, i.e., η, is averaged after the system reaches a steady state. The color shows the average value of $\eta - \eta^R$ in a window within the steady state. The boundaries for the 1:1 locking are shown as orange lines. In the outer region, there exist multiple lucking which means $\eta/\eta^R = 2, 4$, or higher.

Using the discrete representation of the control signal from Eq. (28), η_n from Eq. (5), and the μ^+ from Eq. (20), we can write a three-dimensional iterative map,

$$\begin{pmatrix} \mu_{n+1}^+ \\ \eta_{n+1} \\ V_{n+1} \end{pmatrix} = \begin{pmatrix} \eta^R - \eta_n + \mu_n^+ \\ \dfrac{1}{\dfrac{1}{\eta_0} + KV_n} \\ V_n e^{-\lambda \eta_n} + 1 - e^{-\lambda \mu_n^+} \end{pmatrix}. \qquad (29)$$

When the system reaches a steady state with a 1:1 locking, the state vector no longer changes. In this section, we focus on such a case. In the steady state, which corresponds to the states along the diagonal line in the η_{n+1} vs η_n plot in Fig. 4, we have

$$\begin{pmatrix} \mu_{n+1}^{+*} \\ \eta_{n+1}^* \\ V_{n+1}^* \end{pmatrix} = \begin{pmatrix} \mu_n^{+*} \\ \eta_n^* \\ V_n^* \end{pmatrix}. \qquad (30)$$

By substituting Eq. (29) into this steady-state condition, we can find the steady-state values of η, V, and μ. The fixed point can be obtained as

$$\begin{pmatrix} \mu^{+*} \\ \eta^* \\ V^* \end{pmatrix} = \begin{pmatrix} -\dfrac{1}{\lambda} \log \left[\dfrac{1}{K} \left(\dfrac{1}{\eta^R} - \dfrac{1}{\eta_0} \right) (e^{-\lambda \eta^R} - 1) + 1 \right] \\ \eta^R \\ \dfrac{1}{K} \left(\dfrac{1}{\eta^R} - \dfrac{1}{\eta_0} \right) \end{pmatrix}. \qquad (31)$$

The hold-in range is obtained by calculating the frequency where the PD signal is at its maximum. The maximum frequency difference before losing the lock in the PLL system is called the hold-in range (see Ref. 17, p. 258). Our numerical simulations show that in the case of 1 : 1 locking, the smaller the mismatch between the reference η^R and η_0, the smaller the value of μ^+ required to maintain the lock. When $\eta_R < \eta_0$, the system achieves 1 : 1 locking. Here, the XOR phase detector imposes the condition that the shift between the two signals cannot be out of the range $[0, \eta^R]$, that is $0 < \mu^+ < \eta^R$. We use this boundary condition to obtain the parameter region for which 1 : 1 locking holds. By inserting the two extreme values of this interval, $\mu^+ = 0$ and $\mu^+ = \eta^R$, into Eq. (31), we obtain the imposed boundaries for 1 : 1 locking,

$$0 < \frac{1}{\eta^R} - \frac{1}{\eta_0} < K, \qquad (32)$$

which is shown in Fig. 10 in orange and in Fig. 11 in magenta for $\eta^R < 1$. Since $1/\eta$ is proportional to the frequency, $\frac{1}{\eta^R} - \frac{1}{\eta_0}$ is the counterpart of the frequency mismatch in analog oscillators. In the Kuramoto model, for instance, the frequency mismatch has to be within a certain range to allow synchronization.[18] Here, Eq. (32) provides such a condition for 1:1 locking in digital oscillators.

2. Discrete map for multiple locking

We perform numeric simulations to explore the parameter space and understand the behavior outside the 1 : 1 locking region. As shown in Fig. 10, in addition to 1 : 1 locking, multiple-locking states exist (2 : 1 and 4 : 1,...), where the control signal reaches a
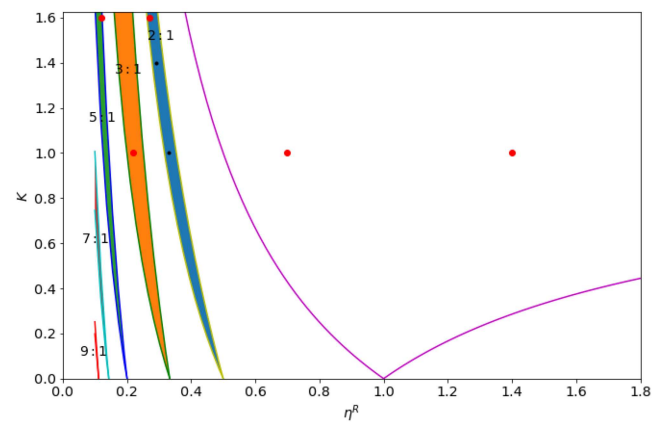

FIG. 11. Arnold's tongue for digital oscillator with $\lambda = 1$ and $K = 1$.

cyclic behavior with a period of length higher than one, for certain values of the external reference. Detailed examples are provided in Appendix D. As demonstrated in Appendix E, the 1 : 1 discrete map does not hold in this region. In the following, we derive the iterative map for the case of $\eta/\eta^R = 3$, which is a 3 : 1 locking. For this case, the discretized control signal can be written as

$$V_{n+1} = V_n e^{-\lambda(2\eta^R + \mu_n^- + \mu_n^+)} + \left(e^{-\lambda(\eta^R + \mu_n^+)} - e^{-\lambda(2\eta^R + \mu_n^+)} \right)$$
$$+ \left(1 - e^{-\lambda \mu_n^+} \right). \qquad (33)$$

We can write the equation for η_{n+1} in order to find μ_{n+1}:

$$\eta_{n+1} = 2\eta^R + \mu_{n+1}^- + \mu_{n+1}^+. \qquad (34)$$

Using the condition imposed by the phase detector $\mu_{n+1}^- = \eta^R - \mu_n^+$, we have

$$\eta_{n+1} = 2\eta^R + \left(\eta^R - \mu_n^+ \right) + \mu_{n+1}^+ = 3\eta^R - \mu_n^+ + \mu_{n+1}^+. \qquad (35)$$

and from this, one can determine μ_{n+1} as a function of μ_n,

$$\mu_{n+1}^+ = \eta_{n+1} - 3\eta^R + \mu_n^+. \qquad (36)$$

Taking V from Eq. (33), the equation for η from Eq. (5) and μ^+ from Eq. (36) we can write the map as

$$\begin{pmatrix} \mu_{n+1}^+ \\ \eta_{n+1} \\ V_{n+1} \end{pmatrix}$$
$$= \begin{pmatrix} \eta_{n+1} - 3\eta^R + \mu_n^+ \\ \dfrac{1}{\dfrac{1}{\eta_0} + KV_n} \\ V_n e^{-\lambda(2\eta^R + \mu_n^- + \mu_n^+)} + e^{-\lambda(\eta^R + \mu_n^+)} - e^{-\lambda(2\eta^R + \mu_n^+)} + 1 - e^{-\lambda \mu_n^+} \end{pmatrix}.$$

In the steady state, we have

$$\begin{pmatrix} \mu_{n+1}^{+*} \\ \eta_{n+1}^* \\ V_{n+1}^* \end{pmatrix} = \begin{pmatrix} \mu_n^{+*} \\ \eta_n^* \\ V_n^* \end{pmatrix}. \qquad (37)$$

Therefore, the steady state can be written as

$$
\begin{pmatrix} \mu_n^{+*} \\ \eta_n^* \\ V_n^* \end{pmatrix} = \begin{pmatrix} -\frac{1}{\lambda} \log \left[\frac{\frac{1}{K}\left(\frac{1}{3\eta^R} - \frac{1}{\eta_0}\right)\left[e^{-3\lambda\eta^R} - 1\right] + 1}{-e^{-\lambda\eta^R} + e^{-2\lambda\eta^R} + 1} \right] \\ 3\eta^R \\ \frac{1}{K}\left(\frac{1}{3\eta^R} - \frac{1}{\eta_0}\right) \end{pmatrix}. \quad (38)
$$

Using the condition $0 < \mu^+ < \eta^R$ imposed by the phase detector, one can find the boundaries for this solution in the parameter space. To do this, we plug the lower and the upper bound of the interval into the steady-state value of μ^+ in Eq. (38) and obtain the corresponding branch of Arnold's tongue,

$$
\frac{e^0\left(-e^{-\lambda\eta^R} + e^{-\lambda 2\eta^R} + 1\right) - 1}{\left(e^{-\lambda 3\eta^R} - 1\right)} < \frac{1}{K}\left(\frac{1}{3\eta^R} - \frac{1}{\eta_0}\right)
$$
$$
< \frac{e^{-\lambda\eta^R}\left[-e^{-\lambda\eta^R} + e^{-\lambda 2\eta^R} + 1\right] - 1}{\left(e^{-\lambda 3\eta^R} - 1\right)}, \quad (39)
$$

which is the boundary of the orange region in Fig. 11.

B. Negative feedback

A similar approach to that used for positive feedback can also be applied to negative feedback. As seen in previous sections, when $\eta_0 < \eta^R$, the XOR phase detector does not lead to locking with a limit cycle of length one. Negative feedback, however, leads to a state with a limit cycle of length one state, which previously exhibited a higher length cycle in the positive feedback case.

Using a similar approach to that for positive feedback, we find the control signal at time t_{n+1} as a function of the value of the control signal at time t_n by solving the first-order filter equation, Eq. (2), in this interval,

$$
V_{n+1} = V_n e^{-\lambda\eta_n} - e^{-\lambda\left(\eta_n - \mu_n^+\right)} + e^{-\lambda\eta_n}. \quad (40)
$$

Using the discrete control signal obtained in Eq. (40), μ^+ from Eq. (20), and η from Eq. (5), we can write the three-dimensional map,

$$
\begin{pmatrix} \mu_{n+1}^+ \\ \eta_{n+1} \\ V_{n+1} \end{pmatrix} = \begin{pmatrix} \eta^R - \eta_n + \mu_n^+ \\ \frac{1}{\frac{1}{\eta_0} + K V_n} \\ V_n e^{-\lambda\eta_n} - e^{-\lambda\left(\eta_n - \mu_n^+\right)} + e^{-\lambda\eta_n} \end{pmatrix}. \quad (41)
$$

The condition for a steady state is to have

$$
\begin{pmatrix} \mu_{n+1}^{+*} \\ \eta_{n+1}^* \\ V_{n+1}^* \end{pmatrix} = \begin{pmatrix} \mu_n^{+*} \\ \eta_n^* \\ V_n^* \end{pmatrix}. \quad (42)
$$

Substituting Eq. (41) into Eq. (42) and comparing the rows of the matrices on both sides, we can find the steady-state values. The

coordinates of the steady state can then be written as

$$
\begin{pmatrix} \mu^{+*} \\ \eta^* \\ V^* \end{pmatrix} = \begin{pmatrix} \frac{1}{\lambda} \log \left[\frac{1}{K}\left(\frac{1}{\eta^R} - \frac{1}{\eta_0}\right)\left(e^{-\lambda\eta^R} - 1\right) e^{\lambda\eta^R} + 1 \right] \\ \eta^R \\ \frac{1}{K}\left(\frac{1}{\eta^R} - \frac{1}{\eta_0}\right) \end{pmatrix}. \quad (43)
$$

Using the condition imposed by the phase detector, i.e., $0 < \mu^+ < \eta^R$, one can find the boundaries for this solution in the parameter space,

$$
0 < \frac{1}{\eta^R} - \frac{1}{\eta_0} < K \frac{\left(e^{\lambda\eta^R} - 1\right)}{\left(e^{-\lambda\eta^R} - 1\right) e^{\lambda\eta^R}}, \quad (44)
$$

which are plotted in magenta in Fig. 11 for $\eta^R > 1$. Inside this boundary, the system gets to a 1 : 1 locking state, although this was not possible with positive feedback. A similar approach to the previous section can be used to obtain higher-order locking boundaries for negative feedback as well.

C. General map for positive feedback

In this paper, by developing a discrete map, we have obtained a map for 1:1 and 3:1 locking in the positive feedback case. The map for other higher-order lockings can be obtained using the same approach. To generalize the expressions for the bifurcation boundaries obtained from these maps, we derive a general rule for the bifurcation boundaries of higher-order lockings,

$$
\frac{e^0\left(\sum_{w=0}^{W-1} (-1)^w e^{-w\lambda\eta^R}\right) - 1}{\left(e^{-\lambda W\eta^R} - 1\right)} < \frac{1}{K}\left(\frac{1}{W\eta^R} - \frac{1}{\eta_0}\right)
$$
$$
< \frac{e^{-\lambda\eta^R}\left(\sum_{w=0}^{W-1} (-1)^w e^{-w\lambda\eta^R}\right) - 1}{\left(e^{-\lambda W\eta^R} - 1\right)}, \quad (45)
$$

where W represents the locking ratio. Substituting in $W = 1$ gives Eq. (32) for 1 : 1 locking, and $W = 3$ gives Eq. (39) for 3 : 1 locking. These boundaries, together with the results for $W = 2, 5, 7, 9$, are shown in Fig. 11 with solid lines for values of $\eta^R < 1$. The bifurcation boundary for the negative feedback loop is the line in the $\eta^R > 1$ region as obtained from Eq. (44). The accuracy of this formula is tested by performing simulations for parameters within each region. Figure 11 defines the lock-in range of the loop for 1:1 and higher-ratio locking. In the context of synchronization, this is the counterpart of Arnold's tongue. Arnold's tongues describe the regions of parameter space where oscillators exhibit phase locking to a periodic external signal.

Additionally, using the fact that $1/2\eta$ is proportional to ω, Eq. (45) can be written as

$$\frac{e^0\left(\sum_{w=0}^{W-1}(-1)^w e^{-w\lambda\eta^R}\right)-1}{\left(e^{-\lambda W\eta^R}-1\right)} < \frac{1}{K}(F_W - F_0)$$

$$< \frac{e^{-\lambda\eta^R}\left(\sum_{w=0}^{W-1}(-1)^w e^{-w\lambda\eta^R}\right)-1}{\left(e^{-\lambda W\eta^R}-1\right)}.$$

(46)

where $F_W = 1/W\eta^R$ and $F_0 = 1/\eta_0$. This is similar to Adler's equation for analog oscillators,[19,20] which describes injection locking,

$$-\frac{1}{2Q}\frac{V_i}{V} \le \frac{\Delta f_0}{f_0} \le \frac{1}{2Q}\frac{V_i}{V}.$$

(47)

This expression provides the locking range of an oscillator with intrinsic frequency f_0. The frequency difference between the injected signal and the oscillator is Δf_0. The amplitude of the injected signal is V_i, and the output amplitude of the oscillator is V. Q is the figure of merit of the plate load in LCR circuit. In the case of Adler's equation, the range $-1 < \sin(\Delta\phi(t)) < +1$ gives the interval, where $\Delta\phi$ is the phase difference. In our model, the range imposed by the phase detector signal, $0 < \mu^+ < \eta^R$, sets the boundary.

VI. CONCLUSION

In this study, we have developed an event-based model for phase-locked loops (PLLs) with digital oscillator, leveraging their discrete nature to formulate phase-locking mechanisms. By focusing on transition times and using event-based sampling, our model addresses the limitations of traditional sinusoidal phase-locking methods, offering a more efficient and responsive approach for digital systems.

We have demonstrated the behavior of PLLs under both positive and negative feedback conditions, exploring the dynamics of the VCO in response to positive and negative control signals. We have investigated the conditions required to achieve 1:1 and higher ratios of frequency locking through numerical simulations and analytical methods. Our model specifies parameters for achieving different types of locking in PLLs with digital oscillators and analog filter.

The discrete map developed in this study using event-based sampling control provides a comprehensive framework for analyzing the phase-locking behavior of digital oscillators. By deriving bifurcation boundaries for different types of locking, we have outlined the parameter space for each type of phase locking, which are analogous to Arnold's tongues in synchronization theory for analog oscillators. Our model extends to higher ratio lockings, offering a generalized approach to understanding the complex dynamics of digital PLLs. In addition to the numerical simulation of the model, the solvable analytic approach makes it easy to obtain the dynamical characteristics of the system and get insight based on that for more efficient circuit design.

This research not only advances the theoretical understanding of phase locking in digital oscillators but also paves the way for practical applications in modern electronics. By aligning with the discrete characteristics of digital signals, our event-based model

enhances the performance and reliability of digital communication systems, providing a robust foundation for future circuit design and implementation.

Given that stability plays a crucial role in electronic circuits,[21,22] future research should investigate the stability of the dynamics using the discrete map. One factor affecting the dynamics of interacting oscillators is delay.[23] Given the prevalent use of these circuits in data transmission systems, studying the effect of time delay on phase locking is essential. Furthermore, in the high-frequency regime, even small amounts of noise can significantly impact system accuracy.[24–27] Therefore, this model can be used for studying the reaction of the system to noise and determining the parameter boundaries within which the circuit can maintain accurate operation despite noise. It is of particular interest to determine the maximum noise strength under which the circuit can remain locked with the reference under the control criteria suggested in this work. In addition, dynamic connectivity in a network of interacting oscillators affects the onset of synchronization. Explosive synchronization happens for specific network topologies and frequency distributions.[28,29] Further study could investigate the effect of dynamic-dependant connectivity in a network of digital phase-locked loops using the model suggested in this work. These studies will provide valuable insights into the practical application of PLLs and enable the design of more efficient and accurate systems for various uses.

Different designs for PLLs are customized for different applications. In this work, we used the general principle of PLLs to construct a basic physical model that abstracts from detailed circuit design while retaining fundamental characteristics and dynamics. This model serves as a foundational basis for a dynamical system model of PLLs, which can be extended to more complex and sophisticated designs depending on circuit specifications. For instance, here, we used the simplest possible phase detector, an XOR, and a variation of that. Our model can be generalized for designs including variations of phase-frequency detector[9,30,31] circuits like the ones with Flip-Flop. In addition, our model can be extended to model second-order PLLs and study their stability.[32] Furthermore, this model can be utilized to model the dynamics of the interacting PLLs.[33–35]

AUTHOR DECLARATIONS
Conflict of Interest

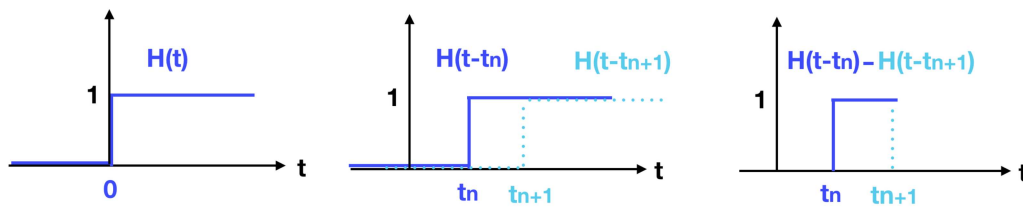The author has no conflicts to disclose.

FIG. 12. Construction of a digital signal using the sum of Heaviside functions with alternating signs.

Author Contributions

Sara Ameli: Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study will be available from the corresponding author upon reasonable request.

APPENDIX A: BUILDING A SQUARE WAVE FROM HEAVISIDE FUNCTIONS

A Heaviside function is a step function whose transition occurs at a given time. A piece of a digital signal can be constructed using two Heaviside functions with different signs, as shown in Fig. 12. Summing over such pieces, we construct a digital signal as a function of transition times.
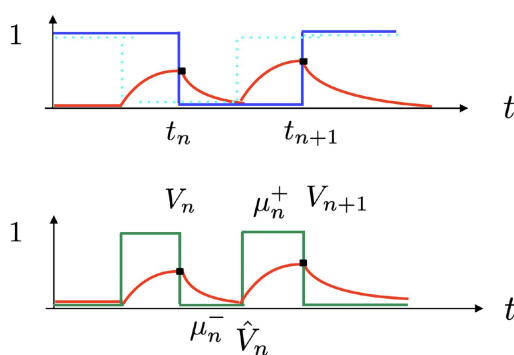
APPENDIX B: SCHEMATIC OF EVENT-BASED CONTROL

FIG. 13. Schematic of the charging and discharging of the RC filter. The dark blue is the output of the VCO, the light blue represents the reference signal. The green signal shows the output of the XOR gate operating on the reference and the VCO and the red line shows the output of the RC filter, when it receives the PD signal as an input.

APPENDIX C: ANALYTICAL SOLUTION OF THE CONTROL SIGNAL IN THE ENTRAINED PLL

To obtain the analytical solution of the control signal in the entrained case, we use the solution offered in Eq. (12).

As defined before, the nonzero state between two consecutive edges is defined as μ^+, and the zero part is defined as μ^-. We aim to obtain an analytical expression for the sampled control signal. With t_m^{PD} representing the edge contributed by the VCO, and t_n^{PD} representing the edge from the reference, when l is an even number, $t_m^{\mathrm{PD}} - t_n^{\mathrm{PD}} = l(\mu^+ + \mu^-) + \mu^+$, and when l is an odd number, $t_m^{\mathrm{PD}} - t_n^{\mathrm{PD}} = l(\mu^+ - \mu^-)$. Substituting these values into Eq. (2) and using $l = 2k$, $2k + 1$, we get

$$V\left(t_m^{\mathrm{PD}}\right) = \sum_{l=0}^{k}\left(1 - e^{-\lambda\mu^+}e^{-\lambda l(\mu^+ + \mu^-)}\right) - \sum_{l=0}^{k-1}\left(1 - e^{-\lambda(l+1)(\mu^+ + \mu^-)}\right),$$
(C1)

and

$$V\left(t_n^{\mathrm{PD}}\right) = \sum_{l=1}^{k}\left(1 - e^{-\lambda l(\mu^+ + \mu^-)}\right) - \sum_{l=1}^{k-1}\left(1 - e^{-\lambda(l-1)(\mu^+ + \mu^-) - \lambda\mu^+}\right).$$
(C2)

In the limit of large k, the sums turn into a geometric series. By calculating the geometric sum, we obtain the solution at each event time of the PD signal.
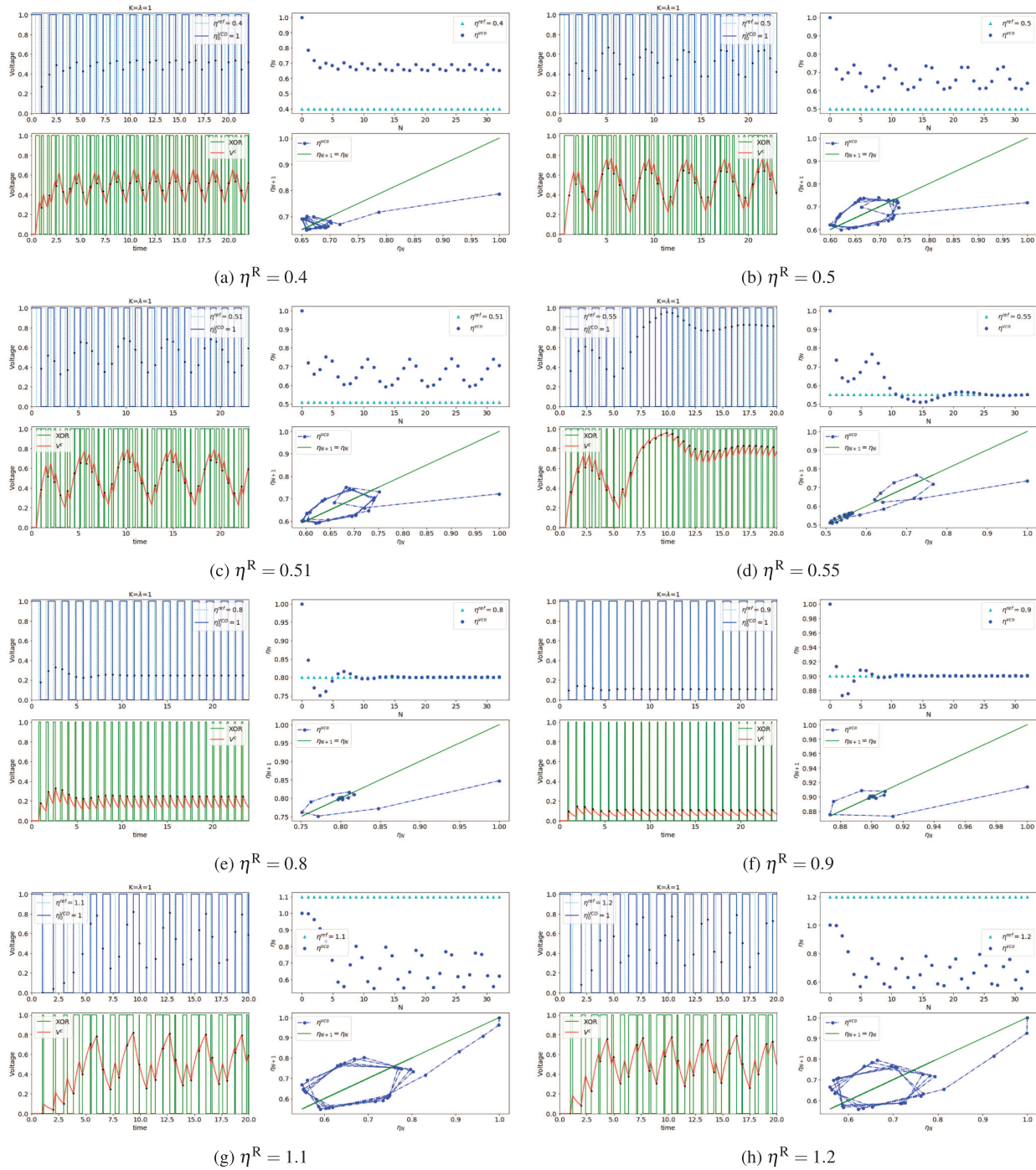
APPENDIX D: HIGHER ORDER LOCKING

In Fig. 14, we present the result of event-based models for phase-locking to different values of reference signal, represented by different η^Rs. Figures 14(d)–14(f) have a 1:1 locking state, while the others demonstrate limit-cycles of length higher than one, represented by a periodic loop. Note that while the limit cycle of length one has 50% duty cycle, the others do not reach that state. A marginal case is shown in Fig. 14(d), where after having a periodic loop, the system proceeds further to reach a fixed point.

APPENDIX E: REGION OF VALIDITY OF 1 : 1 DISCRETE MAPS

In the left column of Fig. 15, we present the signals generated through event-based models for phase locking to different reference

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(a) $\eta^{\mathrm{R}} = 0.4$

(b) $\eta^{\mathrm{R}} = 0.5$

(c) $\eta^{\mathrm{R}} = 0.51$

(d) $\eta^{\mathrm{R}} = 0.55$

(e) $\eta^{\mathrm{R}} = 0.8$

(f) $\eta^{\mathrm{R}} = 0.9$

(g) $\eta^{\mathrm{R}} = 1.1$

(h) $\eta^{\mathrm{R}} = 1.2$

FIG. 14. Phase locking to different references for a VCO with $\eta_0 = 1$, $K = 1$, and a low-pass filter with $\lambda = 1$, under positive feedback. In each panel, the reference signal is presented in light blue and the output signal in dark blue. The phase detector signal is shown in green, and the control signal is shown in red, which is obtained by numerical integration of Eq. (2). The black dots in both panels represent the value of the control signal at the update time of the VCO. For each set of signals, we show the transition to the locked state for different references: (a) $\eta^{\mathrm{R}} = 0.4$. (b) $\eta^{\mathrm{R}} = 0.5$. (c) $\eta^{\mathrm{R}} = 0.51$. (d) $\eta^{\mathrm{R}} = 0.55$. (e) $\eta^{\mathrm{R}} = 0.8$. (f) $\eta^{\mathrm{R}} = 0.9$. (g) $\eta^{\mathrm{R}} = 1.1$. (h) $\eta^{\mathrm{R}} = 1.2$.
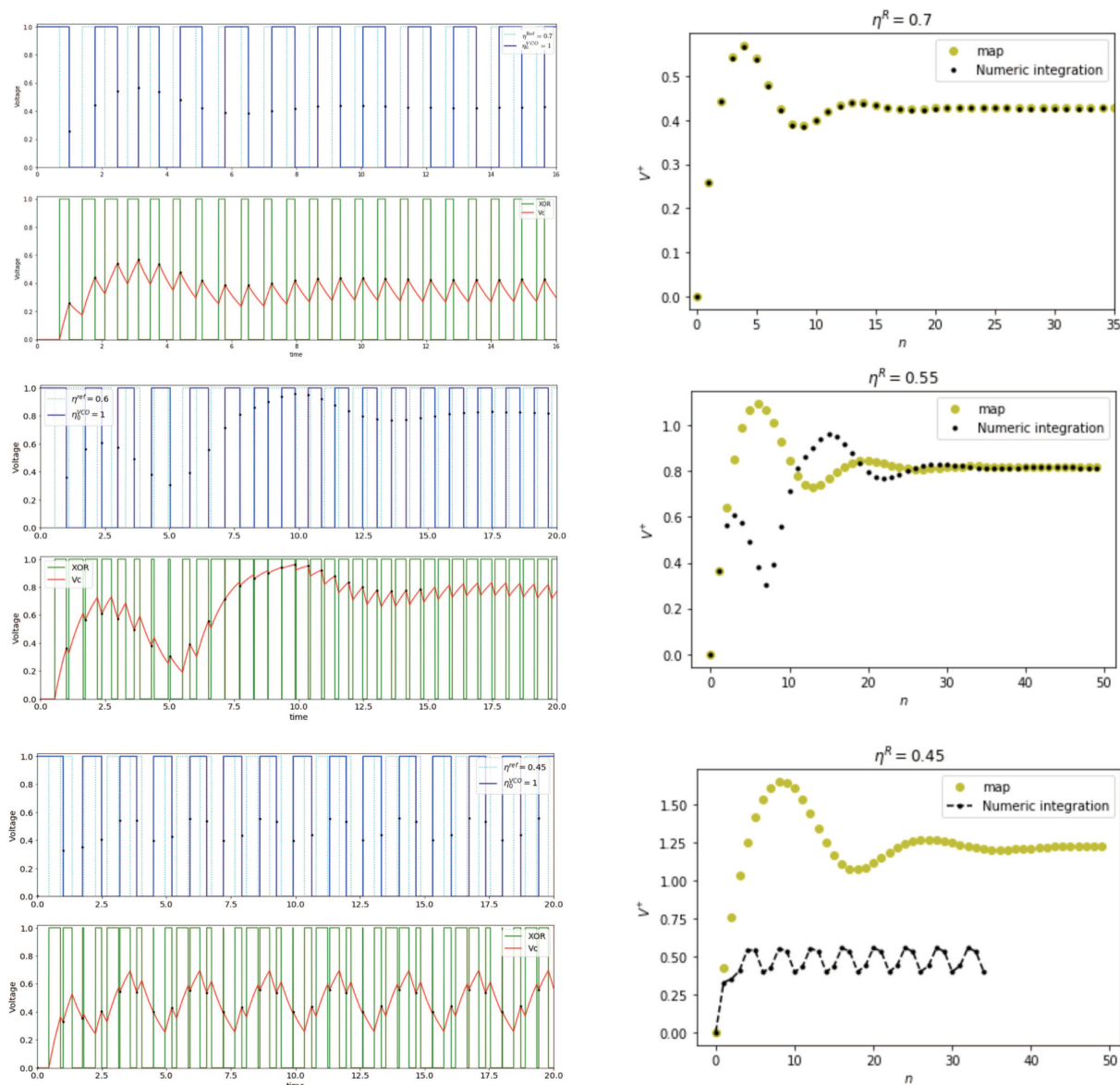
FIG. 15. In the left, we plot the numerical simulation of signals for entrainment of a VCO with $\eta_0 = 1$ to different reference oscillators with $\eta^R = 0.7, 0.6, 0.45$. In the right, we plot the sampled control at the event times with black dots and compare it to the results obtained by the $1:1$ discrete map. We observe that, for $\eta^R = 0.55$, the transient dynamic is different, although they converge at the steady state. For $\eta^R = 0.45$, they do not match.

signals. In the right column, we show the result of sampled control together with the discrete control obtained from $1:1$ discrete maps. While for $\eta^R = 0.7$ they match perfectly, when we decrease η^R to 0.55, they do not match in the transient dynamics but still catch up in the steady state. A further decrease in η^R leads to a complete mismatch, which indicates that the $1:1$ map does not hold in this parameter region.

REFERENCES

[1] F. Ellinger, *Radio Frequency Integrated Circuits and Technologies* (Springer Science & Business Media, 2008).
[2] G.-C. Hsieh and J. C. Hung, "Phase-locked loop techniques. A survey," IEEE Trans. Ind. Electron. **43**(6), 609–615 (1996).
[3] B. Razavi, *Design of Integrated Circuits for Optical Communications* (John Wiley & Sons, 2012).

20 January 2025 17:18:10

[4]B. Razavi, *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level* (Cambridge University Press, 2020).

[5]C.-C. Chung and C.-Y. Lee, "An all-digital phase-locked loop for high-speed clock generation," IEEE J. Solid-State Circuits **38**(2), 347–351 (2003).

[6]T.-Y. Hsu, B.-J. Shieh, and C.-Y. Lee, "An all-digital phase-locked loop (ADPLL)-based clock recovery circuit," IEEE J. Solid-State Circuits **34**(8), 1063–1073 (1999).

[7]I. Hwang, S. Lee, S. Lee, and S. Kim, "A digitally controlled phase-locked loop with fast locking scheme for clock synthesis application," in *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No. 00CH37056)* (IEEE, 2000), pp. 168–169.

[8]R. Bogdan Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, L. Meng-Chang, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phones," IEEE J. Solid-State Circuits **40**(12), 2469–2482 (2005).

[9]K. Gavaskar, R. Dhivya, and R. Dimple Dayana, "Low power CMOS design of phase locked loop for fastest frequency acquisition at various nanometer technologies," Wirel. Pers. Commun. **125**(3), 2239–2251 (2022).

[10]F. M. Gardner, *Phaselock Techniques* (John Wiley & Sons, 2005).

[11]A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," IEEE J. Solid-State Circuits **34**(6), 790–804 (1999).

[12]B. Razavi, "Jitter-power trade-offs in PLLs," IEEE Trans. Circuits Syst. I: Regul. Pap. **68**(4), 1381–1387 (2021).

[13]C.-S. Yen, "Phase-locked sampling instruments," IEEE Trans. Instrum. Meas. (1/2), 64–68 (1965).

[14]S. Ameli, L. Wetzel, and F. Julicher, "Event-based model for digital oscillators," in *Summer Solstice 2019 Conference on Discrete Models of Complex Systems* (Dresden, 2019), p. 24, https://solstice2019.loria.fr/wp-content/uploads/2019/07/Solstice-BookletAbstracts-v3.pdf

[15]K. J. Aström, "Event based control," in *Analysis and Design of Nonlinear Control Systems: In Honor of Alberto Isidori* (Springer, 2008), pp. 127–147.

[16]M. Miskowicz, *Event-Based Control and Signal Processing* (CRC Press, 2018).

[17]V. F. Kroupa, *Frequency Stability: Introduction and Applications* (John Wiley & Sons, 2012), Vol. 34.

[18]A. Pikovsky, M. Rosenblum, and J. Kurths, "Synchronization: A universal concept in nonlinear sciences," Self **2**, 3 (2001).

[19]R. Adler, "A study of locking phenomena in oscillators," Proc. IRE **34**(6), 351–357 (1946).

[20]P. Bhansali and J. Roychowdhury, "Gen-Adler: The generalized Adler's equation for injection locking analysis in oscillators," in *2009 Asia and South Pacific Design Automation Conference* (IEEE, 2009), pp. 522–527.

[21]C. Hoyer, L. Wetzel, D. Prousalis, J. Wagner, F. Jülicher, and F. Ellinger, "Stability analysis of mutually synchronized spatially distributed 24 GHz oscillators," in *2022 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)* (IEEE, 2022), pp. 1–6.

[22]X.-G. Li, H.-G. Zhang, A. Cela, and S.-I. Niculescu, "On the stability analysis of sampled-data control systems: A combined continuous-time and discrete-time method," in *2011 International Conference on Communications, Computing and Control Applications (CCCA)* (IEEE, 2011), pp. 1–6.

[23]S. Ameli, M. Karimian, and F. Shahbazi, "Time-delayed Kuramoto model in the Watts–Strogatz small-world networks," Chaos **31**(11), 113125 (2021).

[24]S. Ameli, F. Shahbazi, M. Karimian, and T. Malakoutikhah, "The effects of noise and time delay on the synchronization of the Kuramoto model in small-world networks," arXiv:1705.07875 (2017).

[25]A. Hajimiri, "Noise in phase-locked loops," in *2001 Southwest Symposium on Mixed-Signal Design (Cat. No. 01EX475)* (IEEE, 2001), pp. 1–6.

[26]A. Mehrotra, "Noise analysis of phase-locked loops," in *IEEE/ACM International Conference on Computer Aided Design. ICCAD-2000. IEEE/ACM Digest of Technical Papers (Cat. No. 00CH37140)* (IEEE, 2000), pp. 277–282.

[27]B. Razavi, *A General Theory of Phase Noise in Electrical Oscillators* (Wiley-IEEE Press, 2003).

[28]S. Ameli and K. Aghababaei Samani, "Low-dimensional behavior of generalized Kuramoto model," Nonlinear Dyn. **110**(3), 2781–2791 (2022).

[29]S. Ameli and K. Aghababaei Samani, "Two-step and explosive synchronization in frequency-weighted Kuramoto model," Phys. D: Nonlinear Phenom. 134349 (2024).

[30]N. Kuznetsov, A. Matveev, M. Yuldashev, and R. Yuldashev, "Nonlinear analysis of charge-pump phase-locked loop: The hold-in and pull-in ranges," IEEE Trans. Circuits Syst. I: Regul. Pap. **68**(10), 4049–4061 (2021).

[31]N. R. Sivaraaj and A. Majeed KK, "Comprehensive analysis of linear phase frequency detectors in phase-locked loops," AEU-Int. J. Electron. Commun. **178**, 155274 (2024).

[32]N. V. Kuznetsov, M. Y. Lobachev, M. V. Yuldashev, R. V. Yuldashev, E. V. Kudryashova, and O. A. Kuznetsova, "On the limit behavior of second-order analog phase-locked loops," IFAC-PapersOnLine **56**(2), 821–826 (2023).

[33]C. Hoyer, L. Wetzel, D. Prousalis, J. Wagner, F. Jülicher, and F. Ellinger, "Entrainment of mutually synchronized spatially distributed 24 GHz oscillators," IEEE Trans. Circuits Syst. I: Regul. Pap. **70**(7), 2665–2678 (2023).

[34]A. Pollakis, L. Wetzel, D. J. Jörg, W. Rave, G. Fettweis, and F. Jülicher, "Synchronization in networks of mutually delay-coupled phase-locked loops," New J. Phys. **16**(11), 113009 (2014).

[35]L. Wetzel, D. Prousalis, R. Fatima Riaz, C. Hoyer, N. Joram, J. Fritzsche, F. Ellinger, and F. Jülicher, "Network synchronization revisited: Time delays in mutually coupled oscillators," IEEE Access **10**, 80027–80045 (2022).

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