A Current-Mode SAR ADC for Memristor Readout in 28nm CMOS

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Computing in Memory (CIM) is a computing paradigm to overcome the von Neumann bottleneck of traditional computer architectures [1]. A possible implementation uses memristor crossbar arrays, which store information as resistance, to perform parallel vector-matrix multiplication (VMM). In this structure, digital to analog converters (DACs) provide input voltages to the crossbar rows where the output currents are then measured by analog to digital converters (ADCs). Therefore, both converter circuits play an important role when optimizing the speed and power consumption in the operation.

In this research, we propose a single-ended current-mode ADC, as shown in Fig. 1, which can directly measure the input current from the memristor array without the need for any transconductance amplifier (TIA), sampling-and-hold circuit, or even charge integration method that is often used for current measurement [2][3]. This ADC measures single-ended input and is implemented in pseudo-differential manner to enhance its robustness against noise and disturbance. In this ADC, the input current is first compared with half of the reference current provided by transistor M_5 for the most significant bit (MSB) conversion. Then, the subtracted current enters the differential structure formed by transistor $M_{6\text{-}9}$ where they then converted into voltage difference across the 350 Ω load resistance. Data conversion is then performed using an array of current-steering DAC that operate according to the successive-approximation register (SAR) algorithm. The bias for this ADC is implemented as cascoded current source and can be used for multiple ADC core circuits. Additionally, the dynamic range of the ADC can be tuned by simply changing the reference current I_{REF} biasing transistor $M_{0,1}$.

In this work, a 2x2 CIM array is implemented by using 28 nm CMOS technology. As shown in Fig.2, this chip has the size of 1.4 mm^2 and consists of the control circuit for memristor interface followed by two ADCs. A RISC-V processor is also implemented to control the circuit and direct access available through a JTAG programming interface. The ADC is designed to have dynamic range of 1.28 mA with 6 bit resolution and can work with speed up to 100 MSps while consuming less than 3 mW power from 0.9 V power supply. Each ADC occupies less than 0.005 mm^2 area and thus suitable to be implemented multiple times as column ADCs. These ADCs also have the capability of choosing the source of input either from memristor array or from external input to make the measurement and characterization process easier.

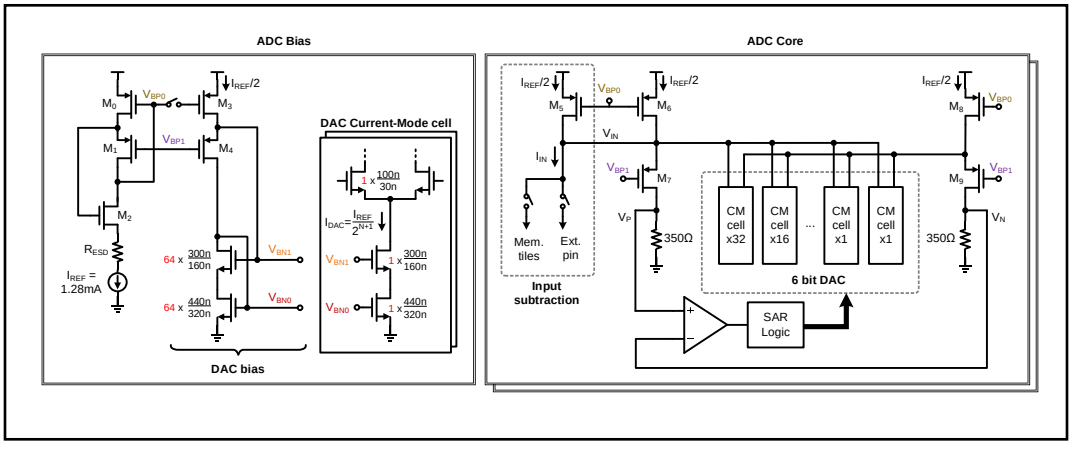

Figure 1. Proposed 6-bit current-mode SAR ADC circuit, consisting of the bias and the core ADC circuit

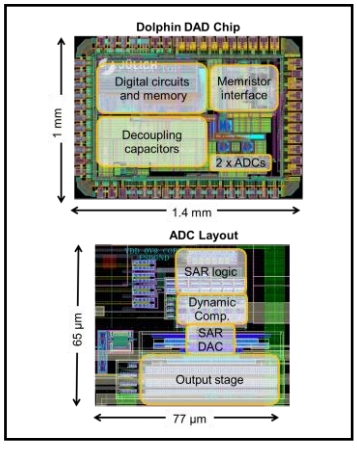

Figure 2. Chip layout

References

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