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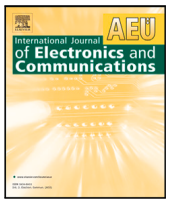

3.35V High Voltage Electroforming System in 28nm with 5.3mV ripple and 46 % efficiency for HfO_2-based Memristors

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ABSTRACT

This work demonstrates an on-chip high voltage (HV) generation, which is a critical requirement for memristor electroforming (EF) but is typically absent in smaller technology nodes. Key achievements of this study includes: (1) the development of a three-stage charge pump (CP) with an efficiency of 46.5%, delivering an EF voltage V_{EF} of 3.35 V with a compliance current I_{cc} of 184.9 µA from a 1.8 V supply voltage V_{dd}, without the need for HV-transistors in 28 nm CMOS process, and is based on preliminary work presented at the 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) in Volos, Greece (Shamookh et al., 2024); (2) the electrostatic discharge (ESD) protection, meeting the requirements of Class C3 CDM (±300 V) and Class 1C HBM (±1.5 kV) as per JEDEC standards (Semenov et al., 2008), employing three ESD diodes to handle positive (> 3.3 V) triggering ESD events and a single ESD diode for negative triggering ESD events above −1.87 V; and (3) the on-chip EF architecture for a 64 × 64 memristor crossbar array, as an active matrix (AM), through source and gate control of the compliance transistor. A ripple detection stage monitors voltage ripple at the three-stage CP bit-line (BL), halting gate pulses to the active compliance transistor and triggering EF for the next memristor in the left-to-right sequence. The proposed design is scalable to any $m \times n$ array and adaptable to various memristor applications, paving the way for fully integrated EF solutions in advanced technology nodes.

1. Introduction

Electroforming (EF) is a crucial process for the formation of memristors, pivotal components in neuromorphic systems, as it establishes a spectrum of resistive states through the growth of conductive filaments within oxide films [1]. The key EF parameters, namely EF voltage V_{EF} and current compliance I_{cc} varies oxygen vacancies in the memristor filament. A preliminary explanation of this behavior was presented at the 31st International Conference on Electronics, Circuits and Systems (ICECS) in Nancy, France [2].

Fig. 1 shows the correlation between EF time and V_{EF}, the memristor undergoes EF when I_{cc} begins to increase through it. The duration taken to reach the initial point of this increase is referred as EF time. Fig. 1(a) illustrates V_{EF}, while Fig. 1(b) displays the corresponding EF of the memristor in relation to EF time. For V_{EF} values of 3.3 V and 3.4 V, EF times are 315.37 m s and 308.95 m s, respectively, with I_{cc} at about 468 µA. A 0.1 V alteration in V_{EF} correlates with a 6.42 m s shift in EF time, highlighting the relationship between EF time and V_{EF} variation. The peak overshoot in I_{cc} arises from inherent memristor noise, but it can be mitigated [3].

Fig. 2 emphasizes the significance of I_{cc} in modulating the channel resistance in an EF process. It demonstrates that, for the same V_{EF}, the plug resistance R_{plug} and disc resistance R_{disc} [4] vary with two different I_{cc} values of 18.40 µA and 400 µA respectively. The R_{disc} starts decreasing, but slower than R_{plug}. After about 311 ms, both resistances decrease abruptly also leading to the abrupt I_{cc} increase (Fig. 1(b)). This sudden decrease of R_{plug} and R_{disc} is due to the positive feedback of Joule heating effect from thermal runaway [5]. Thus, achieving the desired channel resistance in an EF is facilitated by I_{cc} for memristors.

A memristor requires a wide range of voltages for EF, creating low resistance state (LRS), high resistance state (HRS), and for readout. EF characteristics studies [6,7] for various resistive switches, such as TiO_2, Al_2O_3, HfO_2, indicate V_{EF} requirement of 4.5 V, 4.0 V, and 3.3 V

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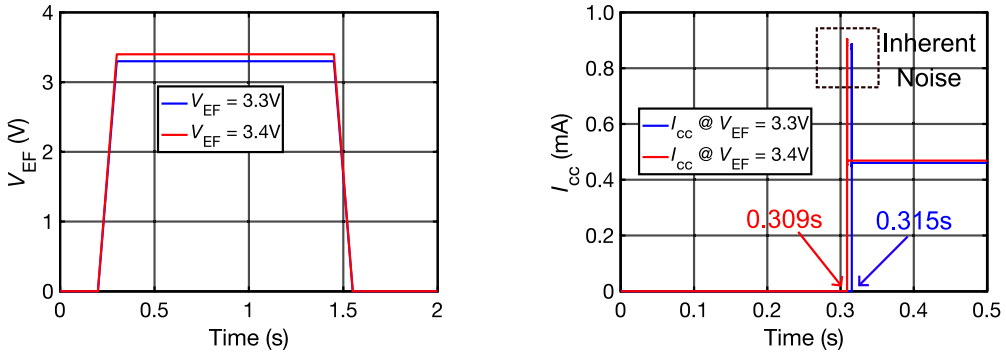

Fig. 1. (a) Electroforming (EF) voltage V_{EF} as a square pulse (b) and compliance current I_{cc} for memristor EF at 3.3 V & 3.4 V, respectively.

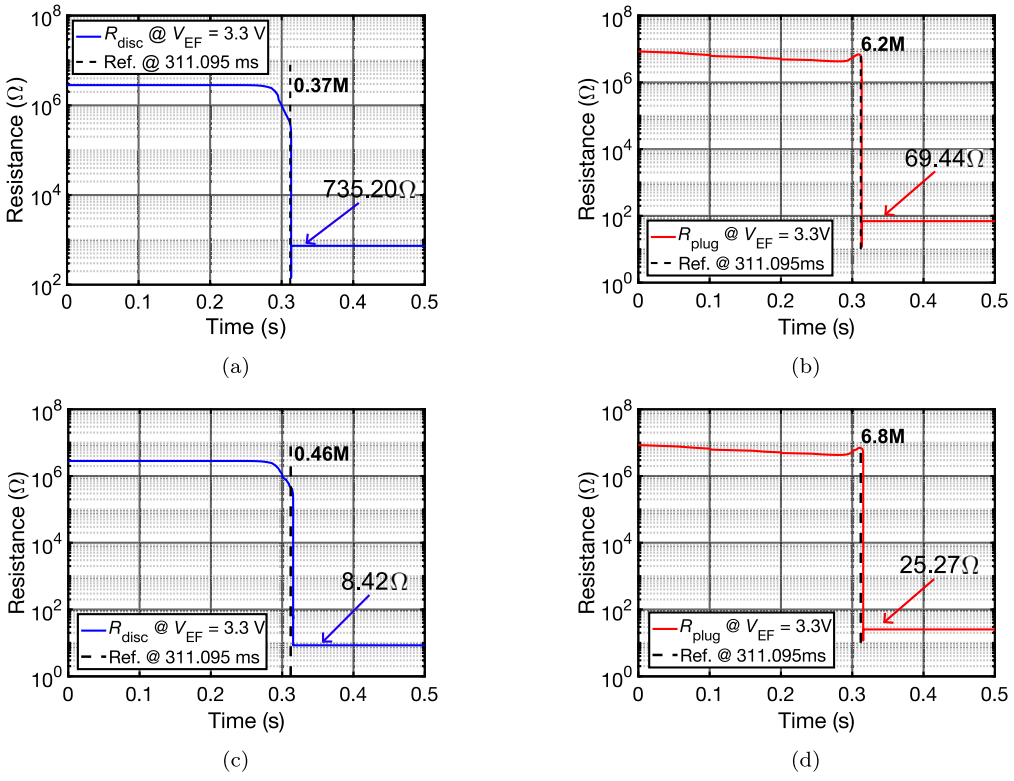

Fig. 2. Variation of disc resistance R_{disc} and plug resistance R_{disc} for V_{EF} = 3.3 V under different I_{cc}: (a) and (b) I_{cc} = 18.4 μA, and (c) and (d) I_{cc} = 400 μA.

respectively for various conditions. Additionally, a low-voltage resistive switch has been reported [8] for V_{EF} less than 1.5 V.

For a scalable CMOS and memristor co-integration in low technology nodes such as 28 nm, the typical input/output (IO) voltage V_{IO} = 1.8 V. Hence, for high voltage (HV) requirement, a HV generator is required. Another possibility could be to use an external HV source for the memristor-based cross-bar array IC. Again, the voltage for the chip will be higher than V_{IO}, which introduces the need for custom electrostatic discharge (ESD) pad-frame for the on-chip IC. A solution is to use the charge pump (CP) to generate higher voltage than V_{IO}.

The design of the CP becomes more challenging as the supply voltage V_{dd} in the new-technology nodes has kept reducing and the cascading of CP is needed to generate required voltages. Thus, a comparison between various CP-topologies is studied [9] to get an optimized solution. The cross-coupled charge pump (CC-CP) is chosen due to its linear scaling, efficiency and current consumption. All the CP circuits studied in literature include HV transistors for the over-voltage tolerance [10,11].

All the subsequent CP designs optimize one of three parameters — output current, output voltage, or output voltage ripple — while relying on HV-transistors. However, memristor EF requires all three factors simultaneously (Figs. 1 and 2). To address this, we propose a three-stage CP (Fig. 3), based on preliminary work presented at 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) in Volos, Greece [12]. The proposed design achieves high output current, high output voltage, and low ripple without HV-transistors (*i.e.,* breakdown voltage > 1.8 V) in a 28 nm CMOS process. Analytical pole analysis is employed in the CP design, aiming to bring the poles of different CP nodes closer together, reducing over-voltage stress while maintaining a balance between efficiency, output voltage ripple, I_{cc}, and capacitance. The design's robustness is validated through corner and Monte Carlo simulations.

Moreover, a custom ESD protection strategy was developed specifically for the three-stage CP due to its operation beyond the standard V_{dd} of 1.8 V. To handle ESD events, diode clamps were implemented at both

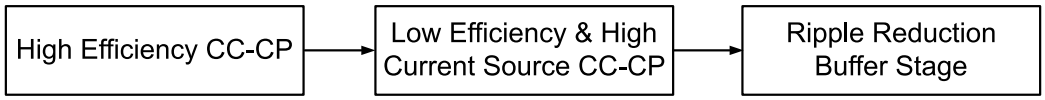

Fig. 3. Modified three-stage charge pump (CP) design for high output current and voltage with a reduced output voltage ripple.

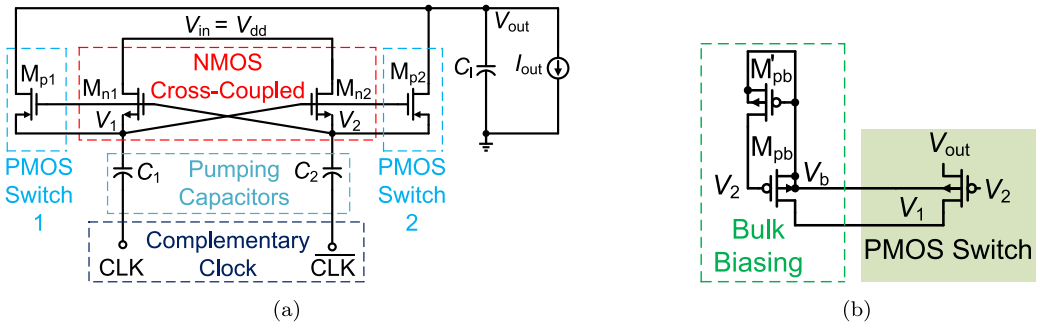

Fig. 4. (a) Schematic of cross-couple charge pump (CC-CP) [13]. (b) Additional auxiliary PMOS for the body bias without latch-up effect in CC-CP for PMOS switches [14].

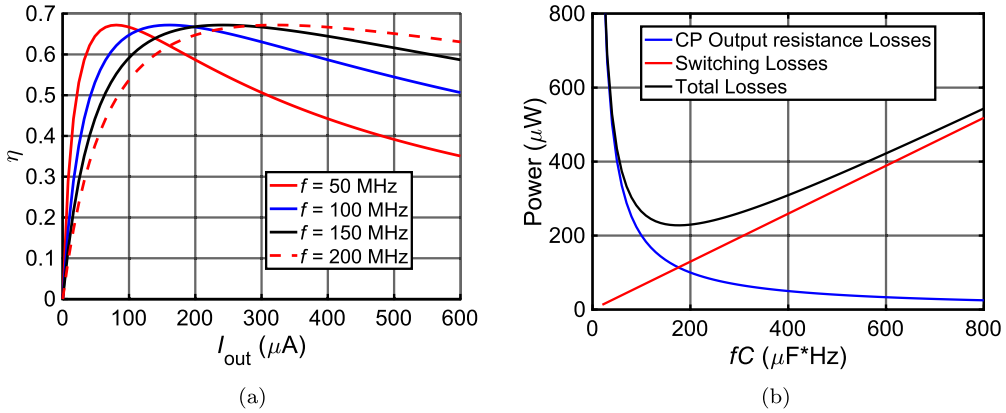

Fig. 5. (a) Plot of efficiency η, from (1) for extracting load current I_{out} and frequency f. (b) Summary of power losses for the unit-cell CC-CP for optimum fC.

the input and output nodes of the CP. A distributed ESD power clamp was designed to provide protection against both positive and negative ESD events, with a rapid triggering time constant of 40 ns. Since, the developed ESD protection is effective for both charge device model (CDM) and human body model (HBM) models, it is also expected to handle the less severe stresses associated with the machine model (MM) model.

The proposed on-chip EF architecture, designed for a 64 × 64 memristor crossbar, follows an active matrix (AM) approach to mitigate IR-drop, device-to-device variations and settling time issues. It is scalable to any $m \times n$ array, reinforcing its broad applicability.

The paper is structured as follows: Section 2 explains the optimum design strategy for the high-efficiency CC-CP with the design concept of the output voltage ripple reduction buffer stage. The goal of this stage is to minimize EF time variation, as V_{EF} has an exponential effect on EF time. [6]. In Section 3, the transient over-voltage stress issue is addressed along with the solution without HV-transistor. In Section 4, the modified CC-CP is presented with an over-voltage protection design strategy and results. Finally, Sections 5 & 6 explain the ESD compatibility of the proposed CP chip and the EF architecture for 64 × 64 memristor cross bar array using only one CP respectively.

2. Design strategy for the unit-cell Cross-Coupled Charge Pump (CC-CP)

A conventional 2-capacitor CP circuit using cross-coupled NMOS transistors is shown in Fig. 4(a) and operates with two clock phases CLK and $\overline{CLK}$, in two cycles. In the first cycle, switch M_{n1} allows pumping capacitor C_1 to charge to V_{dd}. In the second cycle, M_{n2} and M_{p1} activate, charging pumping capacitor C_2 to V_{dd} while C_1, previously charged, connects to the load, boosting output voltage V_{out} to $2V_{dd}$. This alternate clock phases ensure one capacitor charges while the other sources load current I_{out} each cycle. Additionally, Fig. 4(b) shows two PMOS devices M_{pb} and M'_{pb}, for body bias regulation of the PMOS switches M_{p1} and M_{p2} (Fig. 4(a)), helping maintain a stable threshold voltage and prevent latch-up [14]. This design supports positive pumping and a compact layout by isolating the body of each PMOS switch from others.

Fig. 5(a) illustrates the efficiency η of the unit-cell CC-CP as it varies with I_{out}, using (1) [15]. Here, C (where $C = C_1 = C_2$) represents the pumping capacitor, and α accounts for parasitic losses.

$$\eta = \frac{I_{out}V_{out}}{I_{out}V_{out} + 2fC\alpha V_{dd}^2 + \frac{I_{out}^2}{2fC}} \tag{1}$$

For an optimal performance in the desired LRS state, I_{out} should exceed 100 µA. To achieve maximum η at this I_{out}, a pumping frequency f of 100 MHz is selected, as shown in Fig. 5(a).

To determine the best value for C, the goal is to minimize power losses within a single CC-CP cell [15]. The total power loss depends on the product of frequency and capacitor size fC. If adjustments are needed later in the design, keeping fC constant will help maintain minimal power loss. Fig. 5(b) shows how power losses relate to fC,

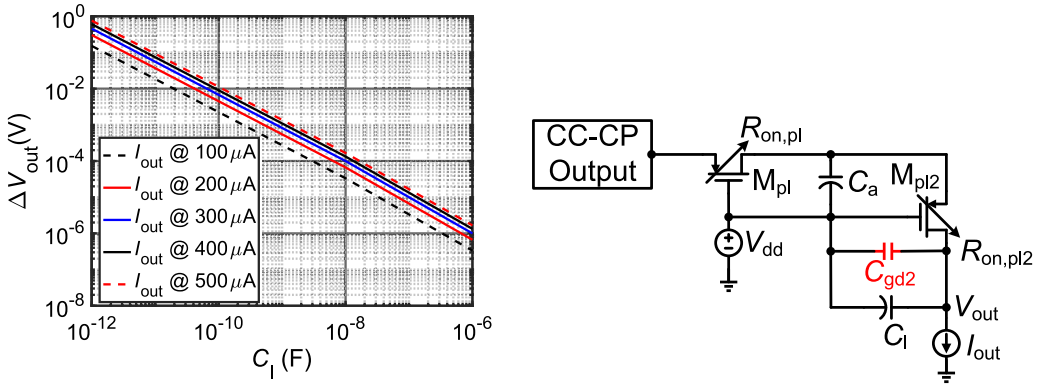

Fig. 6. (a) Optimum output ripple ΔV_{out} for various load capacitor. (b) LPF implementation concept and C_{gd} is the capacitance between drain and source.

Table 1
Finalized parameters for unit-cell cross-coupled charge pump (CC-CP).

Parameters	Values
Supply voltage (V_{dd})	1.8 V
Output voltage (V_{out})	3.3 V
Output current (I_{out})	>100 µA
Frequency (f)	100 MHz
Load capacitor (C_l)	Max. 10 pF

and with f (100 MHz) chosen for optimal η, C can be calculated as:

$$C = \frac{\min(fC)}{f}$$

This approach allows for efficient design while keeping power losses as low as possible.

The load capacitor C_l for the CC-CP is necessary to reduce the output voltage ripple ΔV_{out}, and in the presence of C_l given by:

$$\Delta V_{out} = \frac{I_{out}}{2f(C + C_l)} \tag{2}$$

Therefore, to meet the ΔV_{out} specifications without requiring a large C_l (Fig. 6(a)), a ripple reduction stage, as shown in Fig. 6(b), is implemented. The low-pass filter (LPF) is incorporated using a PMOS transistor operating in the triode region, as in Fig. 6(b). The ΔV_{out}, given by (3) in the s-domain, is controlled by the on-resistance $R_{on,pl}$ of M_{pl} and capacitor C_a, which together form the 1st order LPF. After optimization using first and second derivative tests to find the minimum capacitor values for minimizing ΔV_{out}, the capacitor values were set to $C_a = C_l = 2C$, with $C_l = 10$ pF. This selection helps achieve a compact, efficient design by effectively controlling ΔV_{out} without requiring excessive capacitor area. Capacitors C_a & C_l are referenced to V_{dd} rather ground (0 V) to keep the effective voltage across them within the breakdown voltage limits (1.8 V). Another benefit of this topology is that the V_{out} starts rising with an initial condition at V_{dd} instead of 0 V which assists in over-voltage stress reduction during transient state of CC-CP. The final parameters are listed in Table 1.

$$\Delta V_{out} = \frac{I_{out}}{2fsCC_l R_{on,pl}} \tag{3}$$

3. Over-voltage stress during transient unit-cell CC-CP operation

In 28 nm CMOS technology, the maximum breakdown voltage between any two nodes is limited to V_{IO} (1.8 V). In the absence of HV-transistor, reliability needs to be ensured during transient and steady state. Therefore, a mathematical analysis of CC-CP is done in order to inspect the stress during transient response. By suppressing over-voltage stress during transient state, the over-voltage does not exist in steady-state.

The CC-CP (Fig. 4(a)) is divided into two parts: in the first part, the equivalent circuit in Fig. 7(a) constitute CLK as $v(t)$, C_1, on-resistance R_{p3} of M_{p3} and C_l. When $v(t)$ (CLK) transitions from 0 – 1.8 V, the $v_1(t)$ node rises to $2V_{dd}$ (ideal) and correspondingly the $v_{out}(t)$. The differential equation is:

$$\frac{dv(t)}{dt} = \underbrace{\left(\frac{C_1 C_{par} R_{p3}}{C_1} + R_{p3} C_l\right)}_{a_0} \frac{d^2 v_{out}(t)}{dt^2} + \underbrace{\left(\frac{C_{par}}{C_1} + 1\right)\left(\frac{C_l}{C_1}\right)}_{a_1} \frac{dv_{out}(t)}{dt} \tag{4}$$

Using (4), the transfer function of the system can be derived:

$$\frac{V_{out}(s)}{V(s)} = \frac{s}{a_0 s^2 + a_1 s} \tag{5}$$

The above transfer function indicates a single pole at $\frac{-a_0}{a_1}$ and the node $v_1(t)$ in s-domain is:

$$V_1(s) = \frac{1}{sC_1} I(s) \tag{6}$$

where, $I(s)$ is current sourced by $v(t)$. Similarly from Fig. 7(b), the differential equation is expressed considering the on-resistance R_{n1} of switch M_{n1}, C_2 and C_{gd} is modeled with reference to ground as:

$$\frac{d\bar{v}(t)}{dt} = \underbrace{R_{n1}\left(C_2 + 2C_{gd}\right)}_{b_0} \frac{d^2 v_2(t)}{dt^2} + \frac{dv_2(t)}{dt} \tag{7}$$

and (8) in s-domain results one pole at $\frac{-1}{b_0}$.

$$\frac{V_2(s)}{\bar{V}(s)} = \frac{s}{b_0 s^2 + s} \tag{8}$$

Eq. (6) has a pole location at origin and makes the node $v_1(t)$ reach infinity, *i.e.*, $2V_{dd}$ in zero time, whereas node $v_2(t)$ charges to 1.8 V by a pole $\frac{-1}{b_0}$ of (8) from second part circuit (Fig. 7(b)). Therefore, there exists an over-voltage stress issue during transient phase.

Ideally, for the same charging and discharging nodes $-\frac{a_1}{a_0} = -\frac{1}{b_0}$. For reliability, the voltage difference ΔV between any two nodes should always be less than V_{dd}. This is achieved in two steps: First, C_l is pre-charged to V_{dd} initializing all the lines of the CC-CP to V_{dd} and when the node $v_1(t)$ charges to $2V_{dd}$ instantly, the ΔV is ensured to be less than V_{dd}. Time constant (τ_1 and τ_2) plot in Fig. 8(a) reveals that C_l effects both path differently. ΔV versus C_l in Fig. 8(b) shows safe C_l value for the reliable operation. Hence as a second step, C_l is selected as 2.2 pF resulting $\Delta V < 1.8$ V. This leads to an optimum value for the pumping capacitor C as $C_l/2$, implying $C = 1.1$ pF and

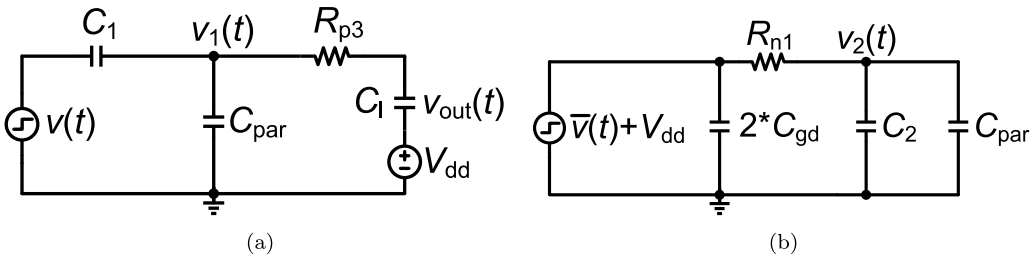

Fig. 7. (a) First part circuit, CLK is modeled as $v(t)$, V_{out} as $v_{out}(t)$ and V_1 as $v_1(t)$. (b) Second part circuit, $\overline{CLK}$ is modeled as $\bar{v}(t)$, V_2 as $v_2(t)$ for CC-CP in transient analysis.

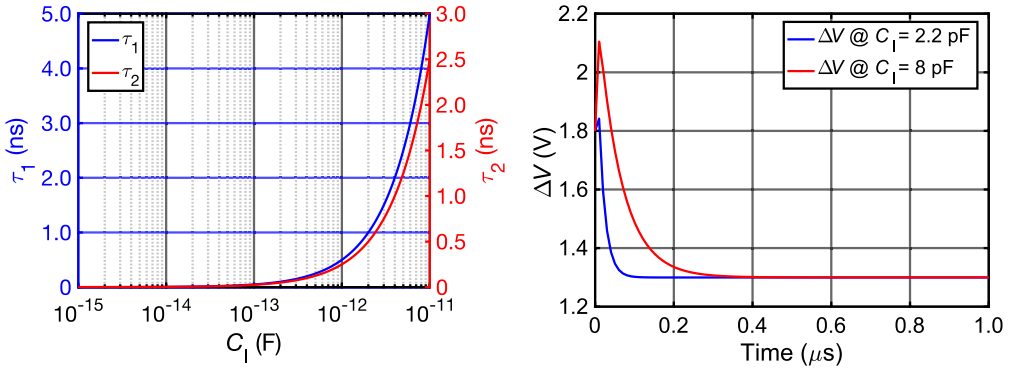

Fig. 8. (a) τ_1 is the time constant for $v_1(t)$ charging and τ_2 is the time constant for $v_2(t)$ charging (b) voltage difference for two nodes versus load capacitor C_l.

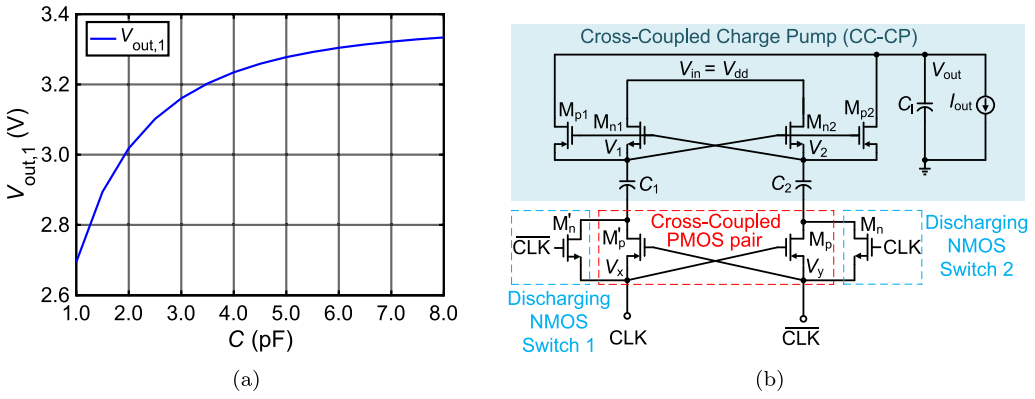

Fig. 9. (a) Stage 1 CP output voltage $V_{out,1}$ for pumping capacitor C sweep. (b) Stage 2 CP modified with cross-coupled PMOS pair (CC-PMOS) for over-voltage protection.

thereby optimizes power losses (Fig. 5(b)). However, the unit-cell CC-CP operates at the efficiency of 77.78% for minimum losses, this limits the CC-CP to 2.8 V rather 3.3 V, apparent from (1) which is the downside of using small C (Fig. 9(a)).

4. Reliable CC-CP design for voltage surge

From Fig. 9(a), $C = 8\,\text{pF}$ is needed to achieve the V_{out} specification of 3.3 V, however that leads to the $C_l = 16\,\text{pF}$. One can argue that $C = 8\,\text{pF}$ can be used to generate V_{out} of 3.3 V according to Fig. 9(a) but that is not an efficient solution because of over-voltage stress and the optimized C_l from first and second derivative test will become 16 pF and the overall area compared to the proposed design increases by 1.6 times without the over-voltage stress.

For pumping higher V_{out}, the second stage, as shown in Fig. 9(b), is cascaded with the original CC-CP architecture. The use of bigger capacitors again raises the over-voltage stress even in the presence of initial condition V_{dd} at the CP lines. Therefore, from the over-voltage stress analysis in previous section, if the pole of (6) is shifted from origin to $\frac{-1}{b_0}$, then the problem can be mitigated. This can be done with the pair of cross-coupled PMOS pair (CC-PMOS) in Fig. 9(b) and the equivalent transfer function with input CLK source $V(s)$ in s-domain

$$V_1(s) = \left(\frac{1}{1 + sR'_pC_1}\right)V(s) \tag{9}$$

Moreover, the CC-PMOS positive feedback can drive the bigger pumping capacitors C_1 & C_2 compared to inverter which requires huge $\frac{W}{L}$−ratio. N-channel MOSFET pairs are used alongside CC-PMOS pairs to discharge parasitic capacitance at the negative plate of the pumping capacitor, crucial for achieving higher voltages. Ideally, the discharging path time constant should be less than 5 ns (by $f = 100\,\text{MHz}$), adjusted with NMOS on-resistance and capacitor to manage over-voltage stress on C_1 & C_2.

Fig. 10 shows the voltage difference ΔV_1, between nodes V_1 and V_2 in the first stage CC-CP (Fig. 4), as well as the voltage difference ΔV_2 between nodes in the second stage of the modified CC-CP (Fig. 9(b)).

In the first stage CC-CP (Fig. 4), overvoltage is reduced by minimizing the charging time differences (or time constants) between the

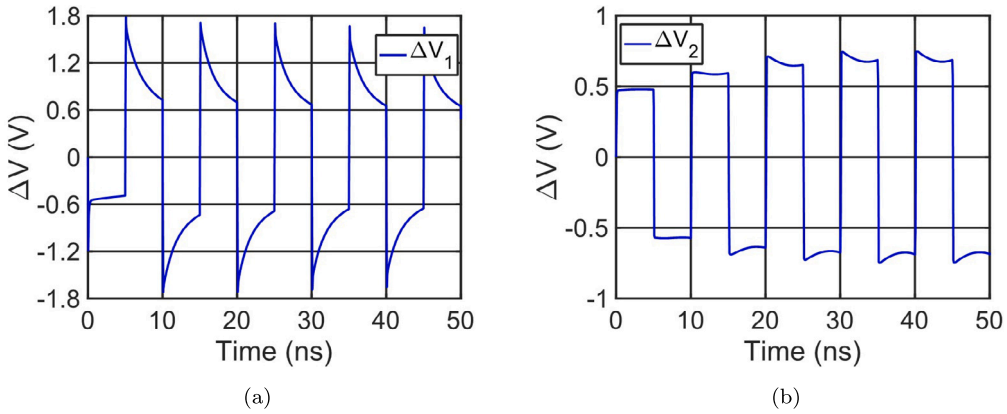

Fig. 10. (a) Stage 1 CC-CP voltage difference ΔV_1 between V_1 and V_2 (Fig. 4) (b) Stage 2 CP voltage difference ΔV_2 between V_1 and V_2 (Fig. 9(b)).

two alternating clock paths (CLK and $\overline{\text{CLK}}$). This is accomplished by positioning two poles closer together, allowing the C (1.1 pF) to operate optimally at 100 MHz. Analytical solutions were used to derive these results, helping to minimize discrepancies noted in Section 3.

As shown in Fig. 10(a), the transient voltage difference ΔV_1 between the nodes remains under 1.8 V. Over time, the peaks in ΔV_1 gradually decrease, eventually reaching a steady-state value of around 1.67 V. Ideally, ΔV_1 should be 1.8 V by alternating one node (V_1 or V_2) to pump the voltage to $2V_{dd}$ and the other (V_2 or V_1) to discharge to V_{dd} in each alternating clock cycle. However, due to approximately 70% efficiency (explained from (1)), thereby the node V_1 and V_2 are limited to 3.32 V and 1.16 V respectively, alternating between these levels with each clock cycle. Hence, minor variations around 130 mV (1.8 − 1.67) indicate the presence of parasitics (α in (1)) on the CC-CP lines, forming a capacitive divider that constrains the final steady-state ΔV_1 to around 1.67 V. Moreover, the C_1 in stage 1 CC-CP (Fig. 4) is referenced to V_{dd} rather than 0 V, thereby limiting the voltage difference (1.0 V) across capacitor, less than the breakdown voltage of 2.7 V (otherwise $V_{out,1} \approx 2.8\,V > 2.7\,V$ from Fig. 9(a)) for the 50 nm fingers spacing. The capacitor breakdown voltage alternatively can be increased by increasing the fingers spacing, which will increase the area.

In the second stage of the CP (Fig. 9(b)), the voltage difference ΔV_2, between the nodes is minimized by using a CC-PMOS pair. This configuration shifts the pole of the clock input (CLK or $\overline{\text{CLK}}$) to the nodes (V_1 or V_2), closer to the pole location from the CC-NMOS configuration to V_2 or V_1, thus bringing the pole location closer for alternating paths.

This results in an *RC*-behavior, meaning that the nodes V_1 and V_2 charge to $V_{out,1} + V_{dd}$ following an *RC*-charging curve during high clock cycles. Therefore, initially, as shown in Fig. 10(b), the ΔV_2 is less than the subsequent transient cycle, for instance, about 500 mV at 5 ns, and increases to approximately 790 mV by 20 ns, finally settling to a steady-state value of 870 mV, thus this configuration effectively reduces ΔV_2 less than V_{dd} for the second stage CP. The ΔV_2 (870 mV), in the second stage CP is lower than the ΔV_1 (1.67 V) in the first stage CC-CP even the input voltage for the second stage is $V_{out,1}$, which is inherently higher than the voltage (V_{dd}) used in the first stage. This is achieved by designing the second stage CP as a lower efficiency pumping effect, but this trade-off allows for higher current (Fig. 5(a)), which is necessary for setting the lower SET-resistance of the memristor during the EF process.

In the second stage CP, the pumping capacitors, with a finger spacing of 50 nm, are protected from overvoltage by connecting the negative plate of the capacitor to an n-channel MOSFET, which is placed in parallel with the CC-PMOS pair (Fig. 9(b)). This configuration ensures that when the clock alternates, the n-channel MOSFETs control the discharge path of the negative plate of the pumping capacitor. As a result, the negative plate is discharged only to around 650 mV, preventing it from discharging fully to ground. This limits the voltage difference between the plates of the pumping capacitor to 1.75 V (2.4 V–0.65 V). Additionally, the voltage difference between the CC-PMOS pair and the n-channel MOSFETs remains lower than V_{dd}, ensuring the second stage CP operation within safe voltage limits.

Table 2
Results for 200 samples in Monte-Carlo simulation corner.

	Mean	Standard deviation (σ)	Specification
V_{out} [V]	3.37	±1.72 m	>3.30
I_{out} [μA]	184.9	±0.34	>100
ΔV_{out} [mV]	5.31	±0.05	< 10

Table 3
Performance summary of the proposed design and comparison with published works.

	[10]	[11]	[16]	This work
Process	180 nm BCD[a]	180 nm CMOS	65 nm CMOS	28 nm CMOS
Pump capacitor	1.2 pF	15 pF	3.0 pF	1.2 pF, 4 pF
Supply voltage (V_{dd})	3.3 V	3.3 V	2.5 V	1.8 V
Max. Breakdown voltage	$>V_{dd}$	$>V_{dd}$	$>V_{dd}$	V_{dd}
Output voltage	19.6 V	−4.4 V	12.0 V	3.35 V
No. of stages	11	2	6	3
Output power	1560 μW	12 500 μW	2.5 mW[b]	598 μW
Efficiency	34 %	12 %	64 %	46.5 %
Ripple voltage	60 mV	≈3 mV	–	5.31 mV

[a] Bipolar-CMOS-DMOS.
[b] Includes 6-phase clock driver power.

The simulation results for the three-stage CP show an output voltage V_{out} of 3.35 V, with an output current I_{out} of approximately 185 μA and a voltage ripple ΔV_{out} of 5.31 mV at an operating frequency f of 100 MHz. Further, three stage CP design is simulated across all corners, presented at [2], under process, voltage, and temperature (PVT) variation. This includes a V_{dd} variation of ±10% and a temperature range from −25 °C to 80 °C. The minimum V_{out} was observed at slow-fast (sf) with V_{dd} = 1.62 V and −25 °C and corresponding deviation in V_{out} is 8.78%. This deviation can effect the EF time, and a system architecture is proposed in Section 6, independent of variations. Additionally, Monte Carlo simulation results for the three-stage CP, which account for statistical variations, are summarized in Table 2.

Comparing with other state-of-the-art integrated CP designs ([10, 11]: measured chips and [16]: post-layout simulation), Table 3 underscores the distinctive and innovative aspects of this application in 28 nm CMOS.

5. Proposed charge pump ESD protection method

ESD stress can occur in eight different modes depending on charge polarity and discharge paths: positive ESD voltage at the input/output (I/O) pad with ground V_{ss} (PS-mode), negative ESD voltage at the

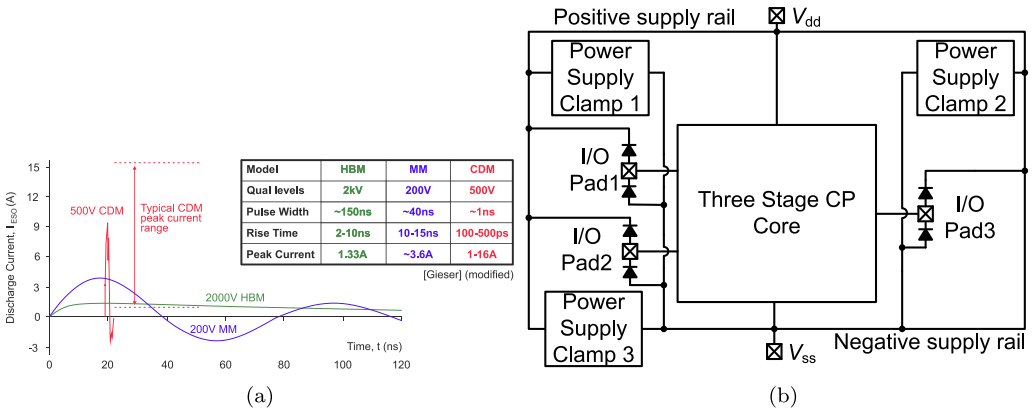

Fig. 11. (a) The current waveform for the different ESD models [17]. (b) Three stage charge pump ESD protection scheme.

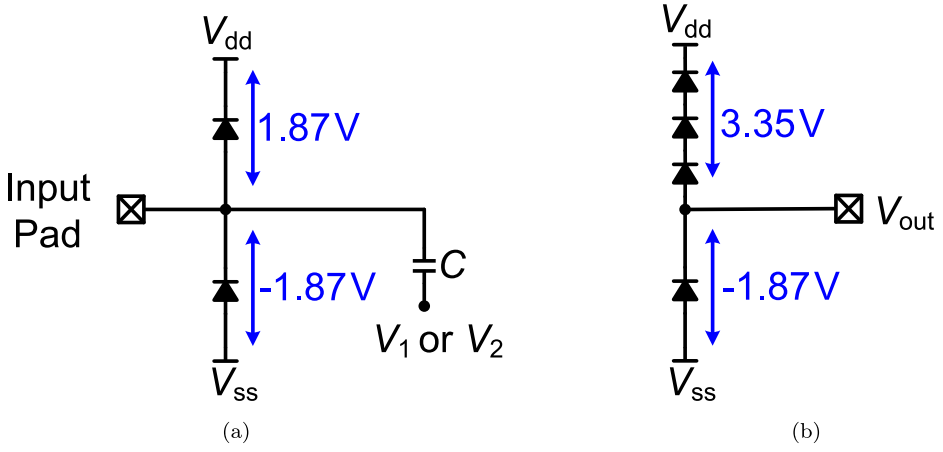

Fig. 12. (a) Diode string protecting input clock CLK and $\overline{\text{CLK}}$ with clamping voltage > 1.8 V. (b) Series diode string for the output ESD protection for clamping voltage > 3.3 V.

I/O pad with ground V_{ss} (NS-mode), positive ESD voltage at the I/O pad with ground V_{dd} (PD-mode), negative ESD voltage at the I/O pad with ground V_{dd} (ND-mode), positive ESD voltage at one I/O pad with respect to another (PIO-mode), negative ESD voltage at one I/O pad with respect to another (NIO-mode), positive ESD voltage at V_{dd} pad with ground V_{ss} pad (PDS-mode), and negative ESD voltage at V_{dd} pad with ground V_{ss} pad (NDS-mode) [17].

To illustrate the whole-chip ESD protection scheme, consider the realization of the PS-mode (a positive charge at an I/O pad with grounded V_{ss}) protection is activate by transferring the ESD charge to the positive supply rail using the forward-biased diode. Subsequently, ESD power supply clamp transfers the charge to V_{ss} and protects the circuit core. Fig. 11(b) shows, diodes are used as the protection component attached to the I/O pads. Multiple power supply clamps are distributed across the IC between the two power rails to reduce the parasitic resistance between the power supply clamp and the pin clamps [18].

When protecting the I/O pad, the output NMOS transistor is typically the most vulnerable component. Protecting the NMOS usually ensures the safety of other devices in the circuit. In the three-stage CP, the V_{out} is 3.35 V. Therefore, the ESD diode-clamp requires cascaded diodes to activate the clamp corresponding to the V_{out} of 3.35 V. This ensures that the CP operates optimally without ESD stress. Hence, the number of diodes m needed for the positive clamp is calculated accordingly.

$$V_{out} - mV_t = V_{dd} \tag{10}$$

where, V_t is the threshold voltage drop across the single diode. Hence, m is calculated for $V_t \approx 0.7$ V.

$$m = \frac{V_{out} - V_{dd}}{V_t} \approx 3 \tag{11}$$

It shows that to active the diode string during ESD stress in forward biasing, approximately 3 diodes (Fig. 12(b)) are required for the V_{out} = 3.35 V. This is valid for the positive ESD stress at the output pad (V_{out}).

For the negative ESD stress, the number of diode string m can be only 1 with respect to ground (0 V). This implies that to counter negative ESD stress 1 diode (Fig. 12(b)) are required without effecting the normal operation of the CP. Fig. 12 summarizes the scheme to protect the clock inputs and output of the proposed CP.

The power supply clamp is also designed for bringing the ESD charge to ground with a low resistive path during an ESD event. Fig. 13(a) shows the power supply clamp voltage under the positive 1.5 kV HBM stress, according to the military standard (method 3015.8) [19] equivalent circuit model, that was applied to V_{dd} node of the power supply clamp with grounded V_{ss} node. It can be seen in Fig. 13(a) the peak voltage of the V_{dd} node is 1.2 V also, the main transistor M_{ESD} in the power supply clamp sinks most of the ESD current I_{ESD}. Fig. 13(b) shows the response to the negative 1.5 kV HBM stress that was applied to V_{ss} node of the power supply clamp with grounded V_{dd} node. It can be seen in Fig. 13(b) that the power supply clamp limits the V_{dd} to −1.2 V, which means that the power supply clamp provides the protection for the circuit core against ±1.5 kV HBM stress.

Further, the power supply clamp design was also simulated for ±300 V CDM according to the JEDEC standard equivalent circuit [20].

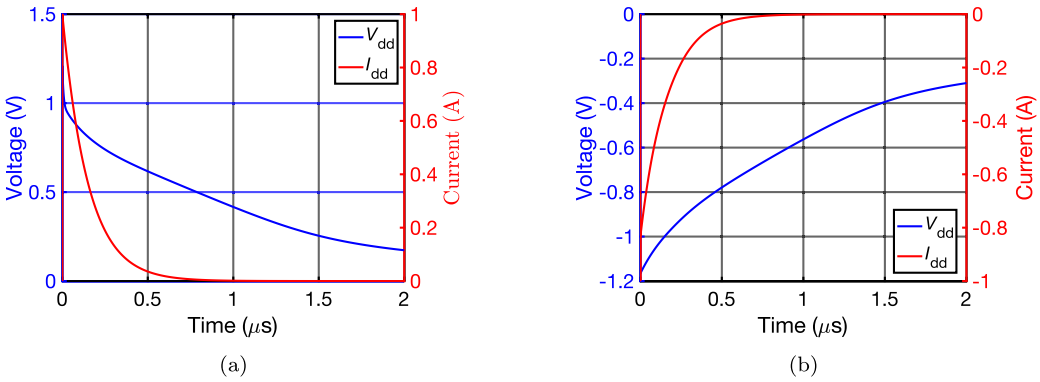

Fig. 13. (a) HBM stress = 1.5 kV (b) HBM stress = −1.5 kV.

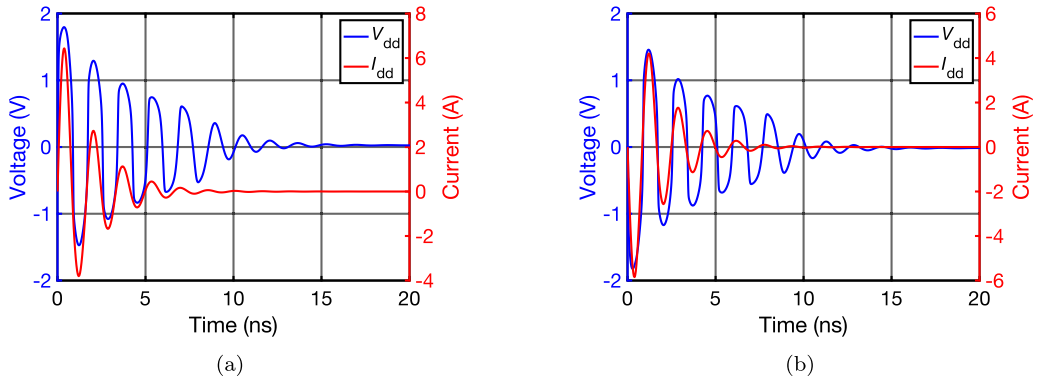

Fig. 14. (a) CDM stress = 300 V (b) CDM stress = −300 V.

Fig. 14(a) shows the design under the positive CDM stress that was applied to V_{dd} node with grounded V_{ss} node, while Fig. 14(b) shows the design under negative CDM stress that was applied to V_{ss} node with grounded V_{dd} node. The power supply clamp design can protect the circuit core against a ±300 V CDM stress as the peak voltage is limited to 1.78 V in the positive CDM stress and to −1.78 V in the negative CDM stress.

6. System architecture for memristor electroforming

The memristor cross-bar array shown in Fig. 15 operates with row and column drivers. The column drivers activate column WL1 to WLn, and during the activation time period T, the CP supply the EF voltage V_{EF} via the row drivers BL1 to BLn. To achieve this, each T is divided into time slots, allowing memristors EF.

By adjusting the strength of the CP signal, I_{cc} can be regulated using pulse width modulation (PWM) technique. This involves dividing one scan period into multiple sections. The number of subdivided slots determine the scale of I_{cc} based on the scan period and the EF time t_{form}. The EF system described above cannot work for a 64 × 64 cross-bar array because the small technology nodes do not have HV-transistors. However, this issue can be addressed by using the proposed CP. Additionally, multiple issues such as power consumption, IR-drop, and settling time arise when EF 64 × 64 (4096) memristors in a cross-bar array. Therefore, these issues are initially explained, and then an architecture for the EF is proposed.

6.1. Power consumption

The power consumption of the matrix-array can be categorized into the following parts: (a) dynamic power consumption of row and column line. (b) static power consumption during the EF phase.

The dynamic power consumption P_{dyn} is because of capacitor charging and discharging. It comprises of switching and short-circuit, therefore P_{dyn} for V_{EF} and I_{cc} is:

$$P_{dyn} = I_{cc} * V_{EF} \tag{12}$$

The parasitic capacitance C_{eff} exists during charging and discharging, using first-order approximation, C_{eff} is neglected compared to load capacitor C_l. Then P_{dyn} can be calculated for a change in EF voltage ΔV_{EF} in time period ΔT across C_l.

$$P_{dyn} = C_l \frac{\Delta V_{EF}}{\Delta T} * V_{EF} \tag{13}$$

Each memristor requires V_{EF} and I_{cc} sourced by the CP. Hence, the static power consumption P_{st} for the memristor array.

$$P_{st} = I_{cc} * V_{EF} * \text{NUM} \tag{14}$$

where, NUM represents total memristors in one row.

The total power consumption P_{total} of the matrix-array can be estimated by summation.

$$P_{total} = P_{dyn} + P_{st} \tag{15}$$

Eq. (15) indicates that when EF is conducted on multiple memristors simultaneously, total power consumption P_{total} will increase by a factor of NUM. Therefore, EF multiple memristors in any single row is a high power consumption P_{total} process.

6.2. Memristor cross-bar array IR-drop

IR-drop refers to the voltage drop that occurs across a conductor (wires) due to its inherent resistance when current flows through it. In the context of memristor EF, IR-drop can cause the actual voltage at different points in the matrix array to be lower than expected.

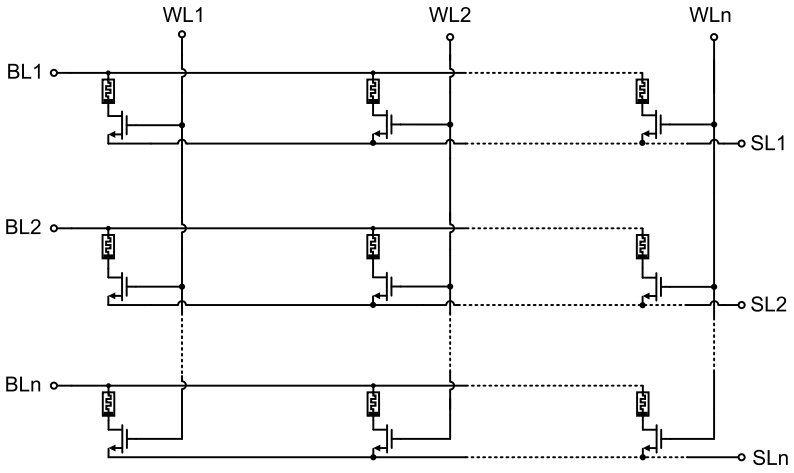

Fig. 15. 1T1R memristor crossbar array.

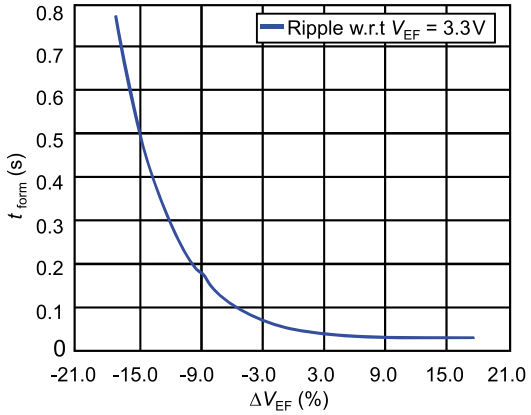

Fig. 16. EF time t_{form} as function of change in EF voltage ΔV_{EF} simulated using HfO_2 memristor.

This can affect the performance of the array, especially in densely packed memristor ICs, leading to an uneven voltage distribution ΔV_{EF} which will ultimately vary the t_{form} exponentially as shown in Fig. 16.

An equivalent circuit model is developed to analyze the IR-drop along power lines in a memristor cross-bar array for $m \times n$ dimensions. Fig. 17(a) shows the CP, buffer transistor M_p in the ripple reduction stage of CP, 1T1R structure, and the load capacitor C_l contribution to the IR-drop. The compliance current I_{cc} flowing through a memristor MR is controlled by the compliance transistor M_{cc}, supplied by the CP and C_l results in the IR-drop array-model in Fig. 17(b). The C_l in Fig. 17(b) is omitted from the equivalent model, which impacts the settling time, discussed in the subsequent section. Wire resistances R_v and R_h represent the resistances along the vertical and horizontal power line segments between adjacent memristors, while R_{ex} and R_{ev} denote the wire resistance between the edge memristor of the matrix-array and external biasing voltages in horizontal and vertical directions respectively. $I_{m,n}$ represents the compliance current, $V_{0,n}$ denotes the biasing voltage to turn-on the compliance transistor M_{cc} for each column and $V_{m,0}$ represents the EF voltage from the CP for each row.

To describe the behavior mathematically, Kirchhoff's current law (KCL) is applied at each corner node and within the corner nodes themselves.

$$I_{1,2} = \frac{V_{1,2} - V_{1,1}}{R_h} + \frac{V_{1,2} - V_{1,3}}{R_h} + \underbrace{\frac{V_{1,2} - V_{0,2}}{R_v} - C_{1,2}\frac{\Delta V_c}{\Delta t}}_{I_{g(1,2)}} \tag{16}$$

In the case of MOSFET, the gate resistance is usually very high ($\approx \infty$) and hence, the gate current $I_{g_{(m,n)}}$ of the MOSFET is negligible and hence is not considered for further mathematical analysis. Therefore (16) can be simplified in generic form.

$$I_{i,j} = -V_{i,j-1}\left(\frac{1}{R_h}\right) + V_{i,j}\left(\frac{2}{R_h}\right) - V_{i,j+1}\left(\frac{1}{R_h}\right) \tag{17}$$

where,

$i = 1, 2, \ldots, m$

$j = 1, 2, \ldots, n-1$

Eq. (17) does not apply to the left-side edge (Fig. 17(b)) of the memristor matrix array, specifically when $i = 1, 2, \ldots, m$ and $j = 1$. The appropriate equation for this situation is derived.

$$I_{i,1} = -V_{i,j-1}\left(\frac{1}{R_{ex}}\right) + V_{i,j}\left(\frac{2}{R_h}\right) - V_{i,j+1}\left(\frac{1}{R_h}\right) \tag{18}$$

Using KCL at the corner node, where the memristors are at the right-side edge of the matrix, denoted by $i = 1, 2, \ldots, m$ and $j = n$. This leads to the derivation of.

$$I_{i,j} = \frac{V_{i,j} - V_{i,j-1}}{R_{ex}} = -V_{i,j-1}\left(\frac{1}{R_{ex}}\right) + V_{i,j}\left(\frac{1}{R_{ex}}\right) \tag{19}$$

Subsequently, all nodal equations are organized into matrix form.

$$\mathbf{V}\mathbf{R}^{-1} = \mathbf{I} \tag{20}$$

where,

$\mathbf{R}$ = matrix containing all resistances with an order $n \times m$

$\mathbf{V}$ = matrix containing all node voltages $V_{i,j}$ with an order $m \times n$

$\mathbf{I}$ = matrix containing the compliance currents $I_{i,j}$

$$\begin{bmatrix} V_{1,0} & V_{1,1} & V_{1,2} & \cdots & V_{1,n} \\ V_{2,0} & V_{2,1} & V_{2,2} & \cdots & V_{2,n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ V_{m,0} & V_{m,1} & V_{m,2} & \cdots & V_{m,n} \end{bmatrix} \begin{bmatrix} \frac{-1}{R_{ex}} & 0 & 0 & 0 & \cdots & 0 \\ \frac{2}{R_h} & \frac{-1}{R_h} & 0 & 0 & \cdots & 0 \\ \frac{-1}{R_h} & \frac{2}{R_h} & \frac{-1}{R_h} & \ddots & \ddots & \vdots \\ 0 & \frac{-1}{R_h} & \ddots & \ddots & 0 & 0 \\ \vdots & 0 & \ddots & \frac{2}{R_h} & \frac{-1}{R_h} & 0 \\ 0 & \vdots & \ddots & \frac{-1}{R_h} & \frac{2}{R_h} & 0 \\ 0 & 0 & \cdots & 0 & \frac{-1}{R_h} & \frac{-1}{R_{ex}} \\ 0 & 0 & \cdots & 0 & 0 & \frac{1}{R_{ex}} \end{bmatrix}^{-1}$$

$$= \begin{bmatrix} I_{1,1} & I_{1,2} & \cdots & I_{1,n} \\ I_{2,1} & I_{2,2} & \cdots & I_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ I_{m,1} & I_{m,2} & \cdots & I_{m,n} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_m \end{bmatrix}$$

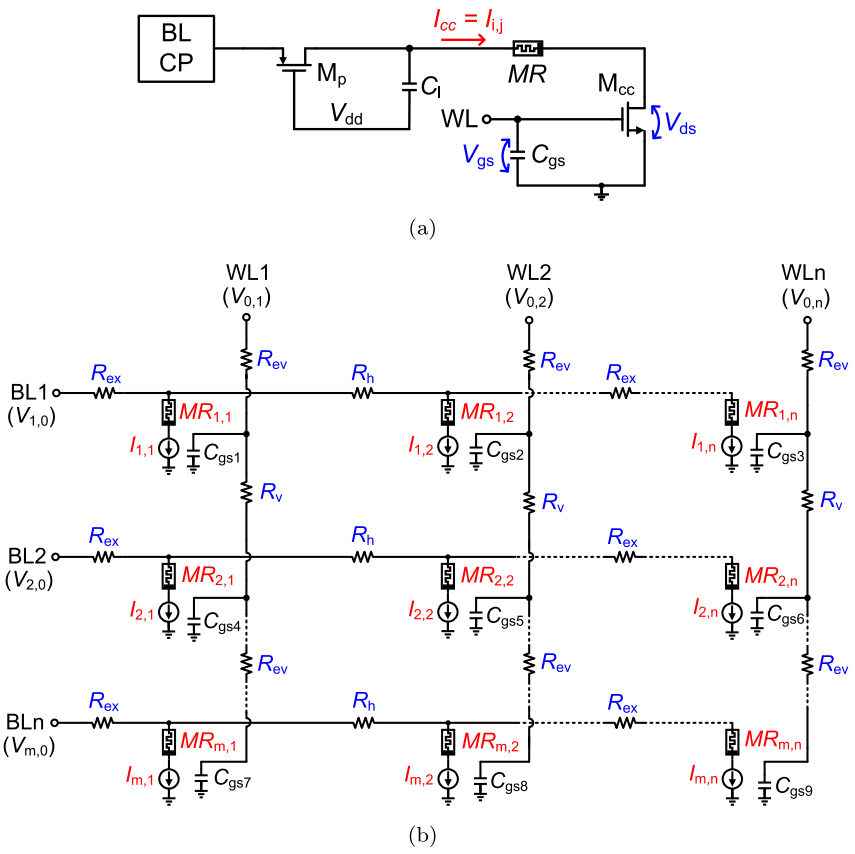

Fig. 17. (a) The equivalent circuit model to characterize the IR-drop along power lines in the memristor cross-bar array and (b) replica of the equivalent circuit model along the complete memristor cross-bar array. C_{gsm} represents the gate-to-source capacitance of the compliance transistor M_{cc} from left to right sequence.

The (20) matrix illustrates that the total I_{cc} required for EF along one row, denoted as I_1, is the sum of currents $I_{1,1} + I_{1,2} + \cdots + I_{1,n}$ in that row. The cumulative I_{cc} will lead to a voltage drop across wire and hence the t_{form} will varies from memristor-to-memristor in left-to-right sequence. For instance, if each memristor requires 180 μA for EF, considering a 2% IR-drop across wire resistance, the nth memristor in that row will face a voltage drop of 0.23 m V, correspondingly the t_{form} increases exponentially as a function of 0.23 m V (Fig. 16). Therefore, the t_{form} must be compensated for the IR-drop in order to electroform all the memristors correctly. The IR-drop due to wire resistance can be estimated using (20) matrix form for known I_{cc} and wire resistance to calculate **V**, but pre-determining the t_{form} will be a problem due to the device to device variations and design mismatches.

Similarly, the IR-drop along the column lines can cause the gate voltage V_{gs} of the compliance transistor to be lower than expected. As a result, the SET/RESET resistance of the memristor may vary, since V_{gs} directly influences the compliance current I_{cc}.

6.3. Memristor cross-bar array compliance current settling time

Settling time is the time required for a system to stabilize or reach its final state after a change in input. In memristor matrix array, settling time refers to the time taken for the I_{cc} to reach and stay within a certain error band around its final value during a EF process. This is critical in ensuring accurate performance of the matrix array, as delays or oscillations can affect the overall functionality and reliability.

The memristor EF process faces challenges related to the settling time of the I_{cc}, influenced by factors like the load capacitor C_l, significant parasitic capacitance C_{par} of the CP line and the gate–source capacitance C_{gs} of the compliance transistor M_{cc} shown in Fig. 18. Especially for lower currents, the settling time can be considerably prolonged. Therefore, a comprehensive investigation into the settling time of the current and the strategy to overcome the issue is presented. To gain insights into this issue, a simplified analytical model is introduced in Fig. 18.

During the memristor EF process, a CP is represented as a current source I_{in} in Fig. 18. Each memristor in the same row contributes a parasitic capacitor C_{par} to the EF line. The gate-to-drain capacitance C_{gd} is formed between the column (gate) line and I_{cc} line of the compliance transistor M_{cc} in each memristor and can be termed as a overlap between column and row lines. The overall impact of the parasitic series resistance R_{par} of the data line associated with each wire is negligible compared to the high series resistance of the memristor MR and hence R_{par} is not considered in the equivalent circuit.

The I_{cc} before the EF is expressed as a single pole transfer due to very high MR resistance

$$I_{cc}(s) = \frac{I_{in}(s)}{(1 + sC_l MR)} \tag{21}$$

Hence, in time domain the step input results as

$$I_{cc}(t) = I_{in}\left(1 - \exp\left(\frac{-t}{C_l MR}\right)\right) \tag{22}$$

The time constant τ is approximated for the single pole system due to very high MR resistance before EF as.

$$\tau \approx C_l MR \tag{23}$$

As evident, the settling time constant τ is directly proportional to C_l and MR before EF. Consequently, achieving the low SET resistance becomes challenging due to extended settling times. The analysis suggests that settling time primarily relies on the dimensions of the compliance transistor M_{cc}, and therefore C_{gs} will increase for the increase in the compliance transistor M_{cc} width W. Additionally, settling time is influenced by the CP input current I_{in}. These factors are contingent on

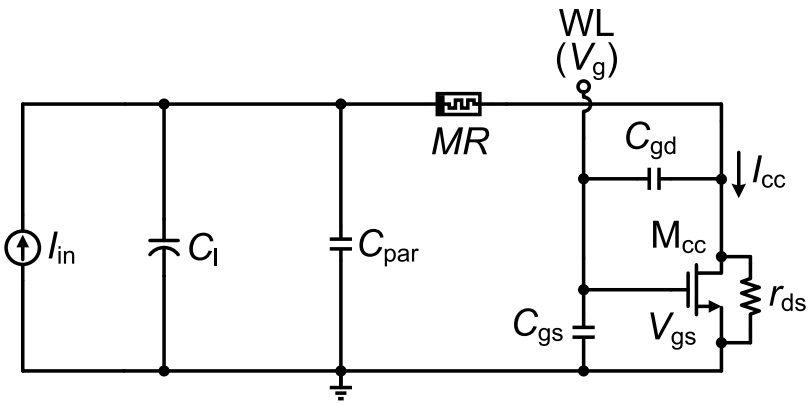

Fig. 18. Analytical model during memristor EF. CP is modeled as a current source I_{in} and C_{gd} is modeled in C_{par}.

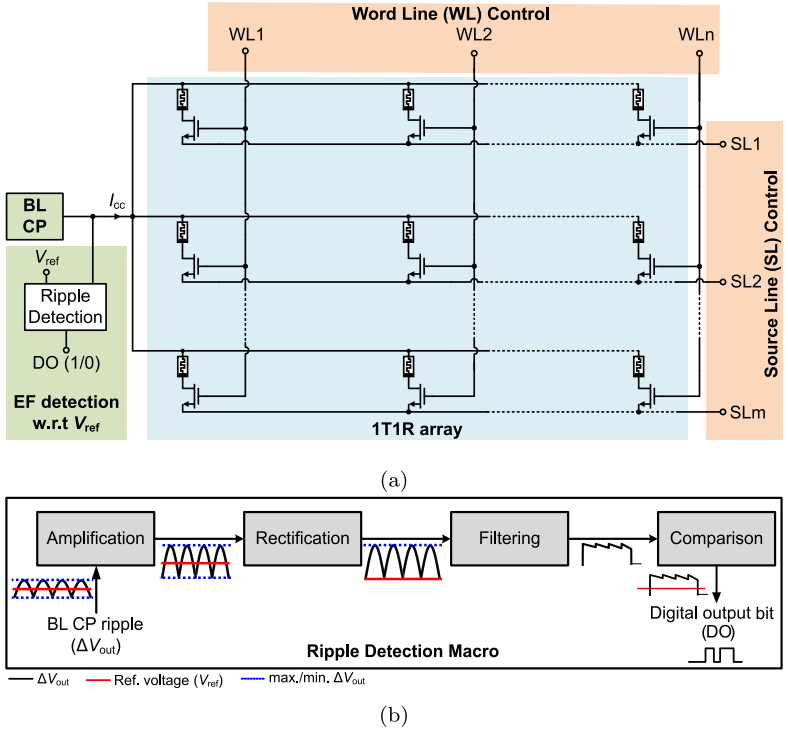

Fig. 19. (a) Proposed memristor cross-bar array EF architecture (b) Block diagram of ripple detection macro which compares the ripple at BL CP with the reference voltage V_{ref}.

the parameters of memristor EF, including SET/RESET resistance, V_{EF}, and t_{form} because the minimum necessary current is dictated by the required SET/RESET resistance.

The compliance transistor M_{cc} operates in the saturation region, where the I_{cc} is given by $I_{cc} = \frac{\beta}{2}(V_{gs} - V_{th})^2 < I_{in}$. Here, β describes the behavior of a MOSFET with respect to width over length ratio. Therefore, the minimum time duration t of the clock pulse for any memristor experiencing the maximum IR-drop is approximated as

$$t = \left| C_1 MR \ln\left(1 - \frac{\frac{\beta}{2}(V_{gs} - V_{th})^2}{I_{in}}\right) + t(\Delta V_{EF}) \right| \tag{24}$$

where, $t(\Delta V_{EF})$ represents the variation in EF time as a function of IR-drop as shown in Fig. 16. Eq. (24) calculates settling time specifically for the memristor experiencing the maximum IR-drop because the EF time for the memristor is prolonged. Therefore, to ensure that all memristors are electroformed properly, a t is determined based on the worst-case scenario IR-drop among the memristors. This approach guarantees that all memristors receive sufficient EF time despite variations in IR-drop across the array.

The device-to-device variations of the memristor and design mismatches have not been modeled in the analytical analysis, and these factors could have a significant impact on the on-chip EF process. To address this, a new EF architecture has been proposed in the next section. Unlike the pre-determined results, the new design utilizes an adaptive system to better account for these variations and ensure more reliable performance.

7. Proposed on-chip system architecture for memristor electroforming

To address challenges such as power consumption, IR-drop, and settling time, we propose the architecture illustrated in Fig. 19(a). This setup utilizes an AM array, which enables precise, individual addressing of each memristor during the EF process by coordinating the word line (WL) and source line (SL) controls. This precise addressing allows control over which specific memristor receives the EF, leveraging the existing digital drivers already present in the crossbar array for MAC operations. Consequently, no additional area is required beyond a CP

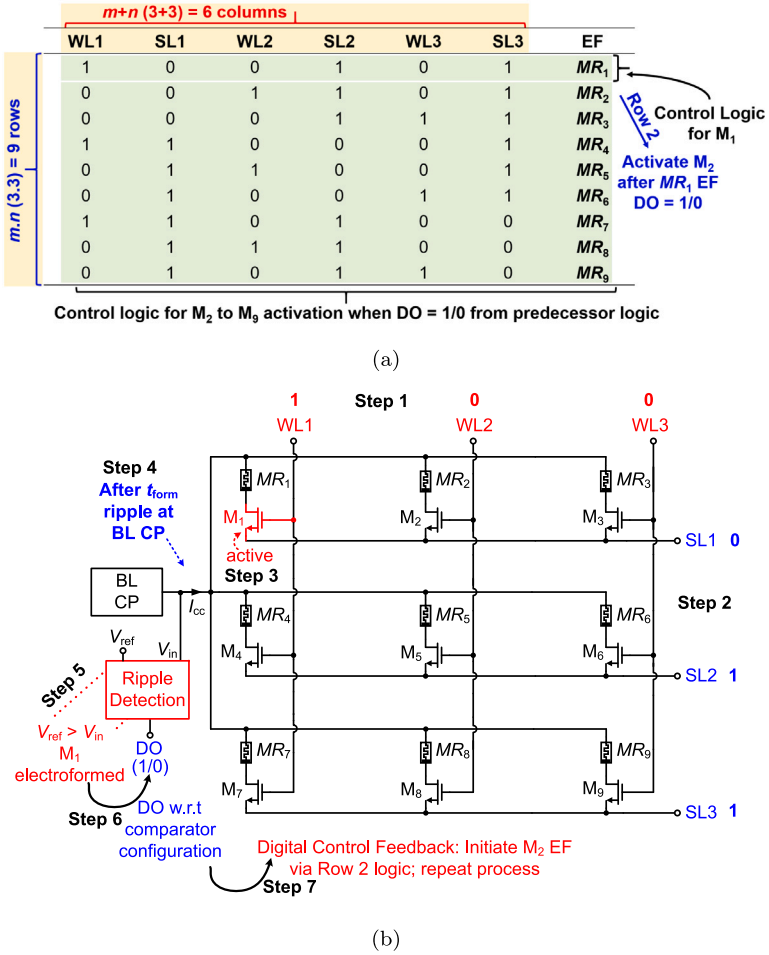

Fig. 20. (a) Truth table for WL1 to WL3 and SL1 to SL3 signals, detailing the control logic for each compliance transistor for achieving the AM array. (b) Detailed sequence of the EF process for a 3 × 3 crossbar array, explained in seven steps (step 1 through 7).

and a ripple detection macro, which utilizes the inherent voltage ripple for the detection of EF process for each addressed memristor before progressing to the adjacent in the right direction sequence.

In our proposed architecture shown in Fig. 19(a), WL controls the gate, and SL controls the source of the NMOS compliance transistor. To activate this transistor, the gate voltage must be high while the source voltage remains low. If these conditions are reversed, or if both gate and source voltages are high, the gate–source voltage V_{gs} will be 0 V or < 0 V, which falls below the threshold voltage V_{th} for the 28 nm technology node, preventing the transistor from activating.

This approach allows us to create a logic truth table for an $m \times n$ array, where the table's structure reflects the configuration of the array. In this table, the number of columns corresponds to the sum of the rows and columns $(m + n)$, and the number of rows represents the product of rows and columns $(m \cdot n)$. This setup provides a systematic method for reliably addressing each specific memristor within the array. The logic table can be generated by controlling the WL and SL. To activate a specific WL, we set it to high while simultaneously bringing the corresponding SL low. All other WLs and SLs are kept to low and high respectively. This configuration ensures that only one memristor cell is activated in any row and column, while all other memristor cells in the array remain in the off-mode.

When the desired compliance transistor is activated, the CP supplies the V_{EF} and the I_{cc}. These parameters are crucial for determining the memristor's t_{form} and its SET/RESET resistance after the EF process. I_{cc} can be controlled by the gate voltage V_g of the compliance transistor based on the required memristor SET/RESET resistances after the EF.

Once the EF process for the addressed memristor is completed, the bit-line (BL) CP (Fig. 19(a)) generates an output voltage ripple due to the flow of I_{cc}. This ripple is detected by the ripple detection macro, shown in Fig. 19(b), which first converts the peak-to-peak ripple into a DC voltage through full-wave rectification. The rectified voltage is then compared to a reference voltage V_{ref} using either an inverting or non-inverting comparator. The output of the comparator produces a digital output bit (DO) of either 0 or 1, depending on the comparator's configuration. Based on the DO bit, and using the existing digital control circuitry, the EF process for the next memristor is initiated according to the corresponding logic defined in the truth table.

The EF process is illustrated graphically in Fig. 20 for a 3 × 3 memristor cross-bar array as one specific example. However, this concept can be easily extended to any $m \times n$ array configuration, demonstrating that the proposed architecture is scalable and adaptable to various sizes.

8. Conclusion

The research presented addresses a significant challenge in the integration of memristors within CIM architectures, particularly focusing on the EF process essential for HfO_2 memristor functionality. This work demonstrates a comprehensive approach to an on-chip HV generation, which is a critical requirement for memristor EF but is typically absent in smaller technology nodes. The innovative approach of eliminating overvoltage stress without using HV-transistors or multi-phase clocks not only reduces system costs but also enhances the efficiency and scalability of neuromorphic systems. A custom ESD protection strategy

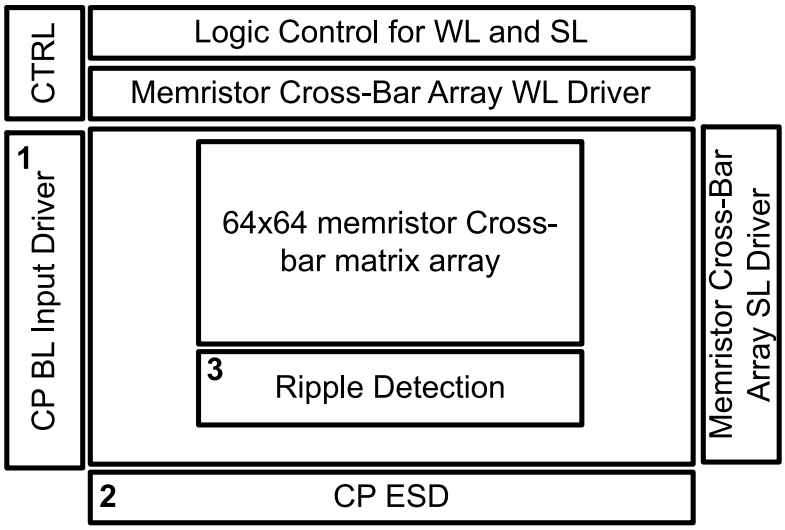

Fig. 21. Proposed memristor cross-bar array EF system using on-chip three-stage CP in 28 nm technology node.

was developed specifically for the three-stage CP due to its operation beyond the standard 1.8 V V_{dd}. To handle ESD events, diode clamps were implemented at both the input and output nodes of the CP.

The proposed EF architecture is designed for a 64 × 64 memristor crossbar array, where the EF process is conducted as an AM process and scalable to any $m \times n$ array. The on-chip EF system is summarized in Fig. 21. The next step in this research would involve the physical prototyping and experimental validation of the proposed system. This would include testing the functionality of the CP, EF system, and driver circuits in real-world scenarios to ensure their reliability and effectiveness in practical applications.

CRediT authorship contribution statement

Muhammad Shamookh: Writing – original draft, Investigation. **Arun Ashok:** Writing – review & editing, Supervision. **André Zambanini:** Writing – review & editing, Supervision. **Anton Geläschus:** Supervision. **Christian Grewing:** Supervision. **Andreas Bahr:** Supervision. **Stefan van Waasen:** Supervision.

Declaration of competing interest

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Data availability

No data was used for the research described in the article.

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