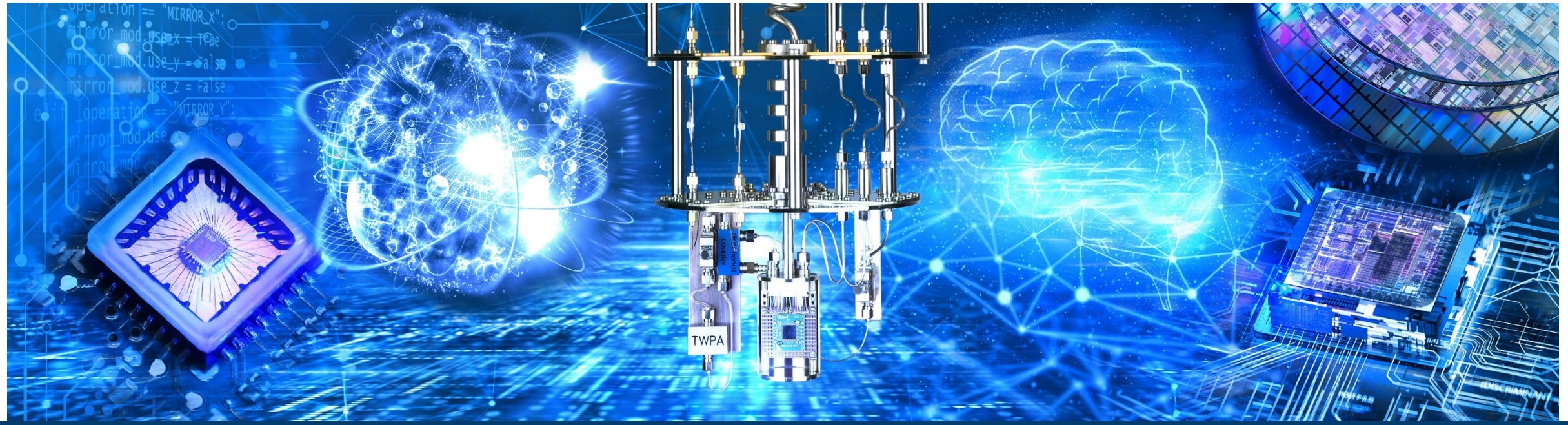

CRYOGENIC CMOS DESIGN FOR SCALABLE QUBIT CONTROL AND READOUT

2025-07-16 | DR.-ING. PATRICK VLIEX

Member of the Helmholtz Association

JÜLICH Forschungszentrum | Integrated Computing Architectures ICA

WHO AM I

Dr.-Ing. Patrick Vliex

- Studied **electrical engineering** at RWTH Aachen
  - Focus on micro- and nanoelectronics
- **IC Design** in 130 nm down to 22 nm
- PhD at Forschungszentrum Jülich (RWTH Aachen)
  - **Cryogenic electronics** for scalable solid-state QC
  - First iteration on a scalable bias voltage DAC
  - Later IC co-integrated with qubits at mK
- Currently scientific coordinator and project lead at ICA

Dr.-Ing. Patrick Vliex
p.vliex@fz-juelich.de

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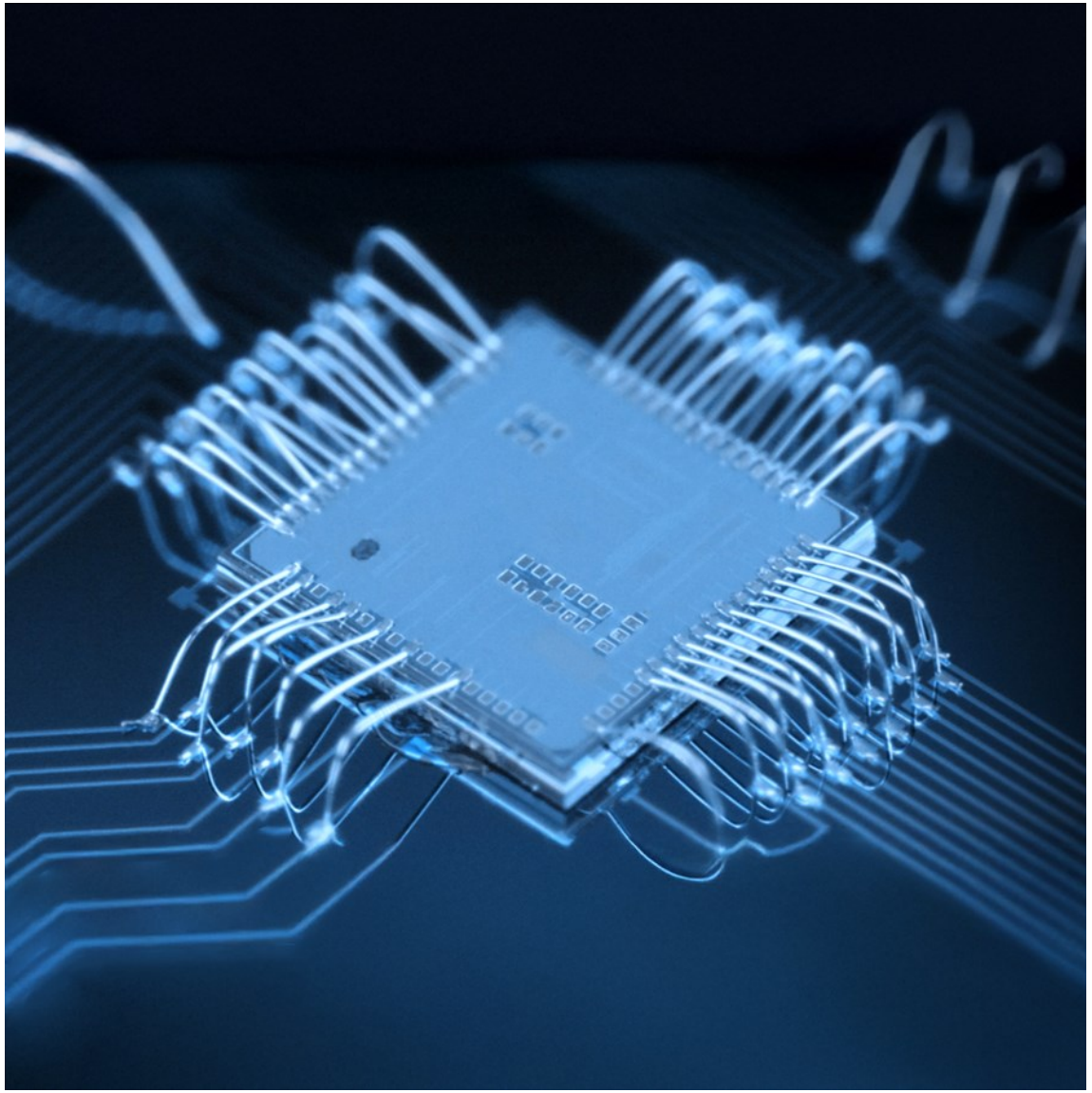
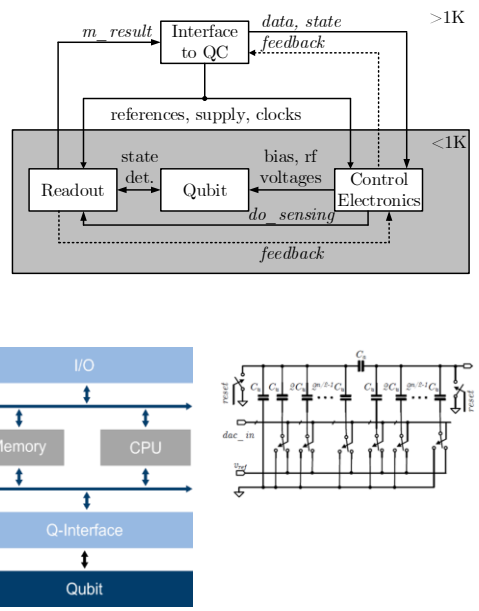
CONTENT

- **Designs in 65nm bulk and 22 nm FD-SOI**
  - Cryogenic measurement results
  - Lessons learned (what to watch out for)
- **Co-integration experiment with qubits at mK**
  - Thermal management
- **Other activities at ICA for QC:**
  - Cryogenic device measurement and modelling
  - Cryogenic photonic link (for superconducting qubits and cryo. electronics)

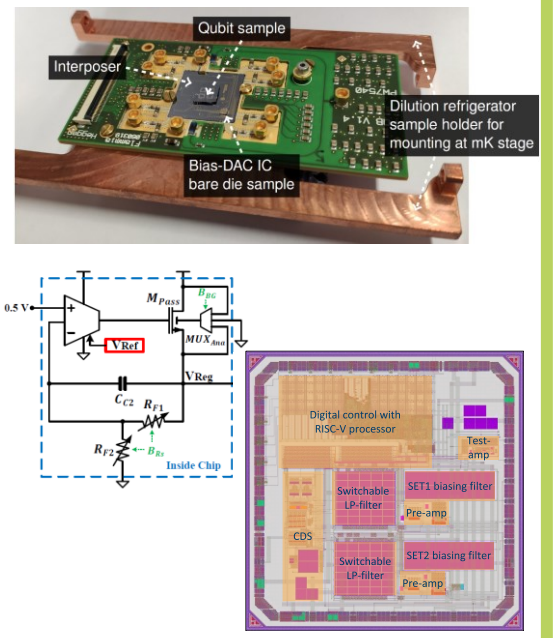


ICA – QC RESEARCH FIELDS

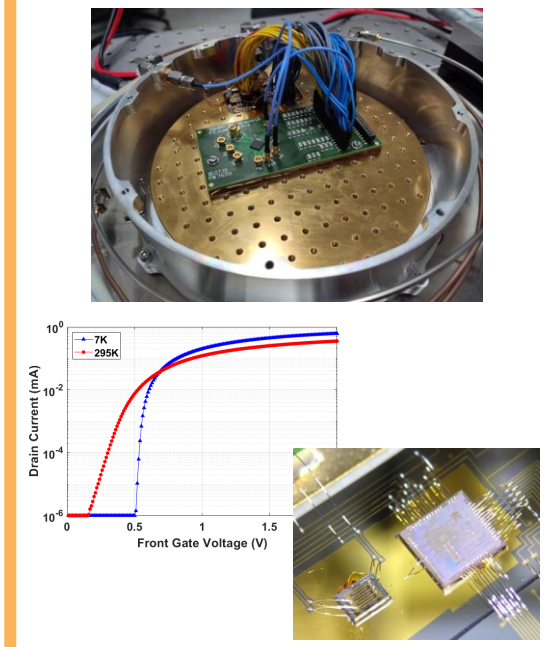
Covering the Whole Value Chain from Modeling/Specification up to System Integration



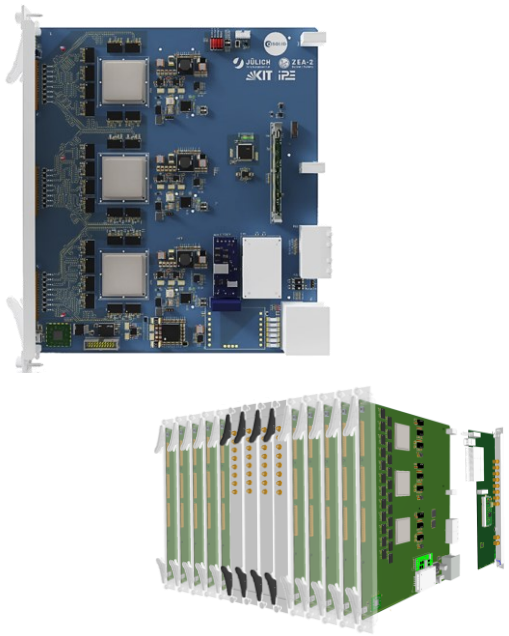
System Modeling
L. Geck



Cryogenic IC Design
P. Vliex

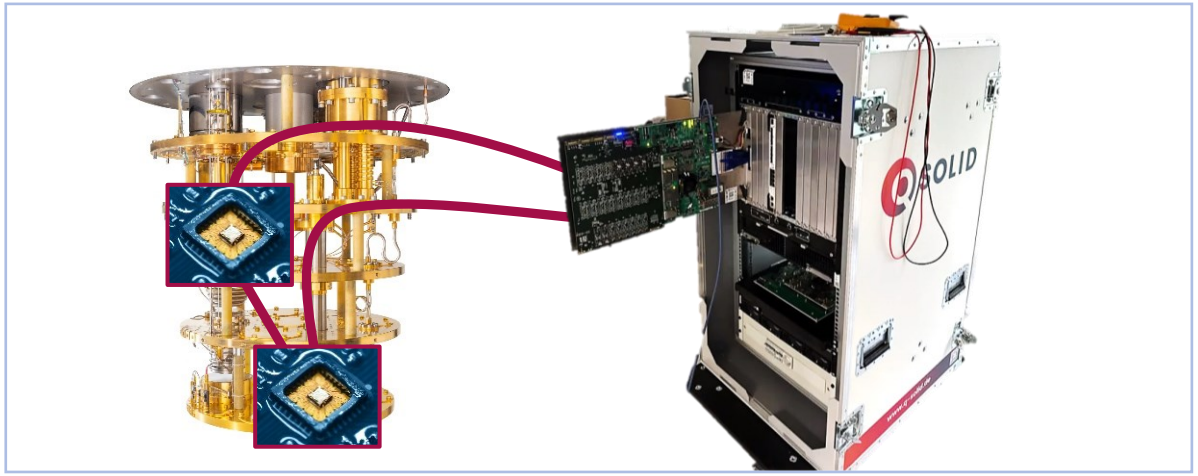


Cryogenic Measurement
C. Degenhardt

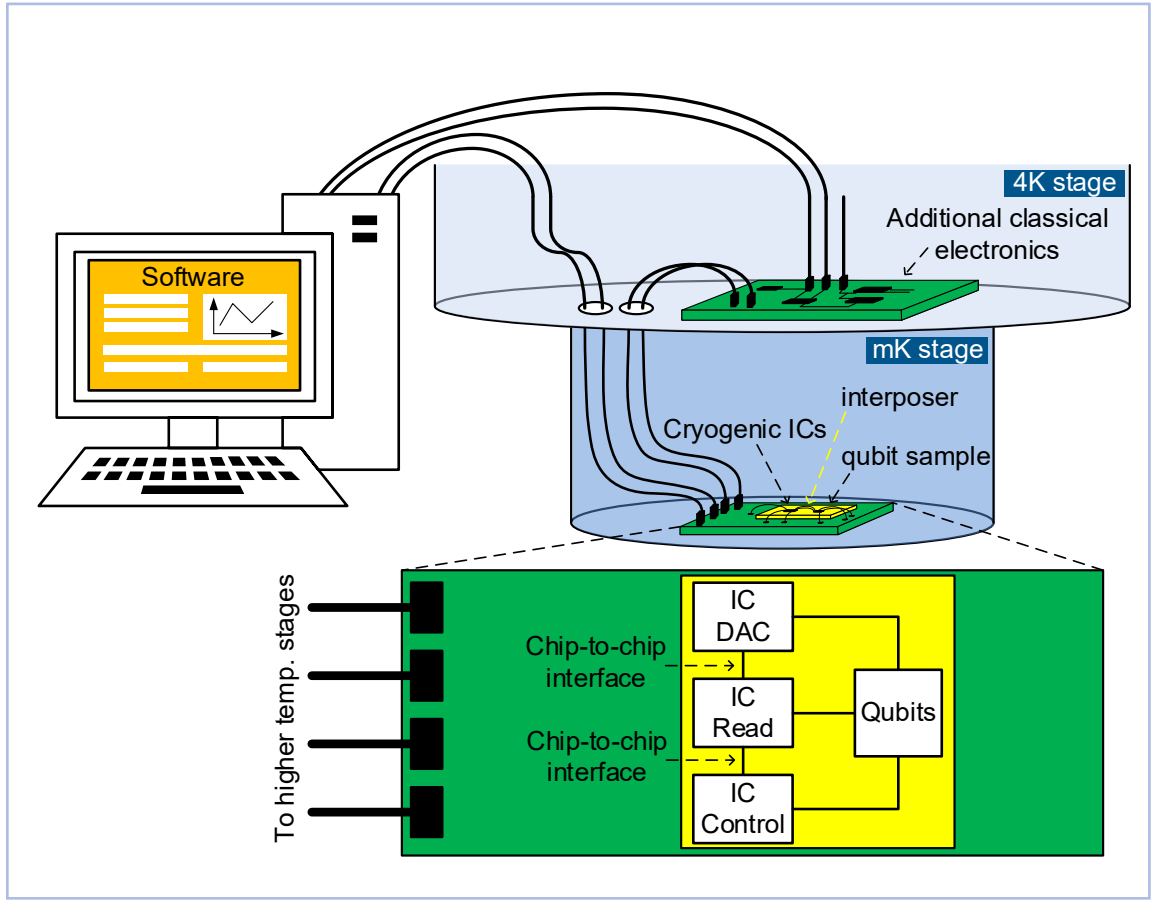


System Engineering
M. Schlösser

CRYOGENIC INTEGRATED CIRCUITS



- Move (parts) of classical control & readout electronics closer to the qubit
- Consequence → operate at cryogenic temperature
- Cryogenic CMOS enables high-integration
  - Comply to ultra strict cooling power budget
- Qubits are evolving quickly → modular IC framework



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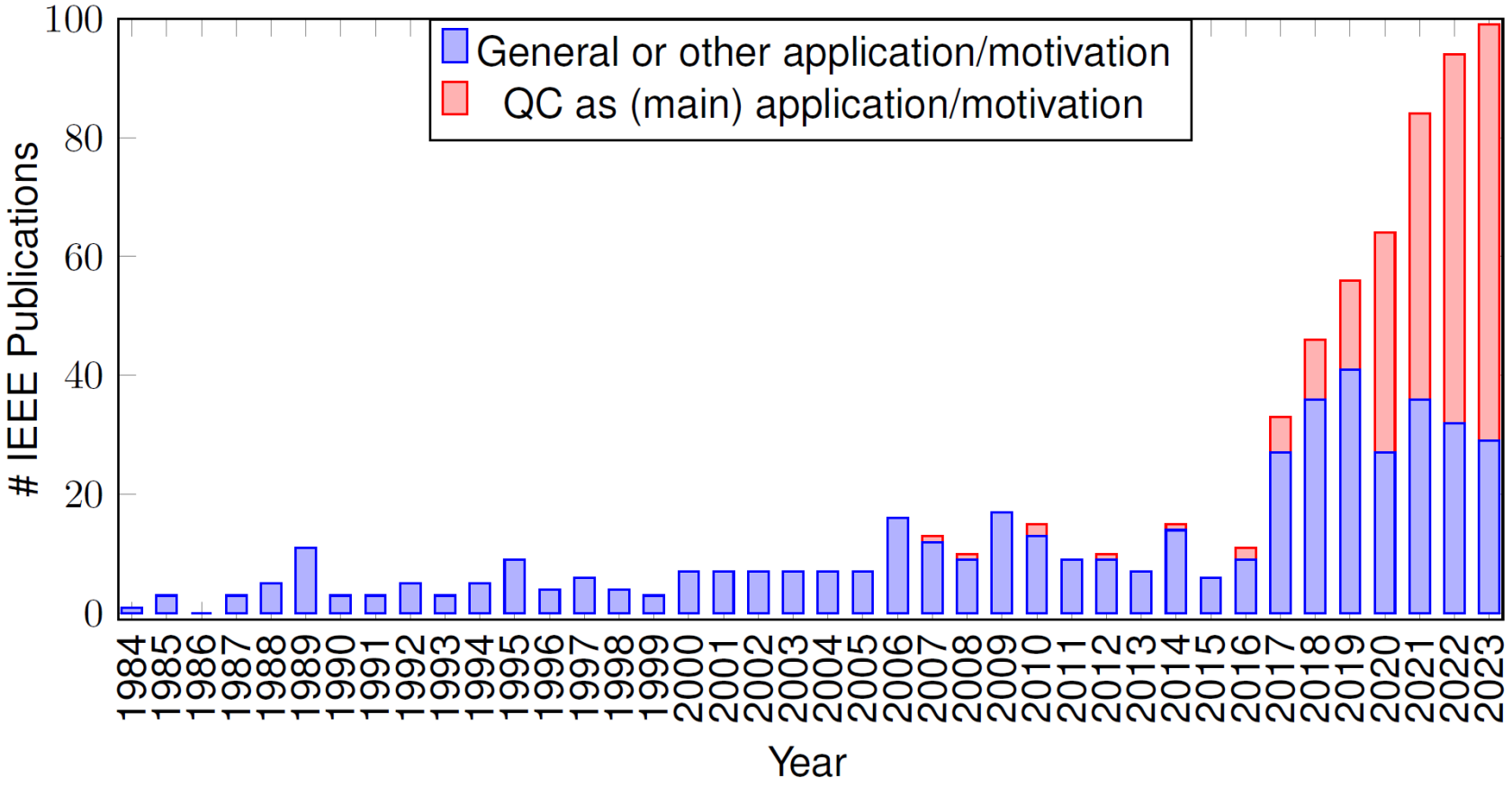
CRYOGENIC INTEGRATED CIRCUITS

In the Spotlight



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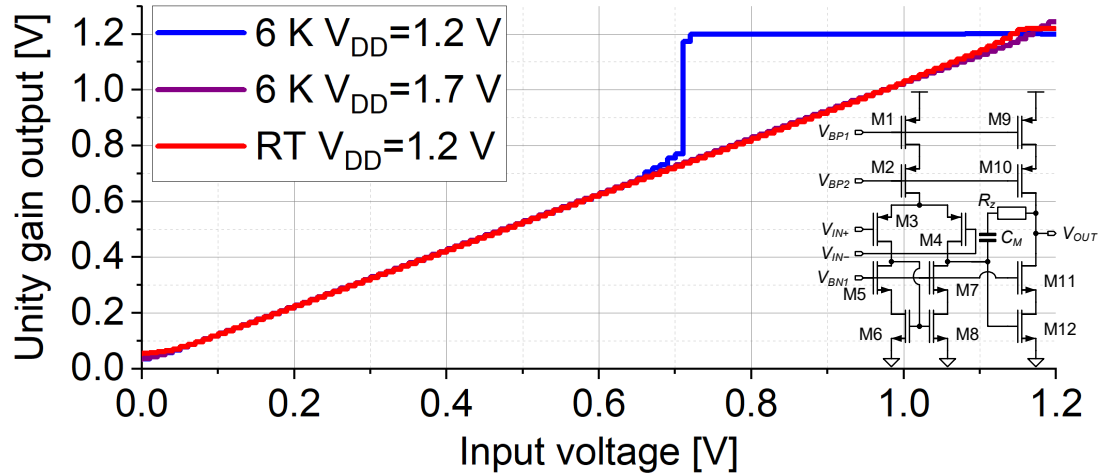
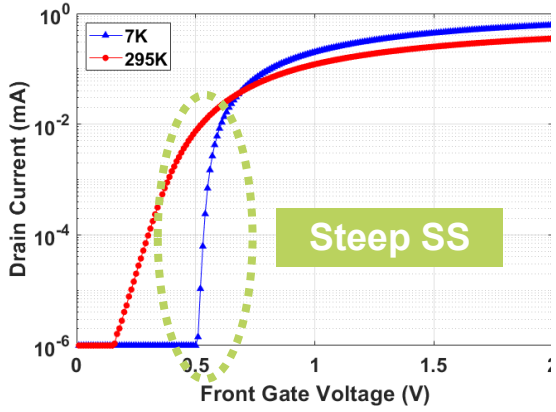
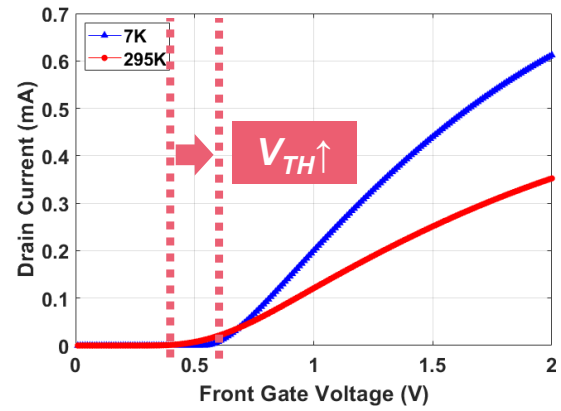
OPAMP

- Clipping of Opamp output at cryo temp.
  - No subthreshold operation possible
  - Due to steep SS
- Increase supply for extra headroom
  - Use **low supply circuit topologies**
- **Pay extra attention to stay in strong inversion**
  - Compensate or be aware of V_{TH} shift







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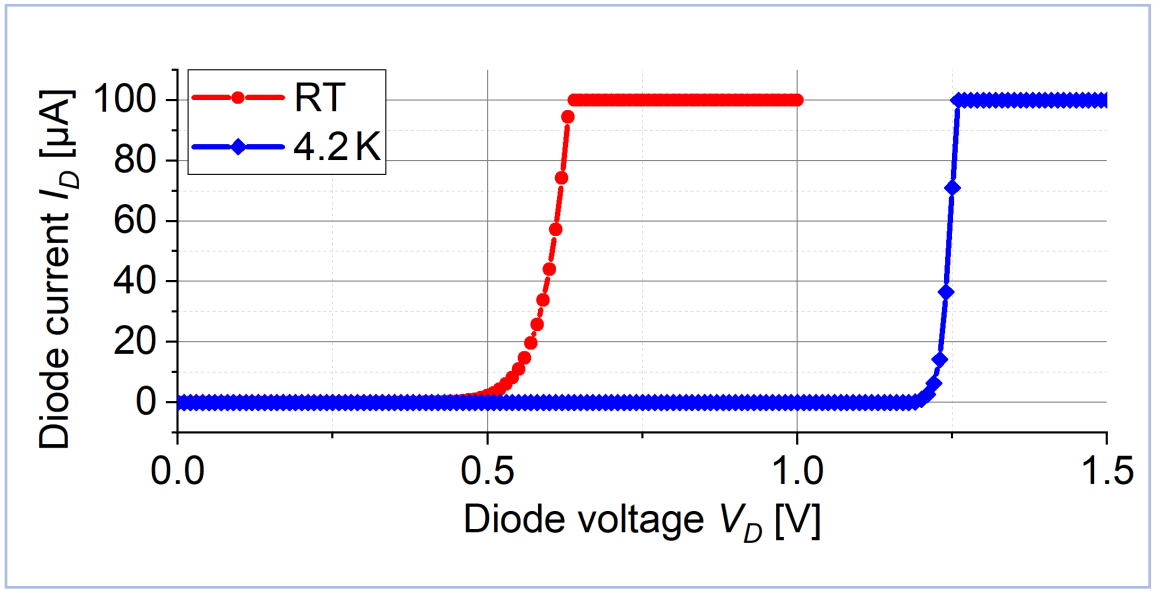
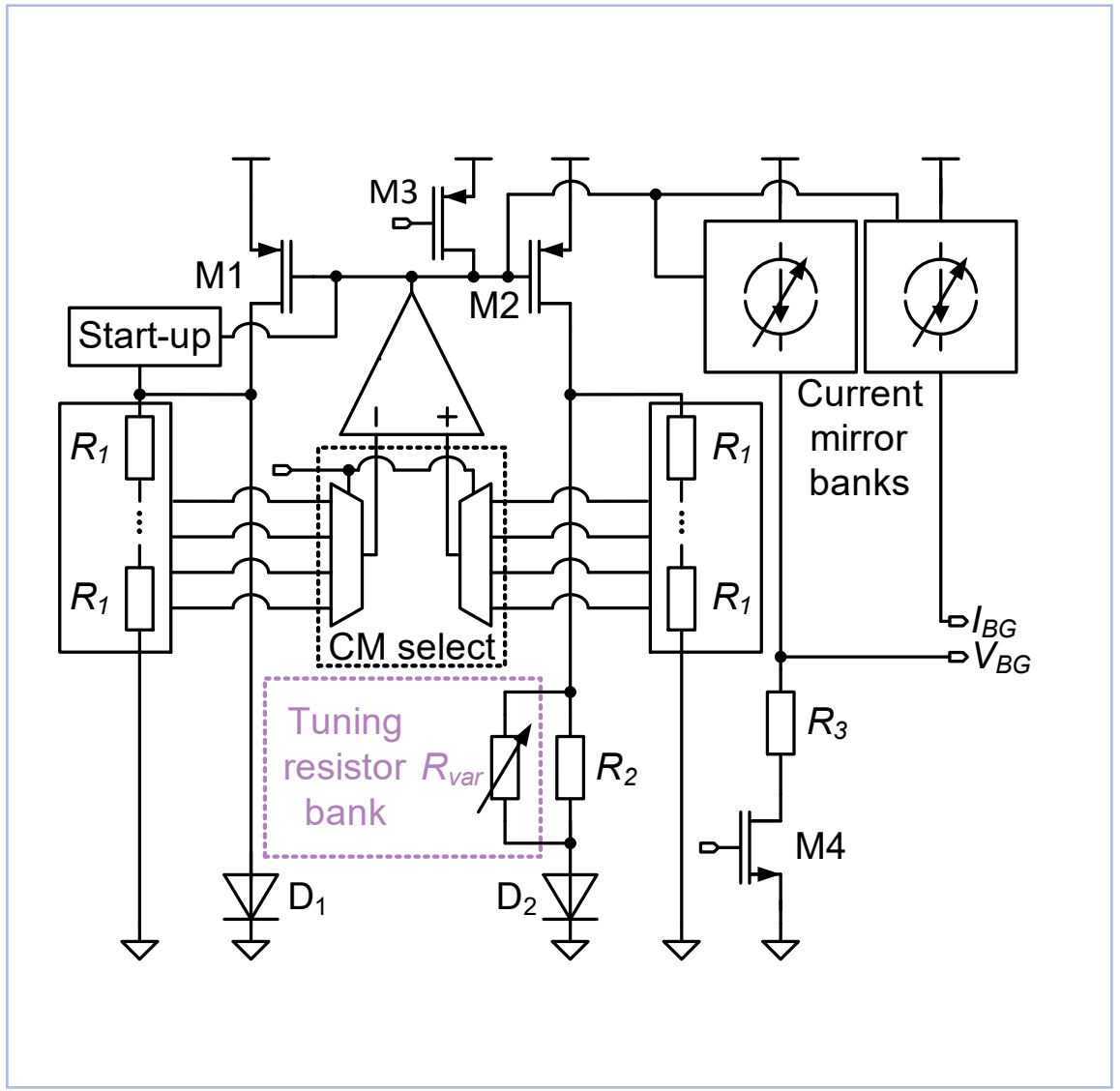
BANDGAP

Design

- Current-mode topology[1] in 65 nm bulk CMOS
- Tuning options for cryogenic temperature
- Diode behavior at room temp. (RT) and 4.2 K





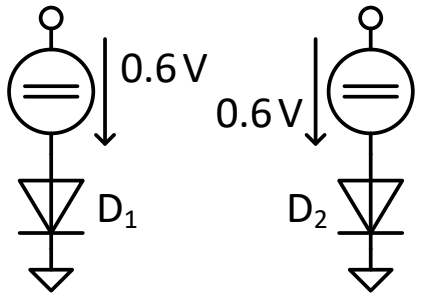
[1] H. Banba et al. “A CMOS bandgap reference circuit with sub-1-V operation”. In: IEEE Journal of Solid-State Circuits 34.5 (May 1999), pp. 670–674. doi: 10.1109/4.760378.

BANDGAP

Simulation Results

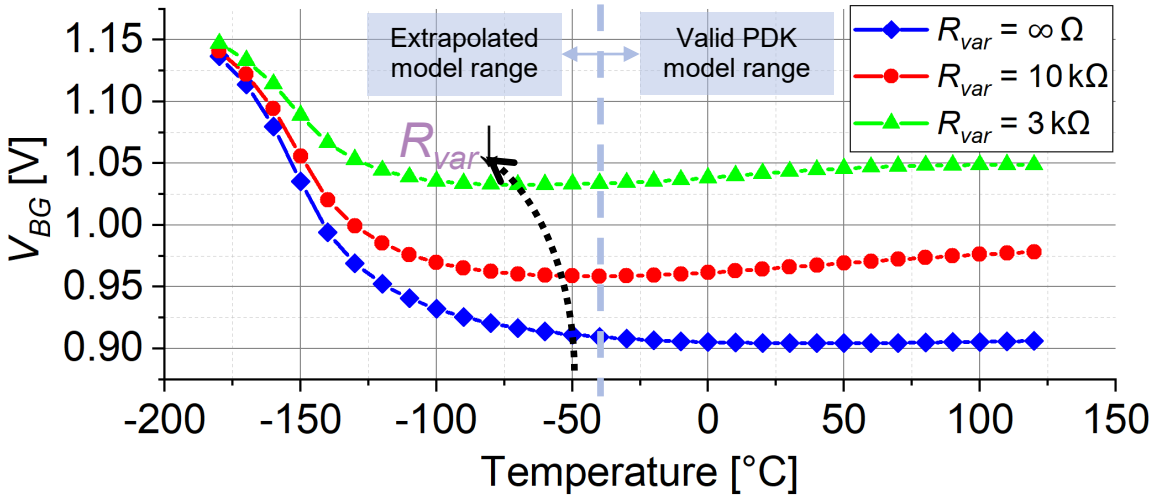
- PDK valid from −40 °C to +125 °C

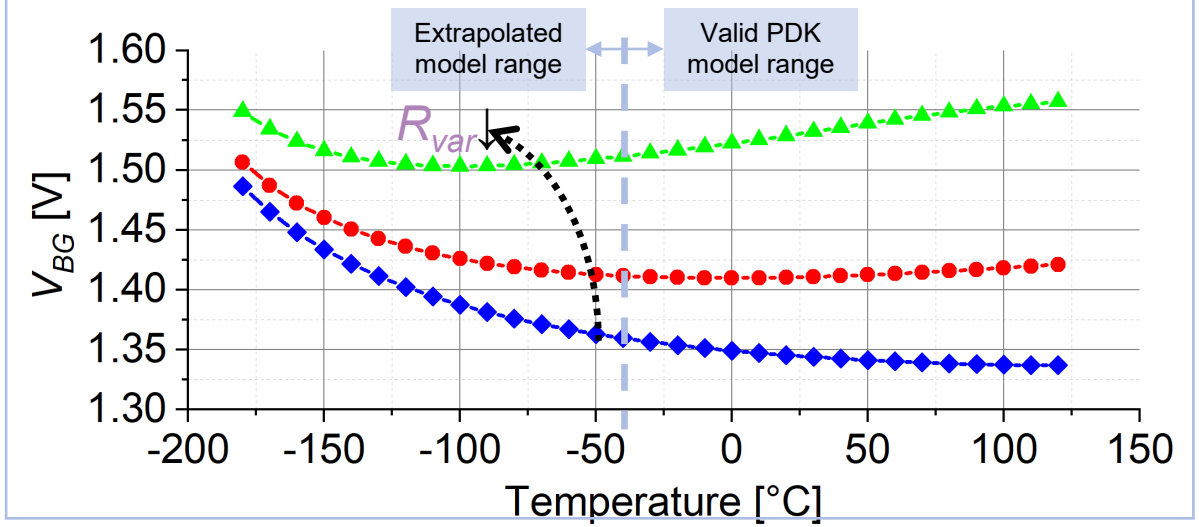
- Cryo V_{TH} increase of D_1 and D_2 ≈ 0.6 V
  - Modeled by added voltage sources
  - V_{DD} increase required: 1.2 V → 1.8 V



Added sources

V_{DD} increased





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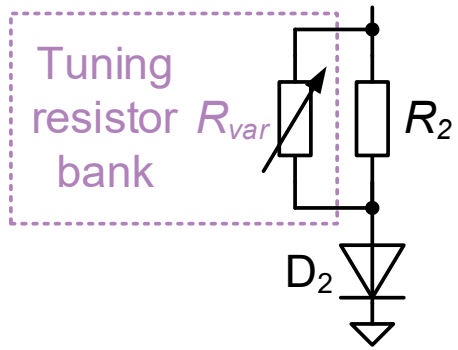
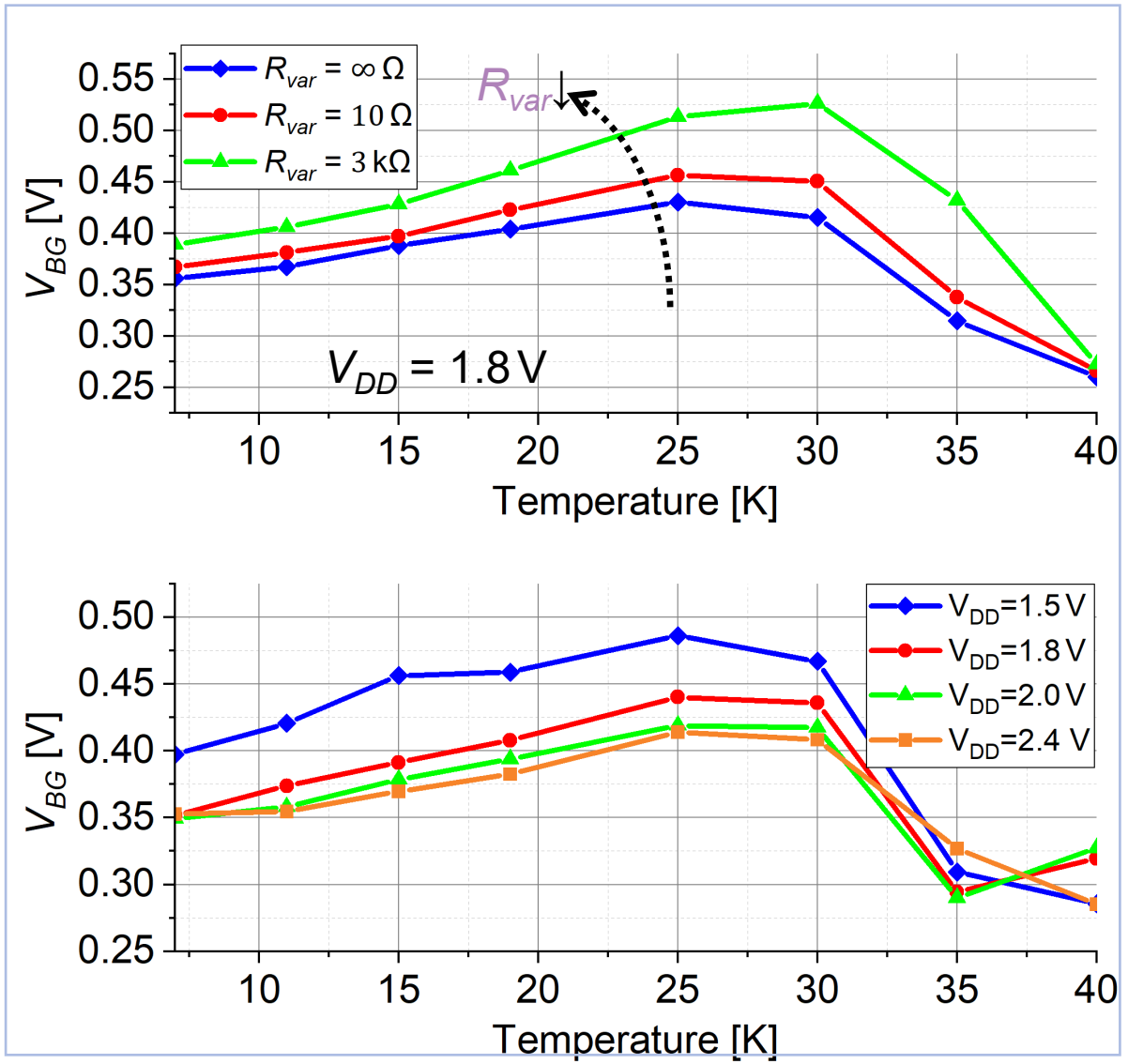
BANDGAP

Measurement

- BG curve is tilted like desired by R_{var}
  - V_{BG} curvature is „convex“
  - Contradicting all simulation results
- In order to improve temp. compensation
  - Need to increase R_2
  - Set $R_{var} \rightarrow \infty\ \Omega$
- BG sweetspot at V_{DD} = 1.8 V
  - Well operating & min. power
- Notable kink at temp. 35 K



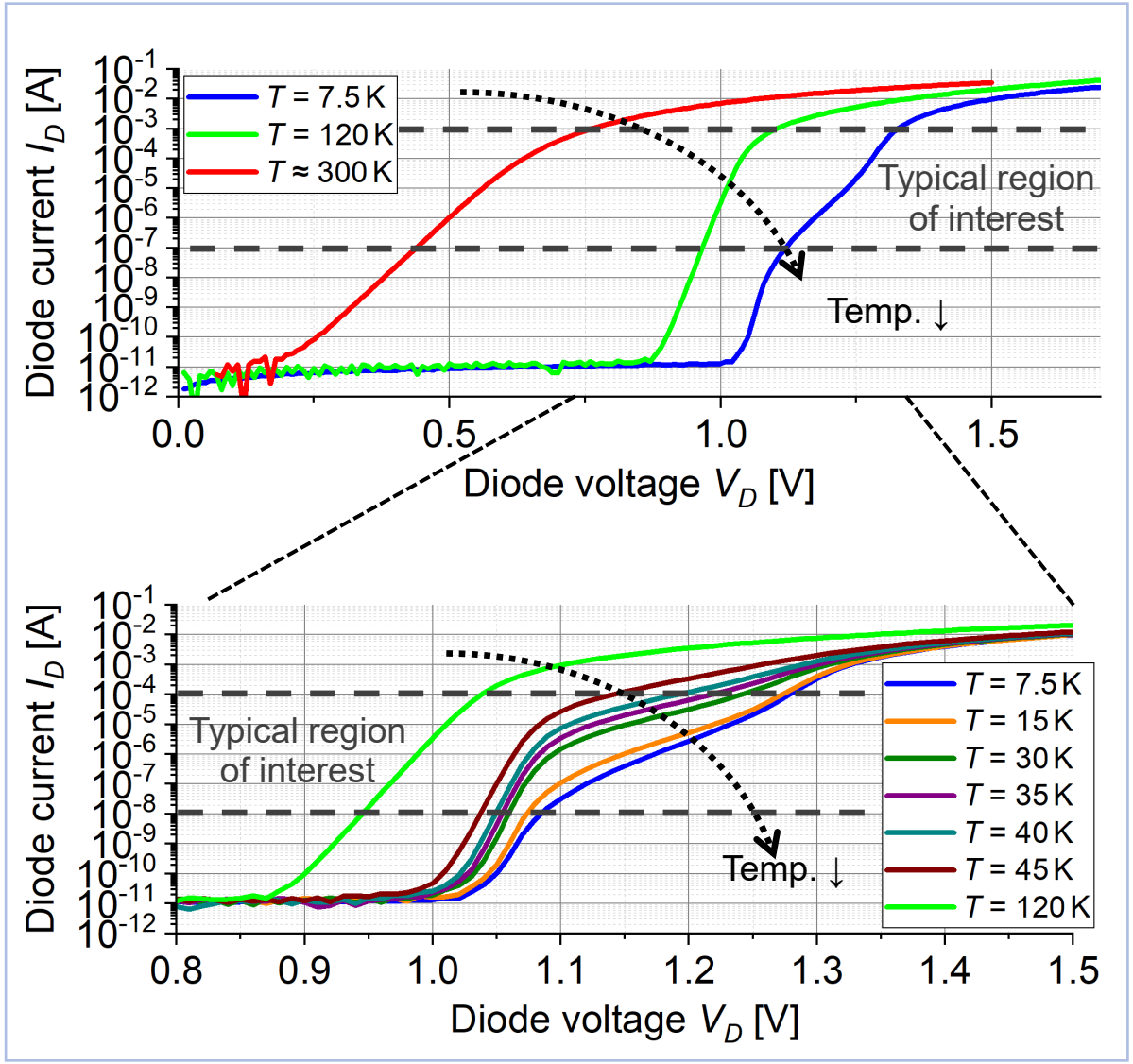


BANDGAP

Measurement

- Steeper diode slope with reduced temperature
  Kink apparent for cryo. temperature
- Notable for temperature $T \lessapprox 40$ K
  - Flattening the curve in the typical region of interest (100 nA to 100 µA)
  - Transition from no-kink to kink

- BG output V_{BG} kink also at 35 K
- BG design requires dedicated diode models and understanding for cryo.



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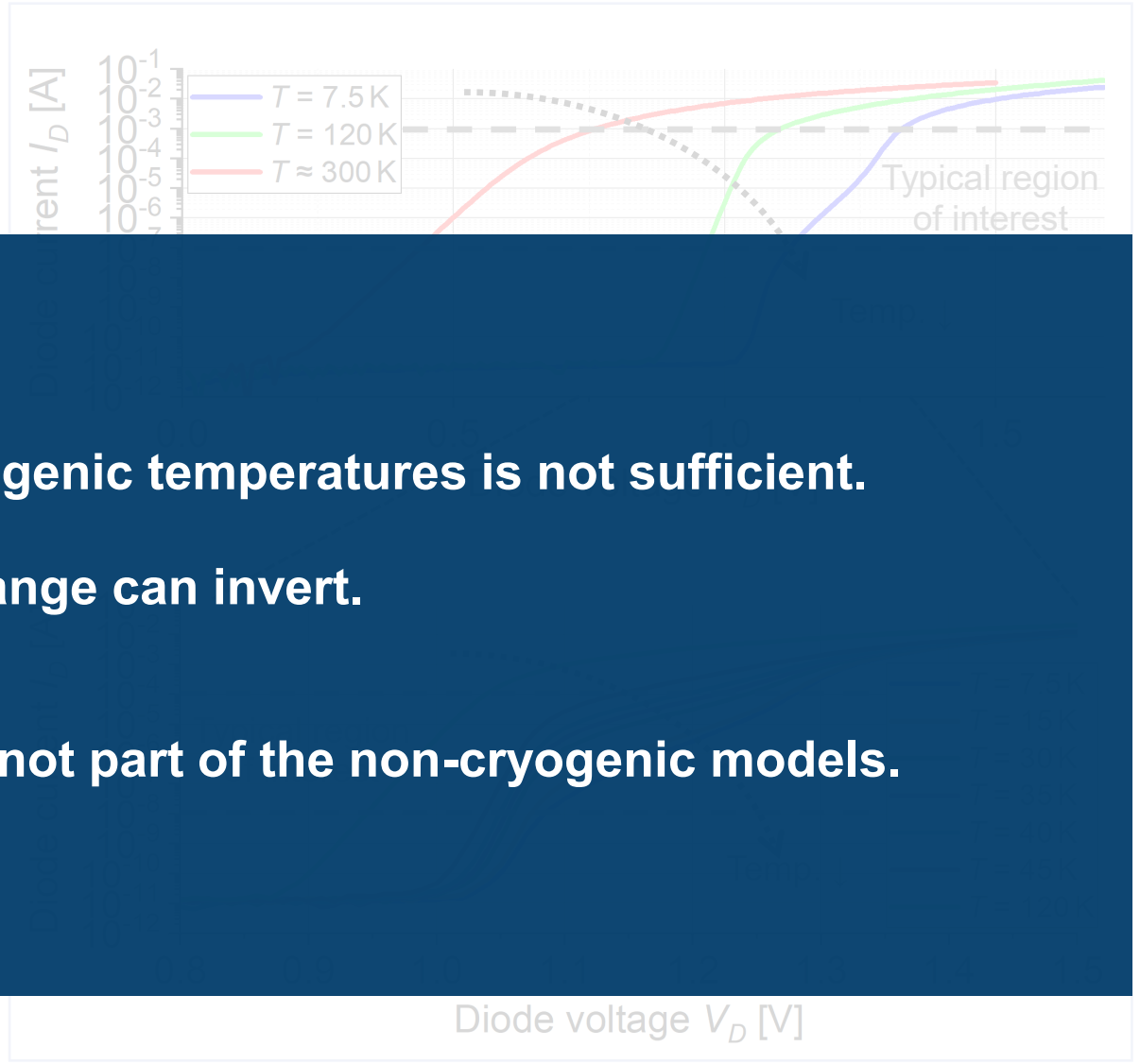
BANDGAP

Measurement



Extrapolating trends from RT to cryogenic temperatures is not sufficient.

Direction of change can invert.

New effects come into play which are not part of the non-cryogenic models.

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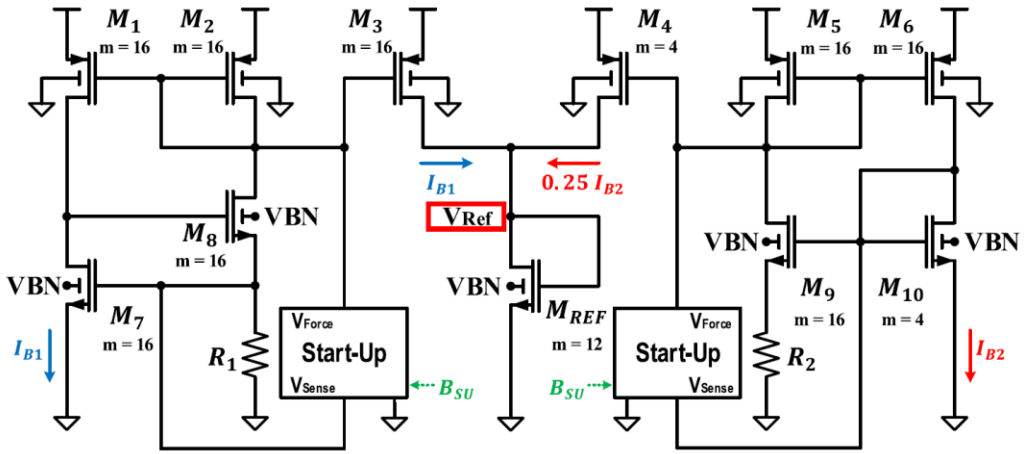
CRYOGENIC INTEGRATED CIRCUITS

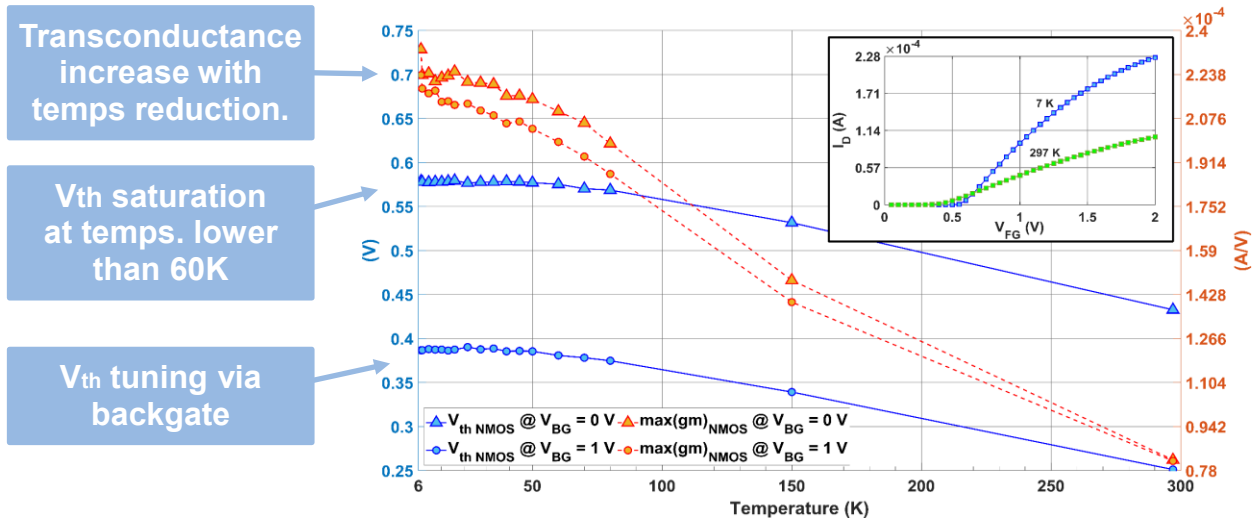
Voltage Reference in 22nm FD-SOI

- Cryogenic V_{TH} saturation as working principle
- The circuit saturates M_{REF} while in V_{TH} saturation temperature region

- Simple and without post-fabrication correction

  →**Utilize transistor effects in cryo!**





[2] A. R. Cabrera-Galicia, et.al, "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology," in IEEE Open Journal of Circuits and Systems, vol. 5, pp. 377-386, 2024, doi: 10.1109/OJCAS.2024.3466395

CRYOGENIC INTEGRATED CIRCUITS

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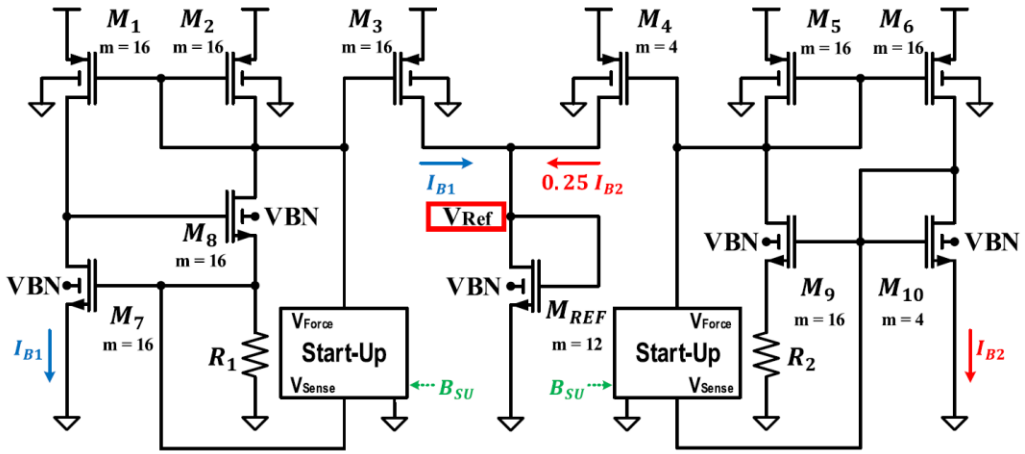
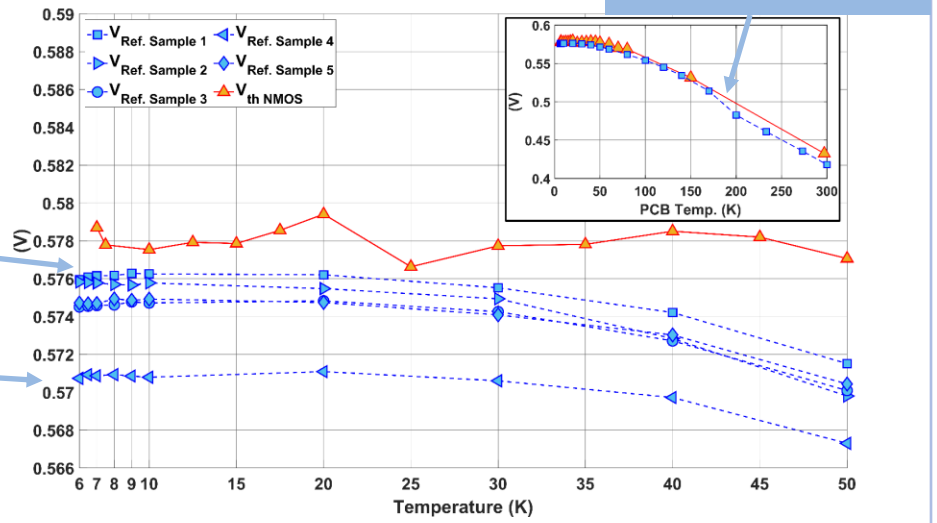


TC = 300 ppm/K @ Temp = [6 K, 50 K]

5 sample chips are tested.

VRef. Sample 1 is compared with Vth from I/O NMOS.



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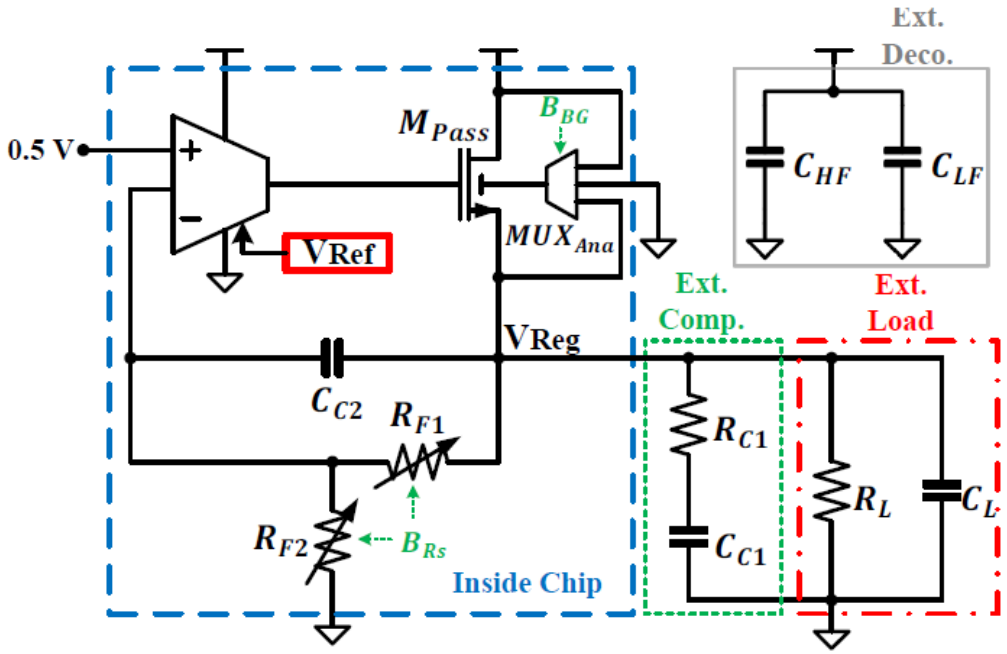
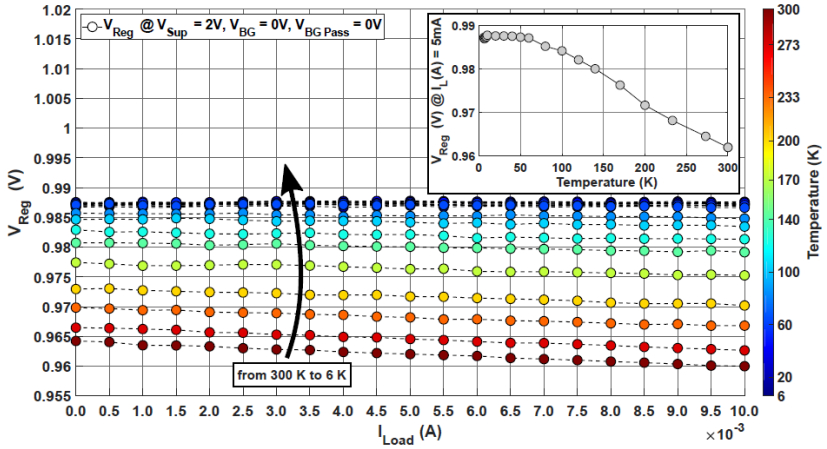
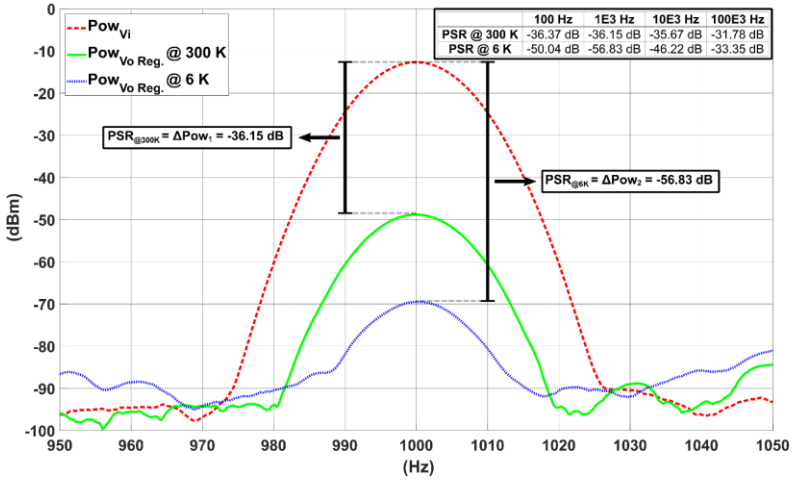
CRYOGENIC INTEGRATED CIRCUITS

Voltage Reference and Regulator Circuit in 22nm FD-SOI







	100 Hz	1E3 Hz	10E3 Hz	100E3 Hz
PSR @ 300 K	-36.37 dB	-36.15 dB	-35.67 dB	-31.78 dB
PSR @ 6 K	-50.04 dB	-56.83 dB	-46.22 dB	-33.35 dB

[2] A. R. Cabrera-Galicia, et.al, "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology," in IEEE Open Journal of Circuits and Systems, vol. 5, pp. 377-386, 2024, doi: 10.1109/OJCAS.2024.3466395

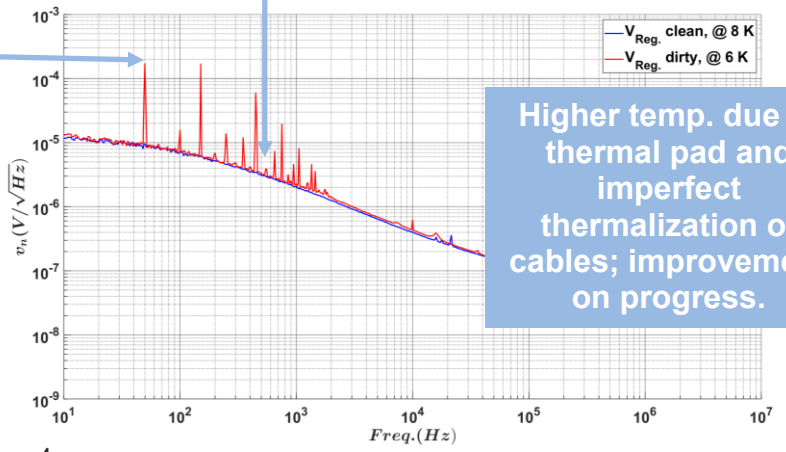
NOISE

Cryostat and Voltage Reference & Regulator

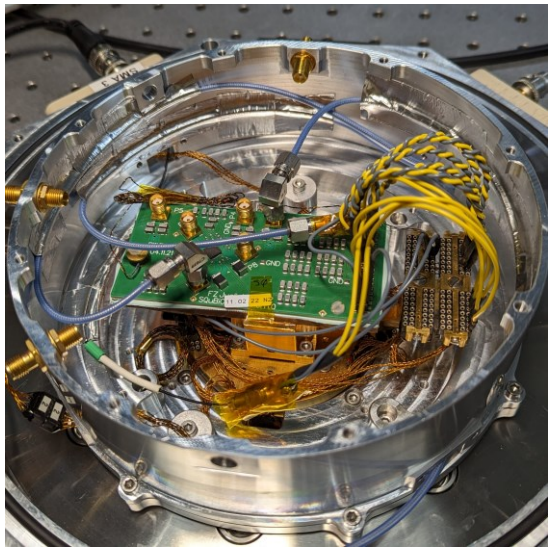
- Avoid GND loops in the cryostat
  - Counteracting the wish to thermal couple
- Increased 1/f noise; decreased thermal noise

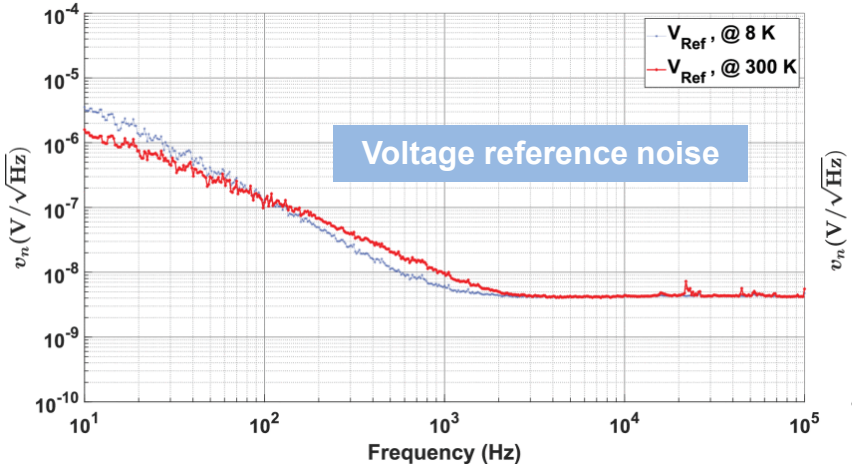
Ground loop noise is removed by electrically detaching the regulator from the cold plate.

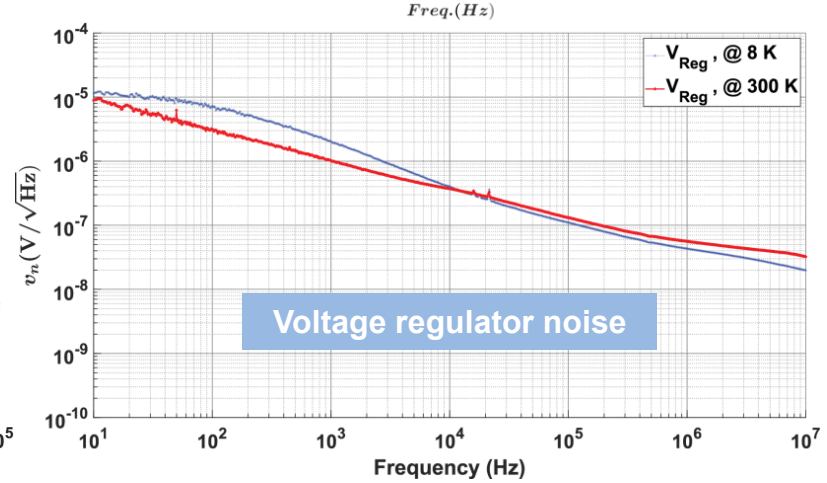
Ground loop noise is coupled to regulator output via cold plate.



Higher temp. due to thermal pad and imperfect thermalization of cables; improvement on progress.







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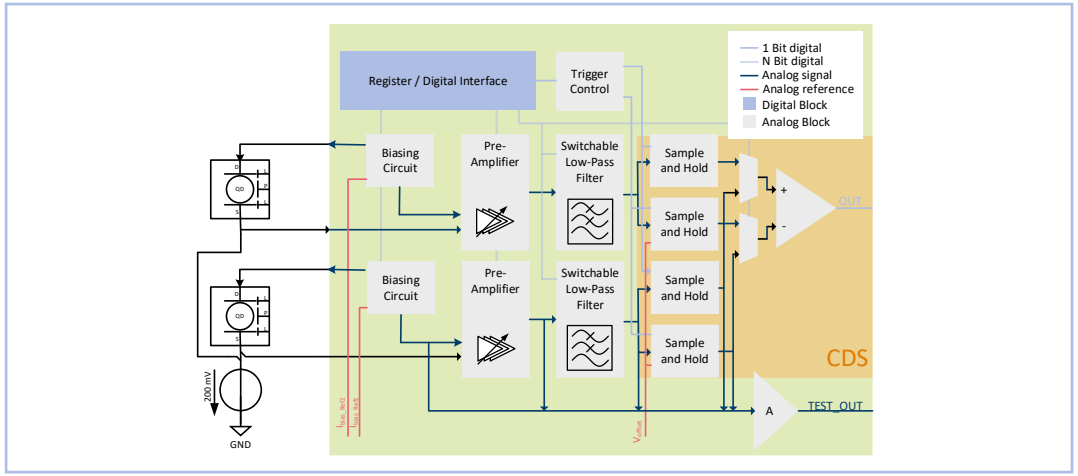
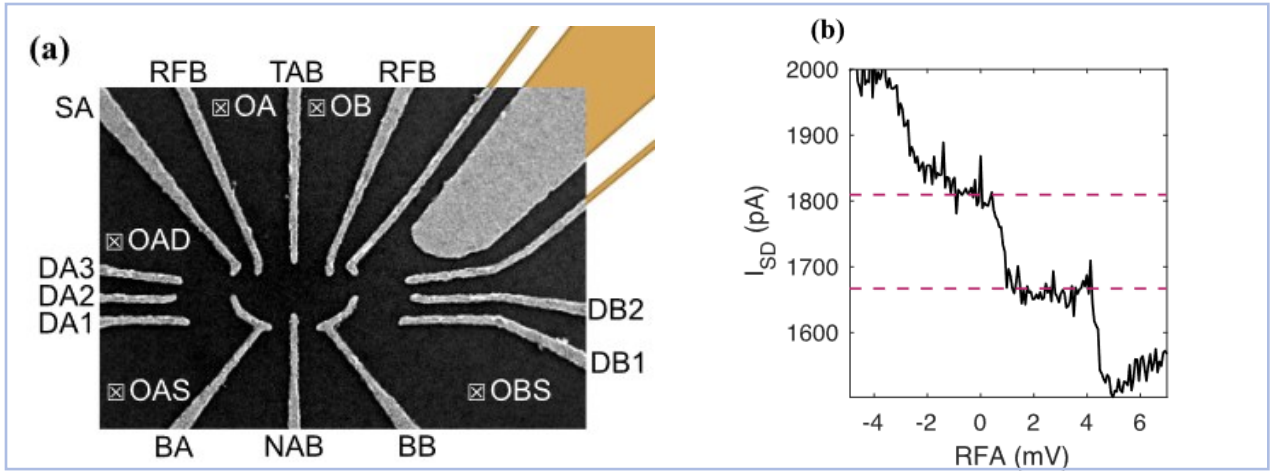
CRYOGENIC INTEGRATED CIRCUITS

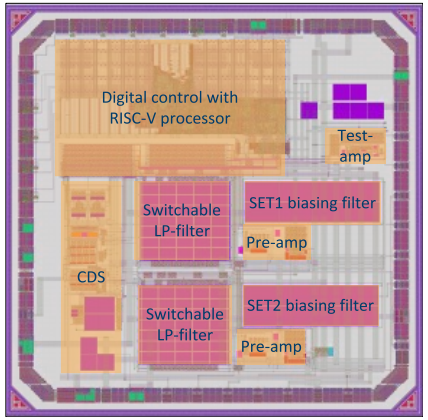
QUOCCA.SET
SET Readout

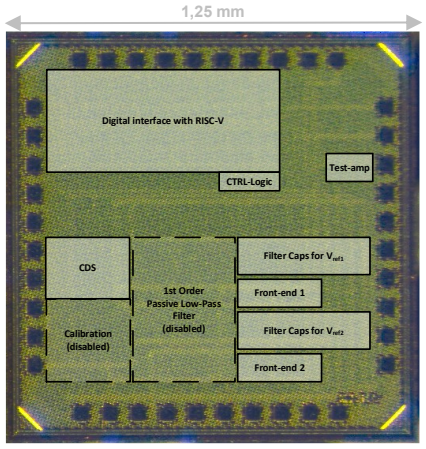
Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- **Target: readout of quantum dots**
- Pauli spin blockade to convert spin to charge
- Single electron transistor (SET) to convert charge to current (signal ca. 250 pA)









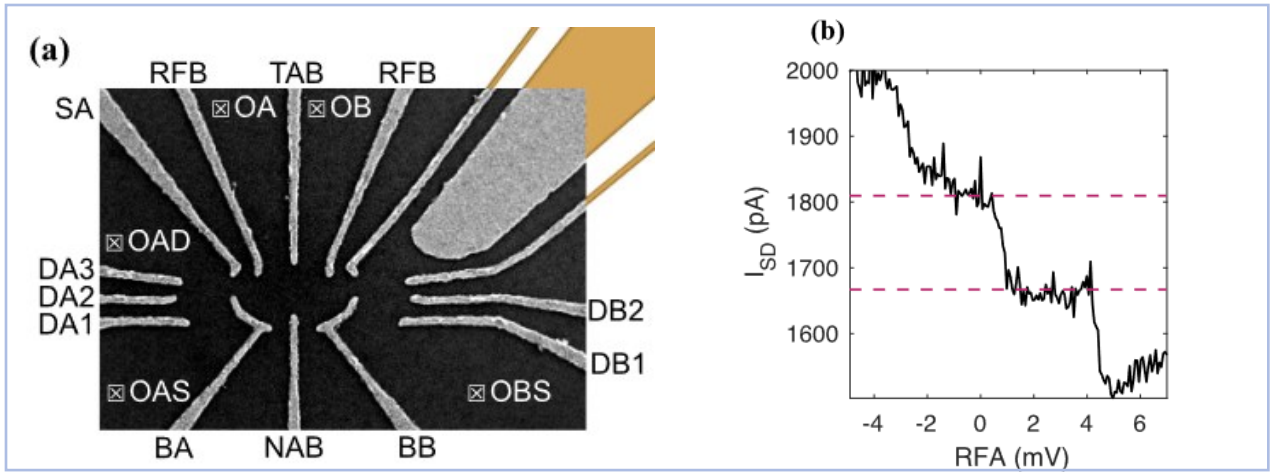
[3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4

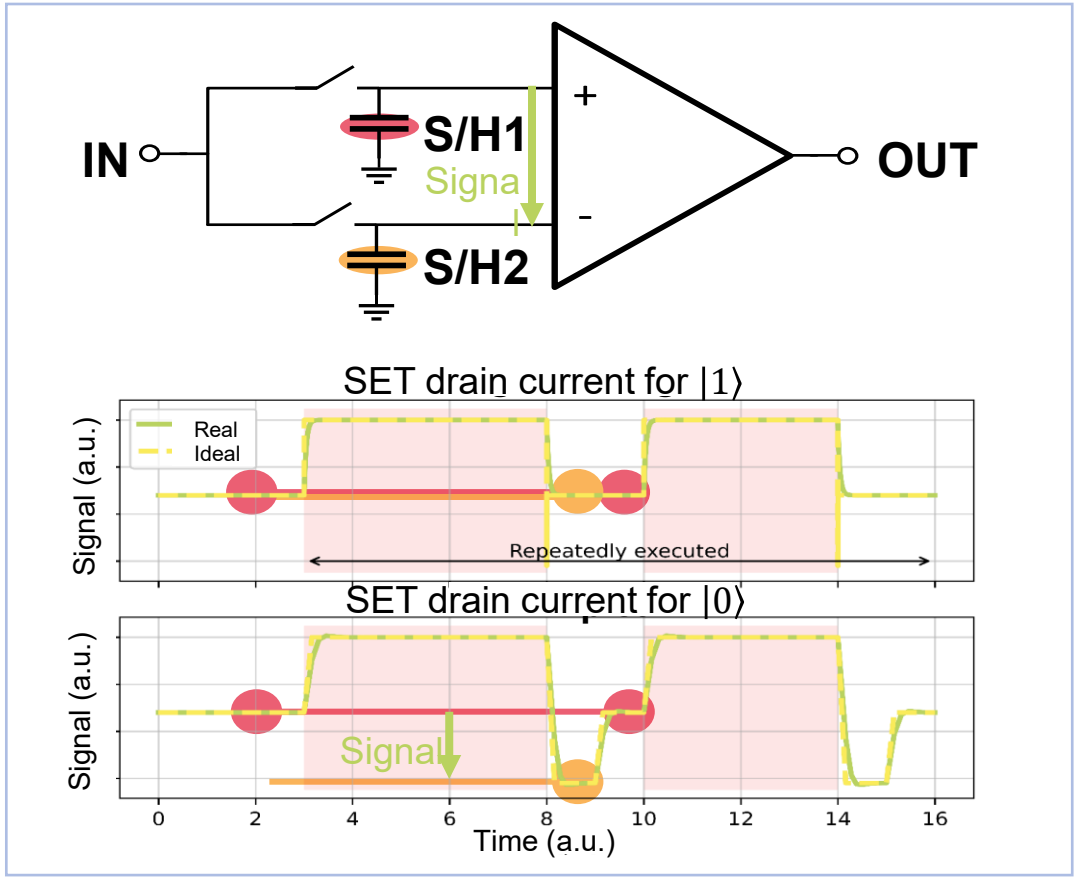
CRYOGENIC INTEGRATED CIRCUITS

QUOCCA.SET
SET Readout

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- **Correlated Double Sampling (CDS)**
  - 1st sample after qubit initialization
  - 2nd sample after qubit operation
  - Cancellation of low frequency noise





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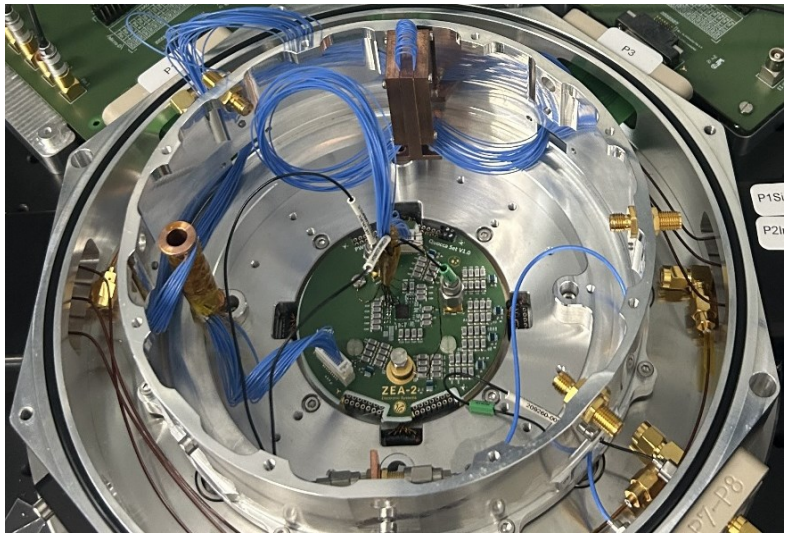
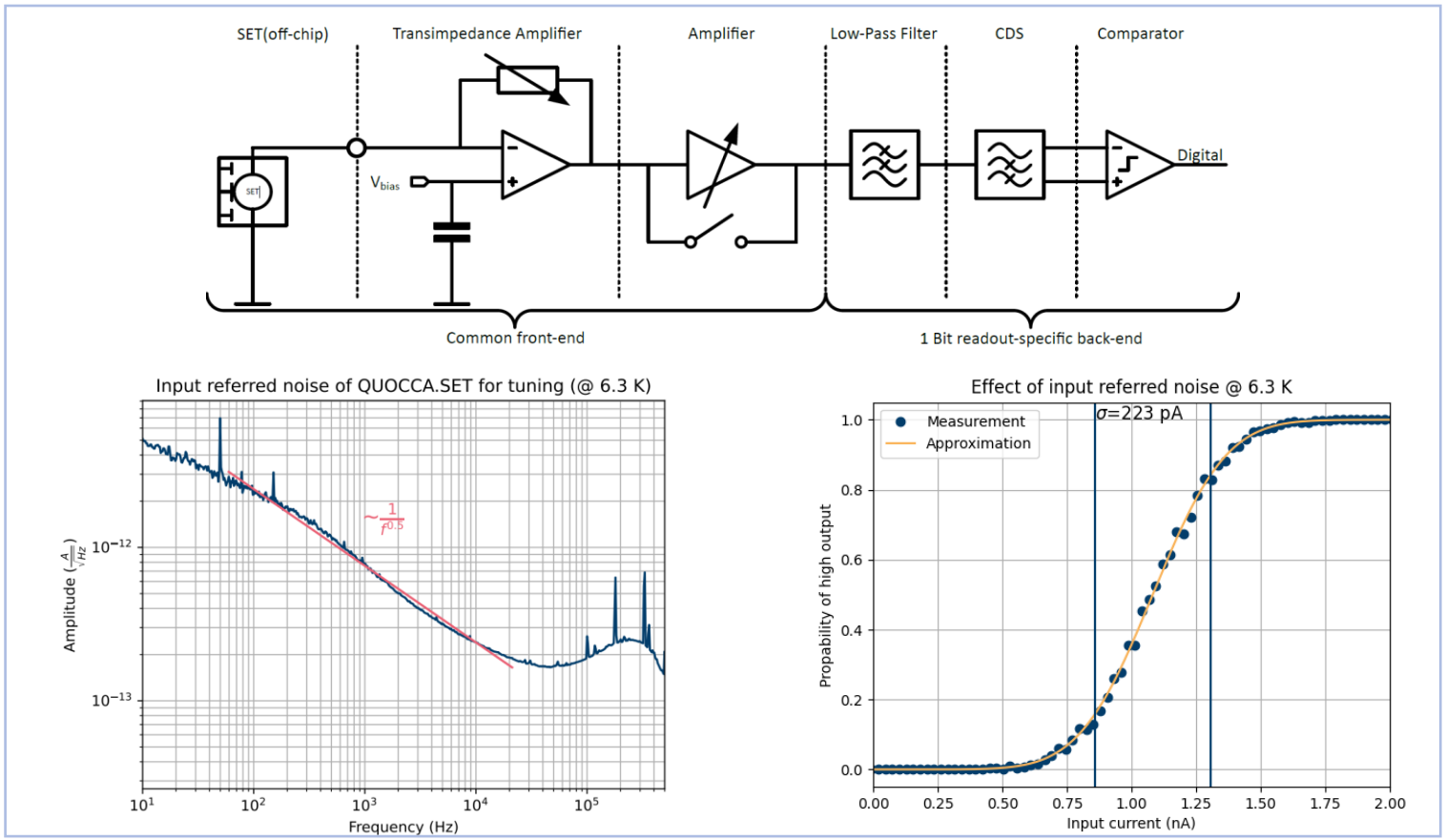
CRYOGENIC INTEGRATED CIRCUITS

QUOCCA.SET
SET Readout

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- 223 pA RMS @ 1 µs, max. BW
- 111 pA RMS @ 1 µs, 1 kHz BW
- Digital Power: 41 µW
- Analog Power: 33.6 µW/SET



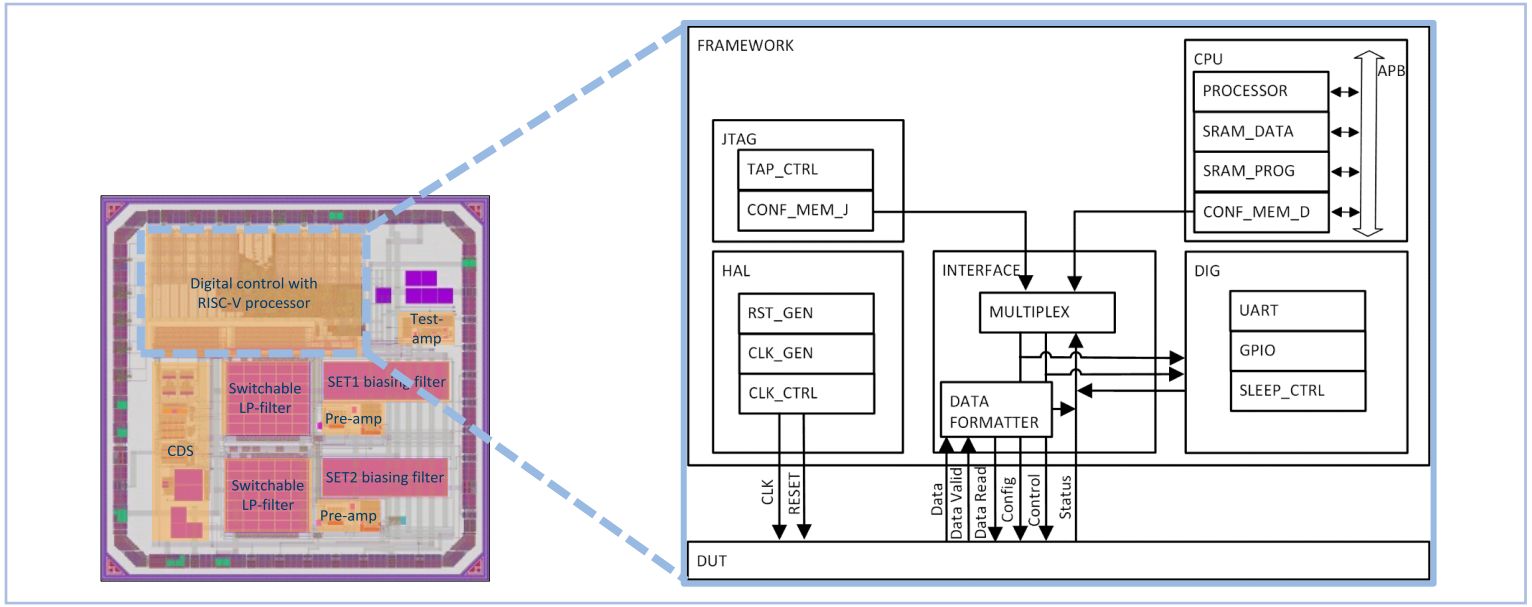


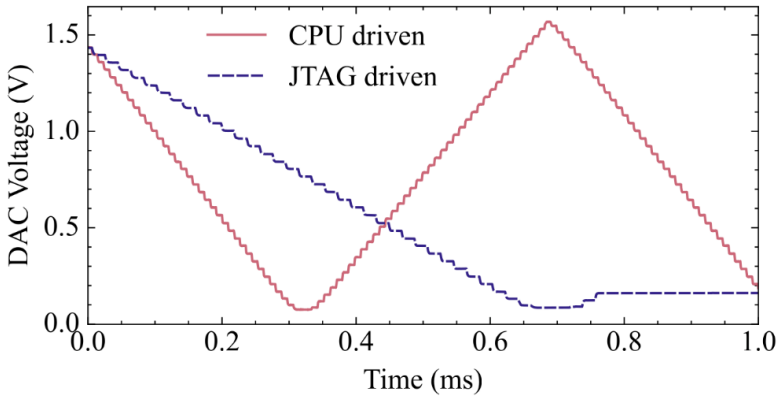
[3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4

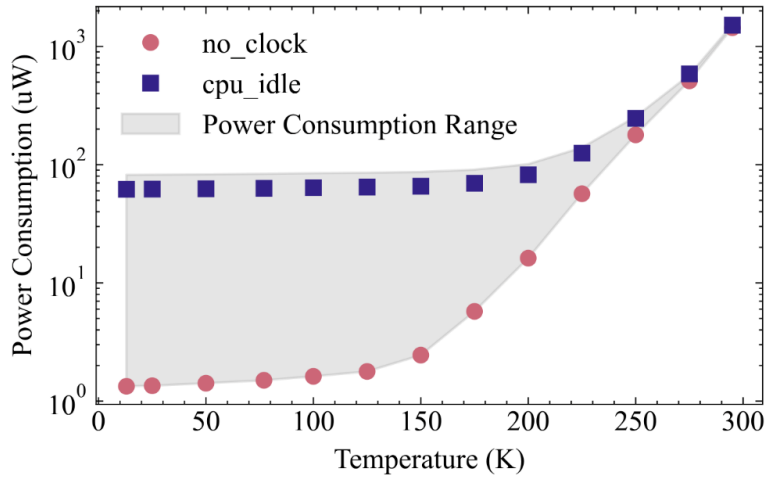
INTEGRATED RISC-V

Rapid Prototyping Platform for Integrated Circuits for Quantum Computing

- RISC-V with SRAM and APB
- Enables flexibility in control (algorithms)
- Leakage negligible at cryo







[4] J. Mair et al., "Rapid Prototyping Platform for Integrated Circuits for Quantum Computing," 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Volos, Greece, 2024, pp. 1-4, doi: 10.1109/SMACD61181.2024.10745395.

DIGITAL INTERFACE

Comparison of Industry Standard Protocols

Protocol	Pro ☺	Cons ☹
UART	2-wire interface (RX TX) No pull-up/down	Requires sync.
I²C	2-wire interface (SDA SCL)	Pull-ups
SPI	No pull-up/down	3[4]-wire interface (SCLK MOSI MISO [CE])
JTAG	No pull-up/down	4-wire interface (TCK TMS TDI TDO) Complex state-machine
cJTAG	2-wire interface (TCKC TMSC)	Complex state-machine Less established Optional Pull-ups/downs

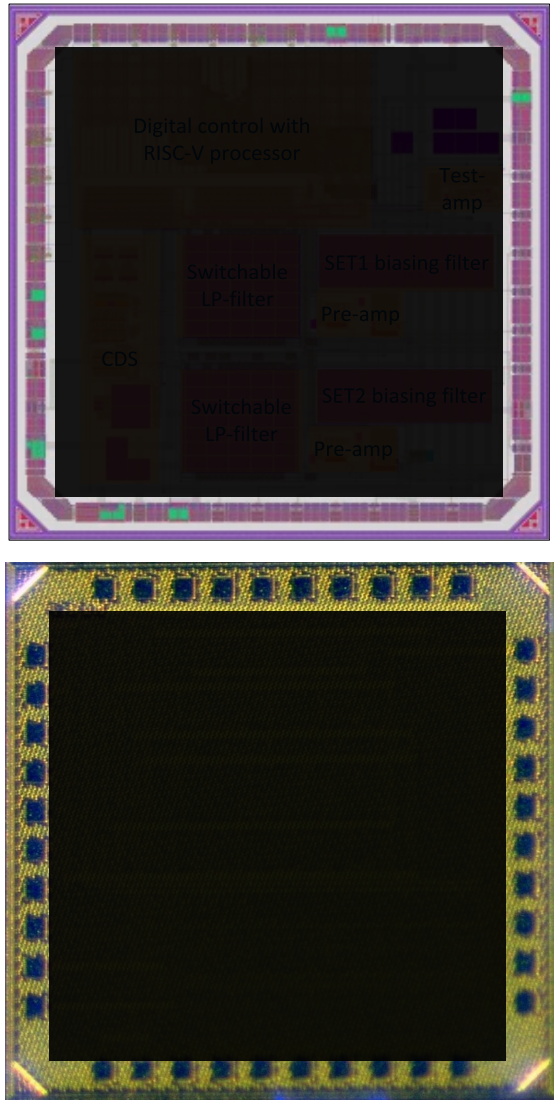
- Write & read IC config regs
- Configuration of IC blocks

POWER DRAW IN PADFRAME

Padframe IP Considerations

- Padframe IP is not made for cryo. temperature
- **Analog pads** are good
  - Typically less leakage in ESD structures

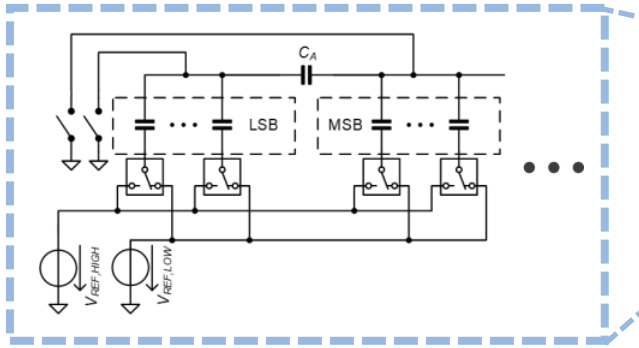
- **Digital pads**:
  - Functionality (mostly fine)
    - even with complex internal circuitry
  - Power (every µW counts at mK)
    - Consider internal power OK generation
    - May generate internal bias voltages (e.g. for IO<-> core voltage levelshifter)



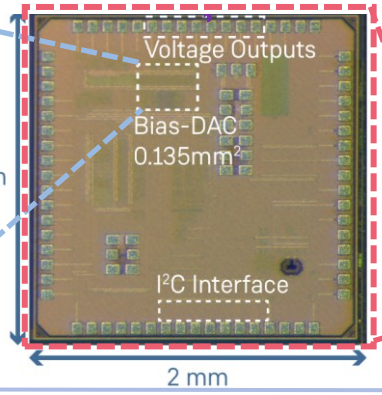
CRYOGENIC INTEGRATED CIRCUITS

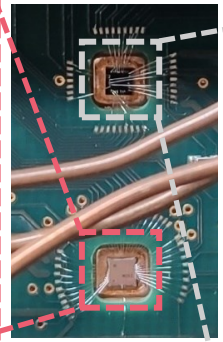
Qubit DC Biasing

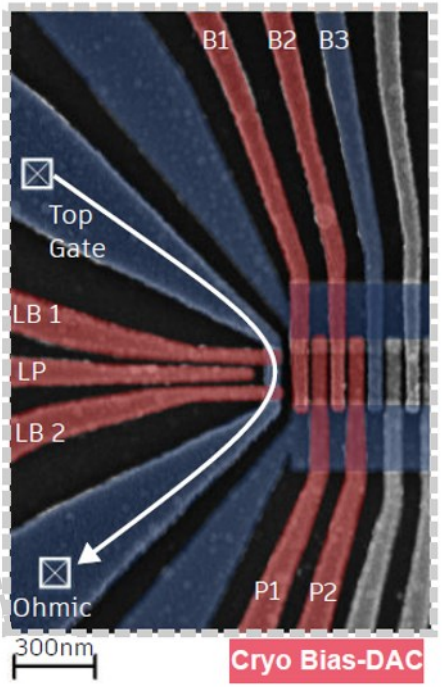

CO-INTEGRATION BIAS DAC WITH Si / SiGe QUBIT



[5]

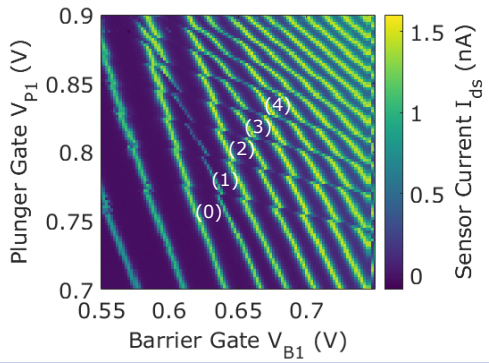


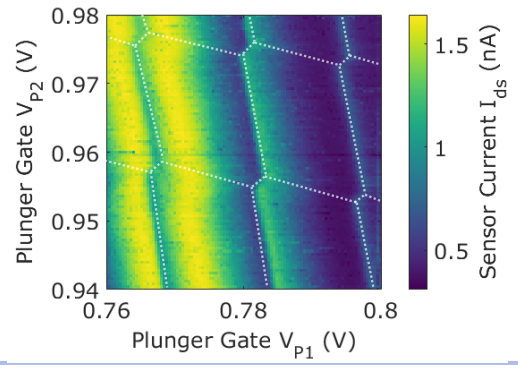




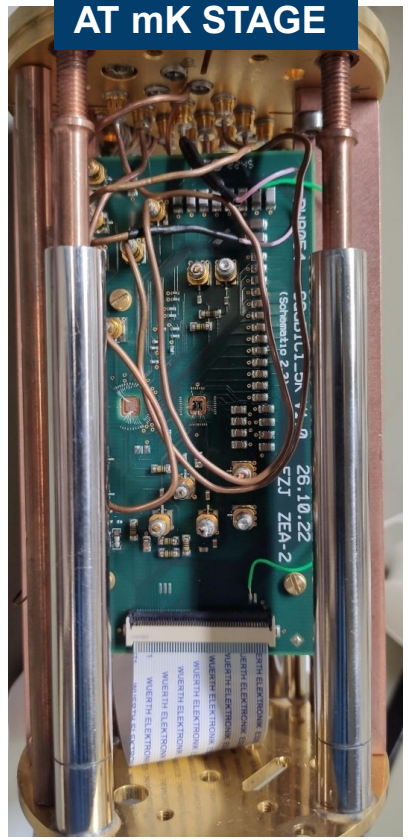
[6]

CHARGE SENSING OF SINGLE AND DOUBLE QUANTUM DOT





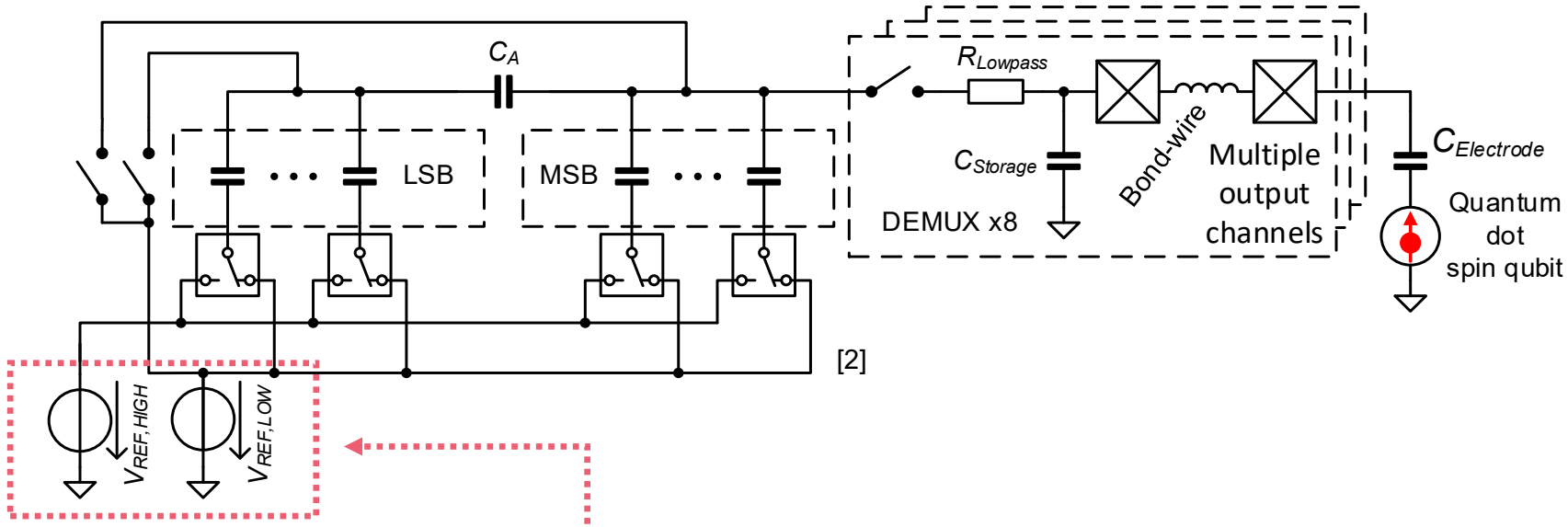
CRYO SETUP AT mK STAGE



[5] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE Solid-State Circuits Letters, 2020
[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

BIAS DAC

Charge-Redistribution Topology



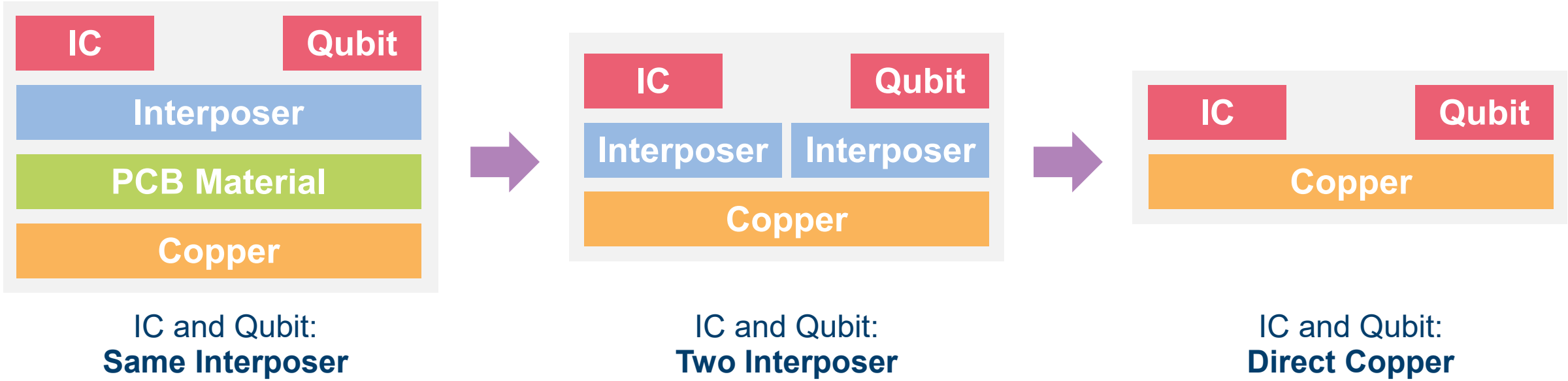
- Negligible static power dissipation
- Low thermal noise at cryo. T : $\bar{v}_N^2 = \frac{k_B \cdot T}{C}$
- No output buffer needed
  → Reduce power and noise

- Coarse tuning by on-chip MUX[2]
  → Reduce power and increase resolution
  → But need for calibration
- Multiple output channels per DAC

[5] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE Solid-State Circuits Letters, 2020

CRYOGENIC CO-INTEGRATION

Multiple Approaches



IC and Qubit:
Same Interposer

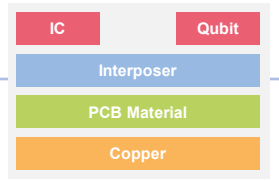
IC and Qubit:
Two Interposer

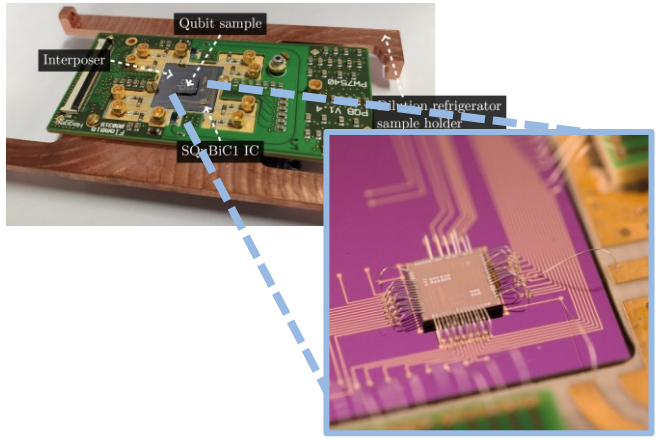
IC and Qubit:
Direct Copper

[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

CRYOGENIC CO-INTEGRATION

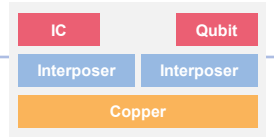
Multiple Approaches

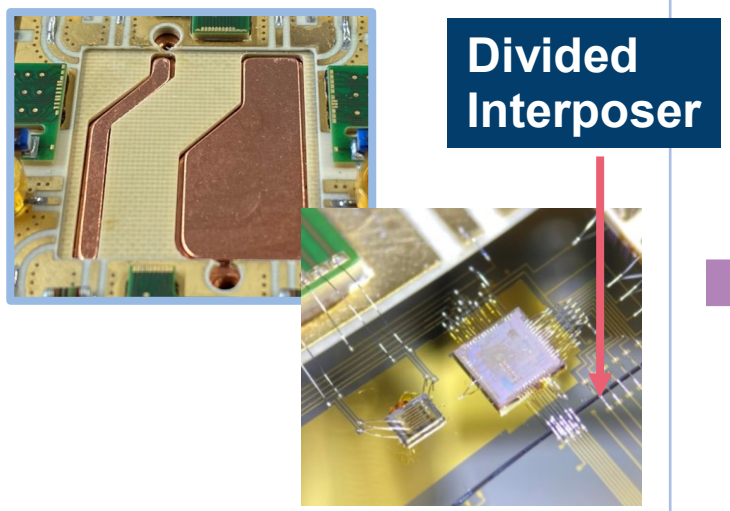




IC and Qubit:
Same Interposer

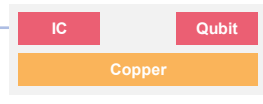
Electron Temperature
Qubit: ca. 2-3K

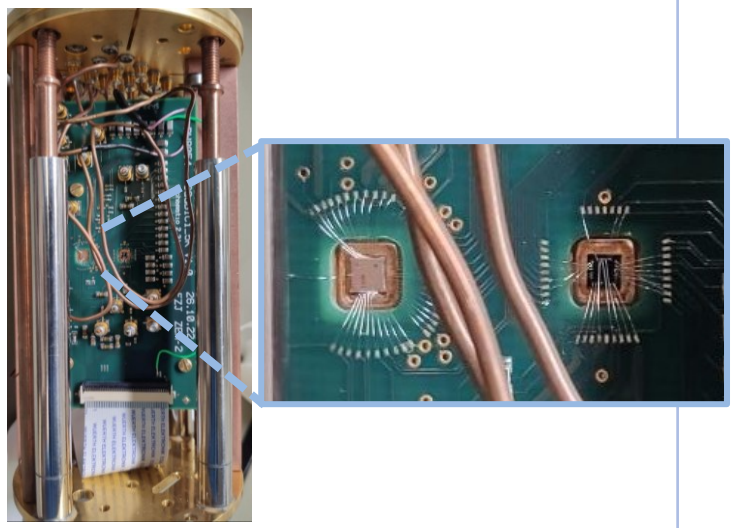




IC and Qubit:
Two Interposer

Electron Temperature
Qubit: ca. 0.5-1K





IC and Qubit:
Direct Copper

Electron Temperature
Qubit: < 0.4K

[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

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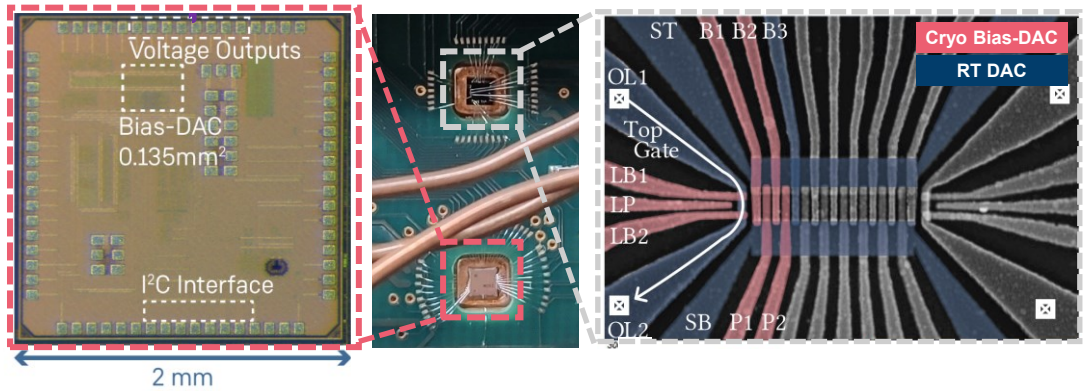
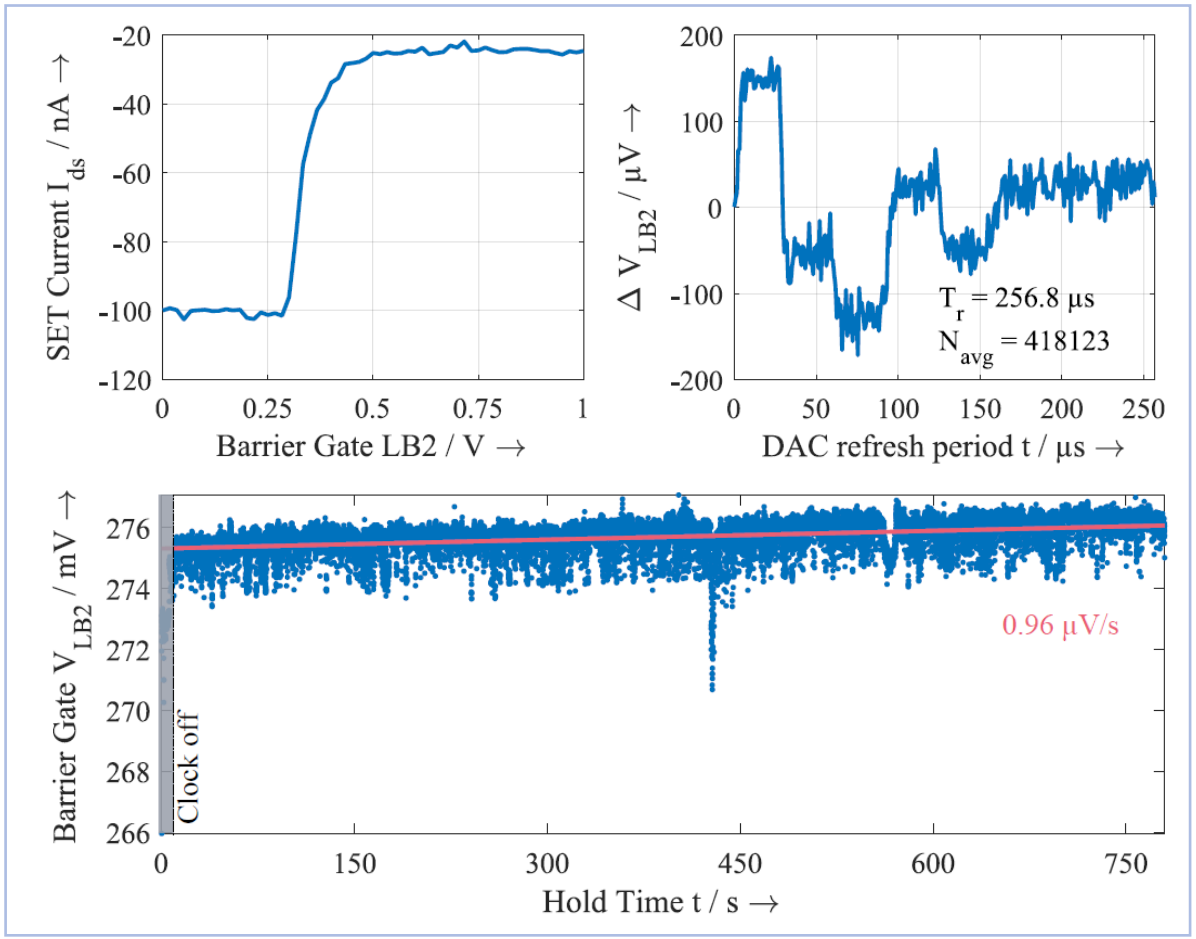
CRYOGENIC CO-INTEGRATION

Ultra-low Leakage Currents

- Bias DAC cycling through 7 metal electrodes
  - SET used as measurement amplifier
  - Visible cross-talk depending on location
- Leakage rates on metal electrodes meas.
  - 2 pF on-chip cap.; ca. 300 fF off-chip cap.
  - Ultra-low voltage drift of <1 µV/s





[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

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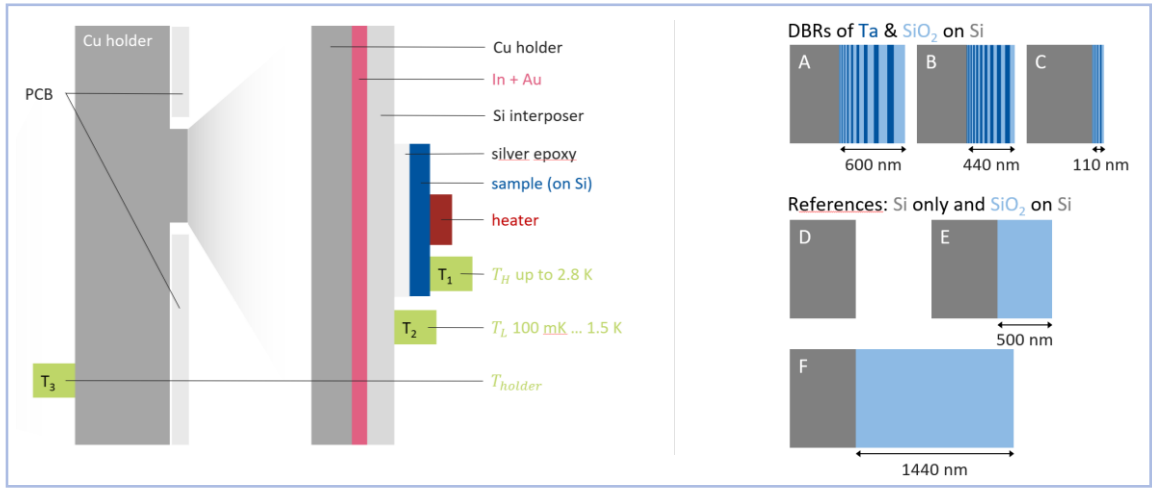
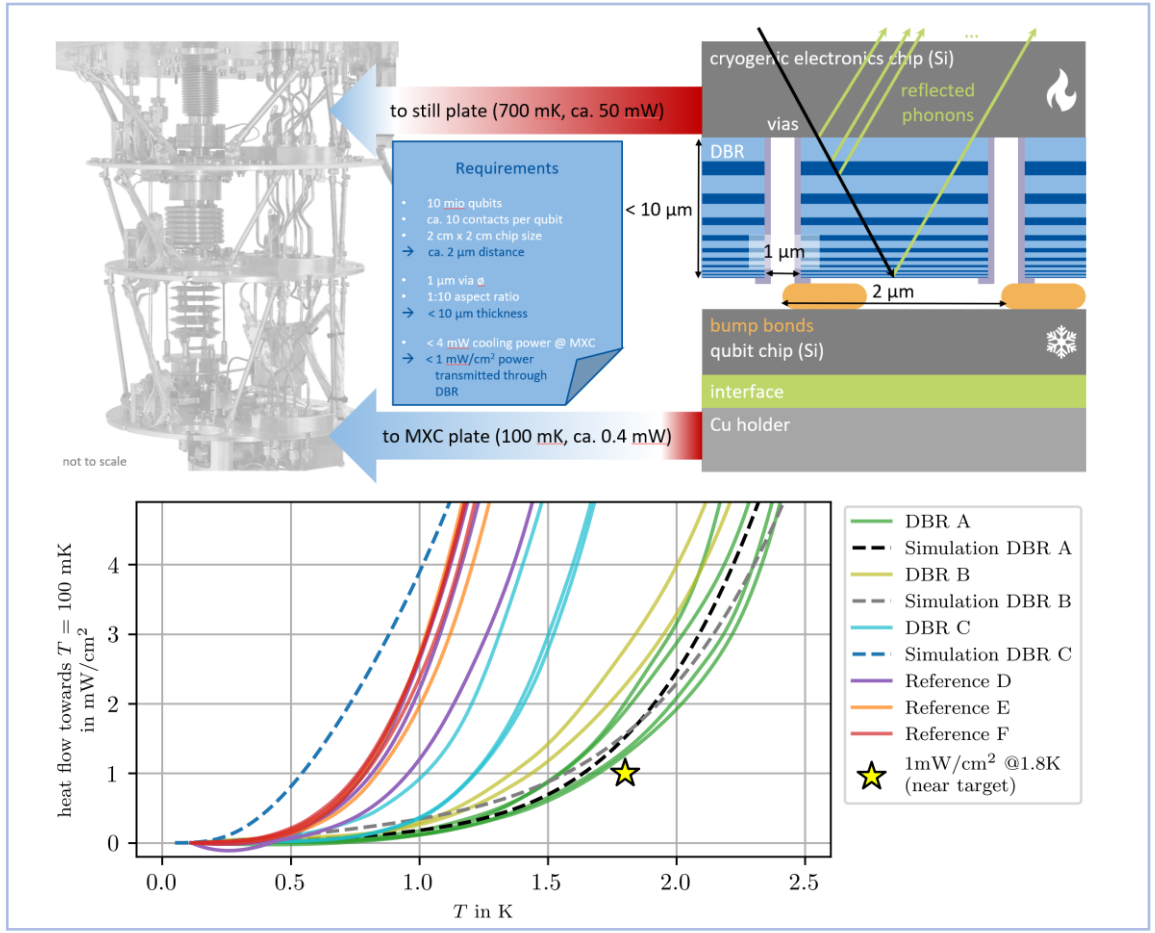
BRAGG REFLECTORS

Thermal Insulation Between Cryogenic Control Electronics and Qubits

- Layers of alternating acoustic impedance
- Broadband constructive interference
  → exponentially increasing thickness
- 600-nm-thick DBR near target
- DBRs insulate much better than the references





[7] I. Sprave et al., "Phononic Bragg Reflectors for Thermal Insulation Between Cryogenic Control Electronics and Qubits", Global Physics Summit 2025, MAR-J19/4

CRYOGENIC MEASUREMENTS

Inputs for a Cryo-PDK for 22 nm CMOS

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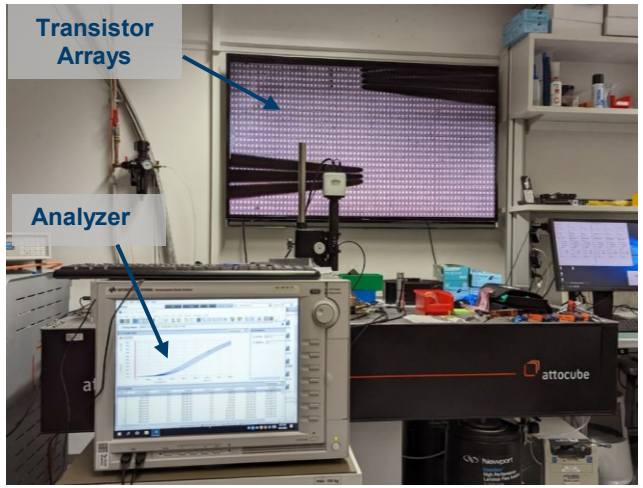
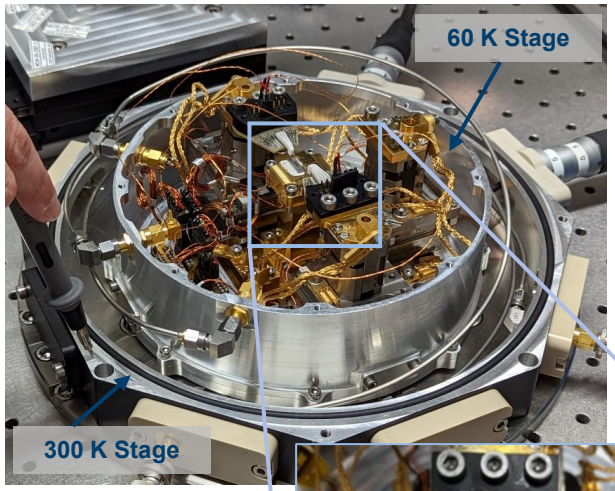
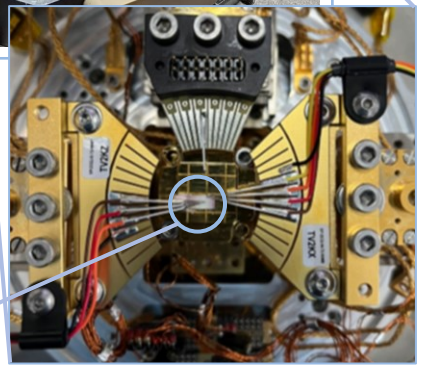
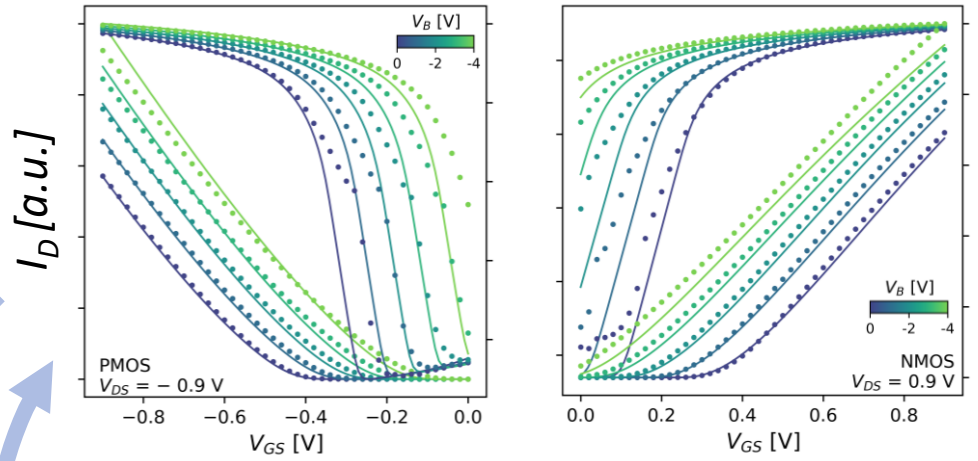
Setup @ ICA | FZJ: T_{min} ~ 7 K







Short-Channel I-V-Curves [8]



Input Data for BSIM-IMG Based Modeling

AdMOS — done by AdMOS GmbH

Cryogenic Model Library

[8] Chava, Phanish, et al. "Evaluation of cryogenic models for FDSOI CMOS transistors." 16th IEEE Workshop on Low Temperature electronics. No. FZJ-2024-05369. Zentralinstitut für Elektronik, 2024.
The QSolid project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework programme “Quantum technologies – from basic research to market” (Grant No. 13N16149).

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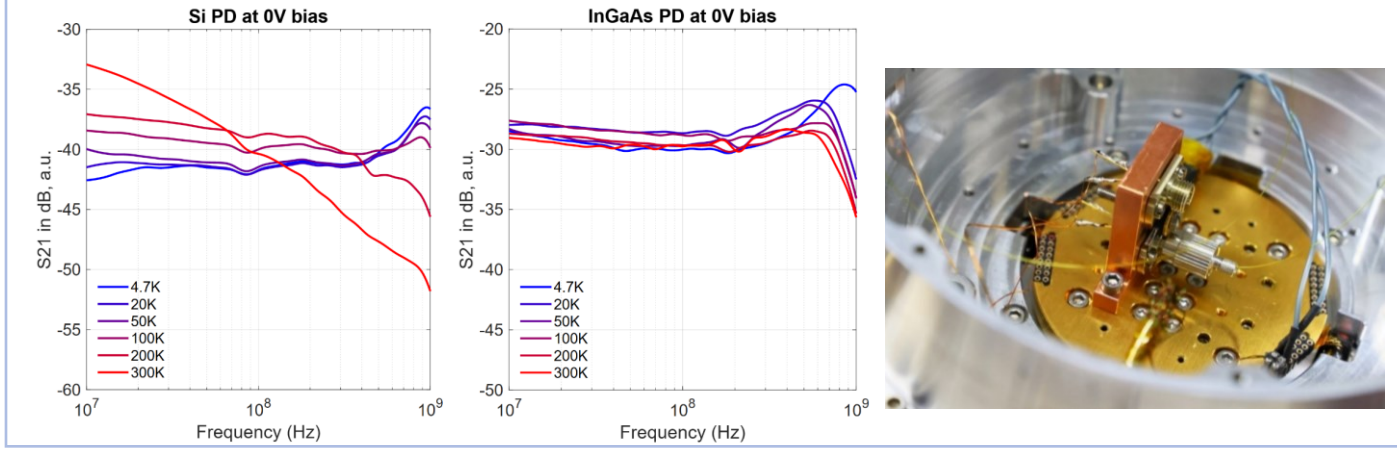
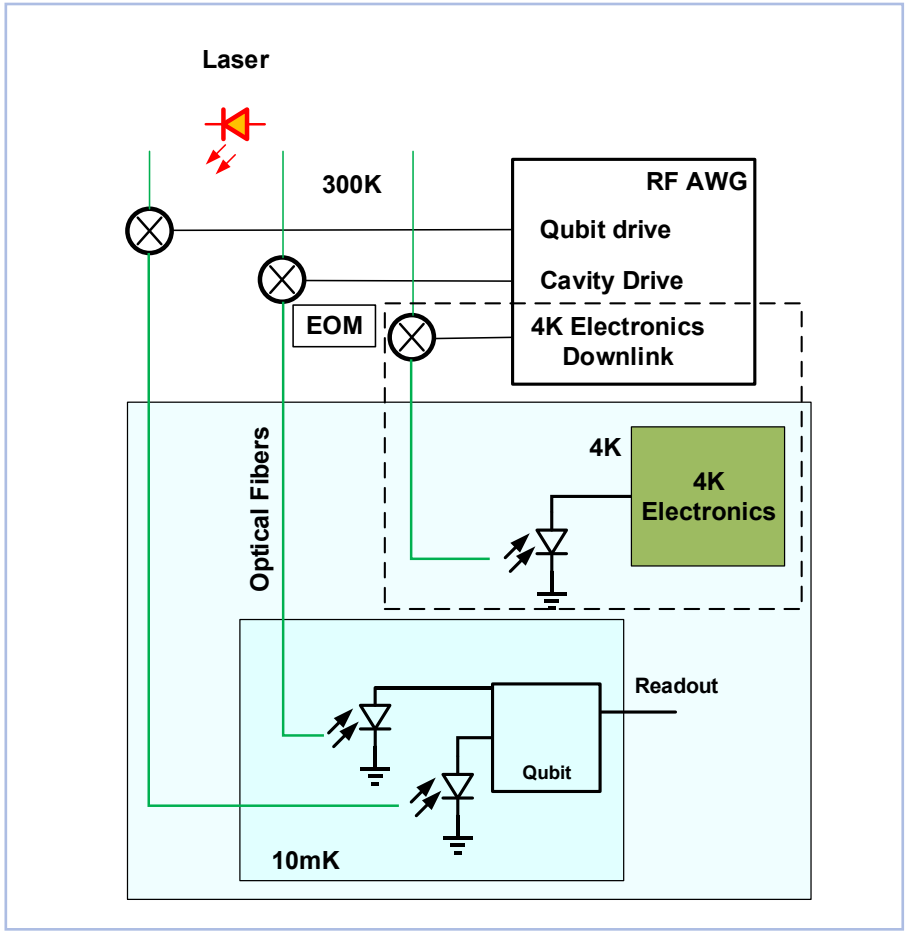
QSOLID – PHOTONIC LINK

Optical Data and Power Link to Cryo

SPONSORED BY THE
Federal Ministry of Education and Research
QSOLID

- Passive optical photodiode link as alternative approach
  - Significantly improved bandwidth & dark currents at cryo
  - Purely passive operation, no bias needed
  - Power and data communication envisioned
- Measurement with SC Qubit in Munich ongoing



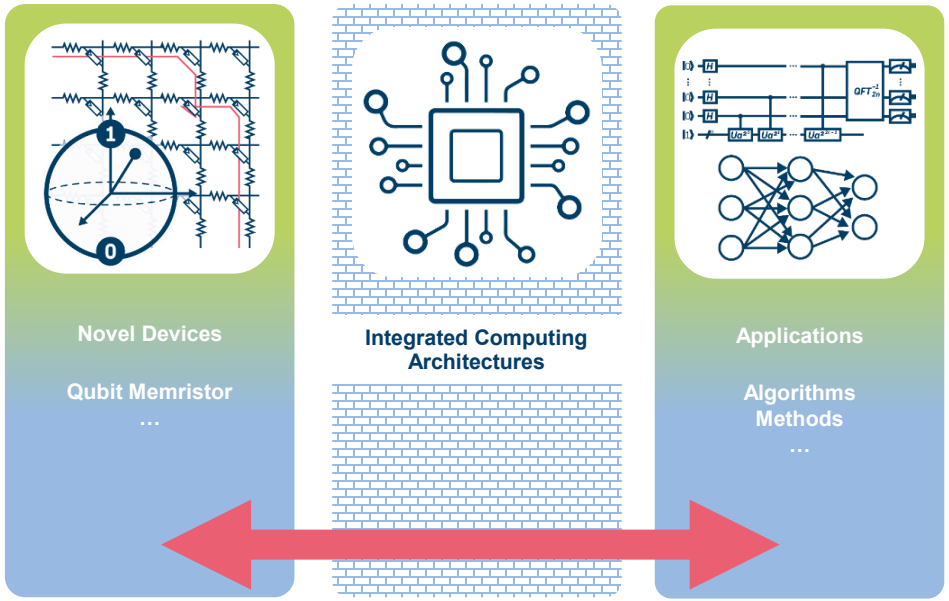


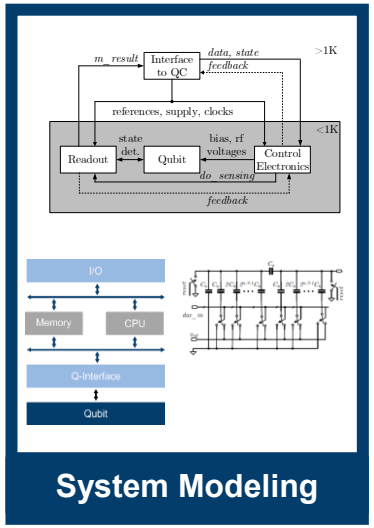
[9] S.Mutum, et. Al, "A Photonic Link at 4.7K with >1 GHz bandwidth towards an Optical Quantum Computing Interface", IEEE MTT-S International Microwave Symposium (IMS) 15-20 June 2025, Moscone Center, San Francisco, CA
The QSolid project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework programme "Quantum technologies – from basic research to market" (Grant No. 13N16149).

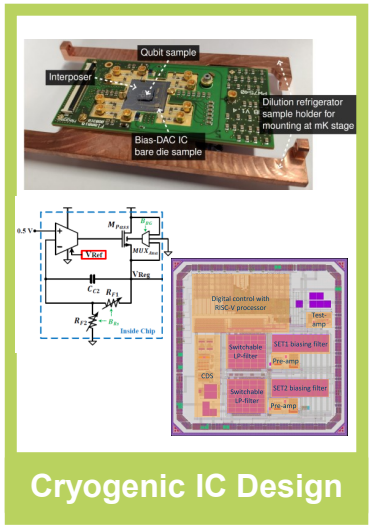
INTERMEDIATE SUMMARY

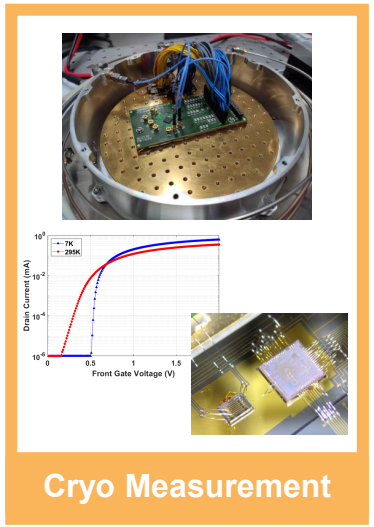
- **Integrated Computing Architectures**
  - Interface between Devices and Applications
  - Active in NC and QC

- **QC activities spanning from:**
  modeling / specification
  over design and verification
  up to system integration









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www.linkedin.com/showcase/ica-pgi4

Mastodon:

https://social.fz-juelich.de/@fzj_ica

Threads:

www.threads.com/@fzj_ica

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- [1] H. Banba et al. “A CMOS bandgap reference circuit with sub-1-V operation”. In: IEEE Journal of Solid-State Circuits 34.5 (May 1999), pp. 670–674. doi: 10.1109/4.760378.
- [2] A. R. Cabrera-Galicia, et.al, "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology," in IEEE Open Journal of Circuits and Systems, vol. 5, pp. 377-386, 2024, doi: 10.1109/OJCAS.2024.3466395
- [3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4
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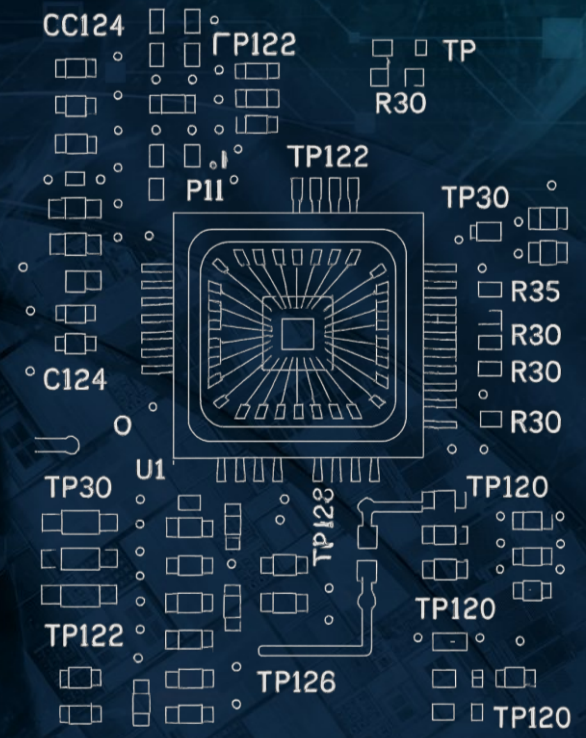
OUR ROOTS

icecirc

icecirc is a spin-off of the Institute for Integrated Computing Architectures at Forschungszentrum Jülich which:

- Has 10 years of experience in cryogenic IC design
- Employs state of the art semiconductor technology
- Has demonstrated integration of cryo electronics with qubits [1]



[1] Schreckenberg et al. "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature", 2023.