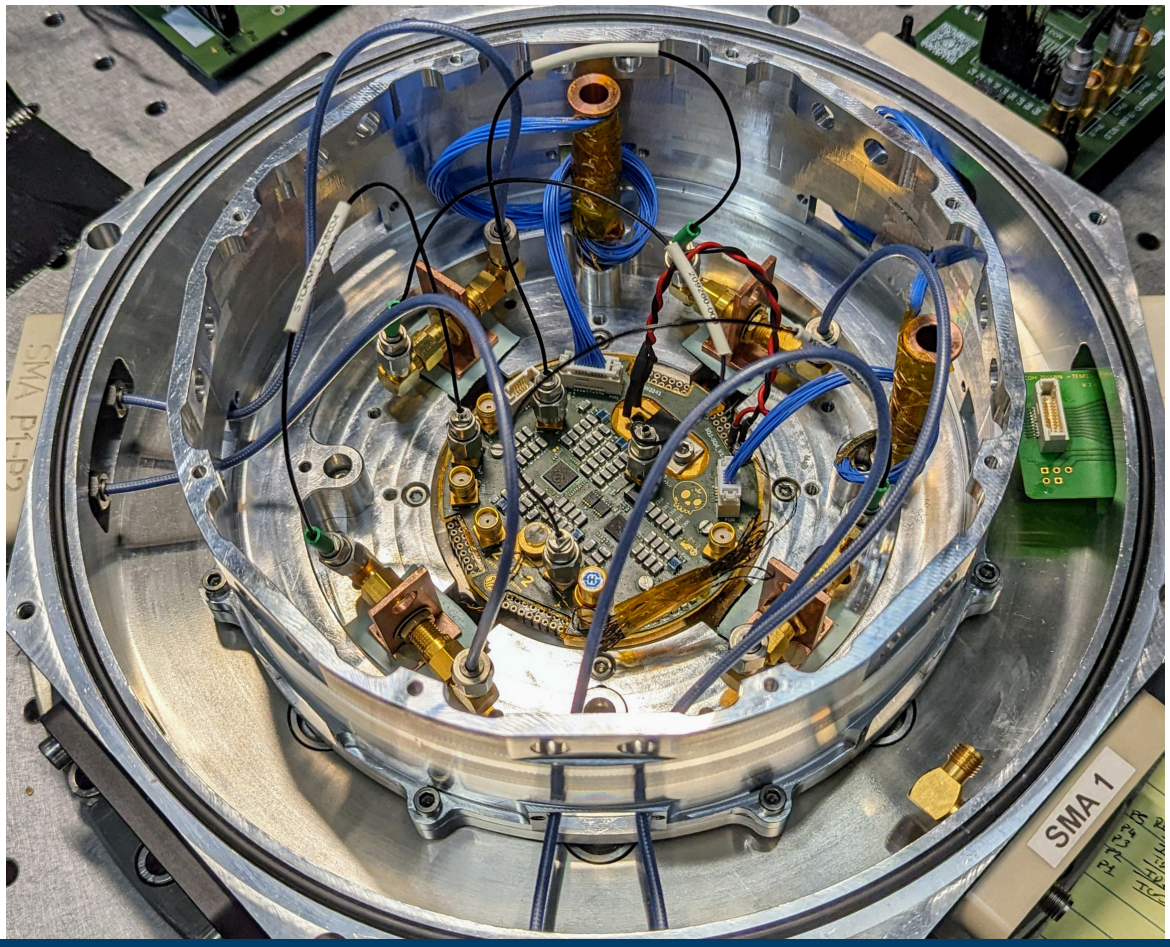

A System for the Cryogenic Power Management of Quantum Computing Electronics: Development, Integration, and Test

Alfonso Rafael Cabrera Galicia

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"Triunfar en la vida no es ganar, es levantarse y volver a empezar cada vez que uno cae."

José Mujica

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Abstract

In view of the post-Moore's law era, new computational paradigms that could serve as powerful alternatives to the classical computing are under development. One of those paradigms is Quantum Computing (QC). By using the quantum mechanical properties of superposition and entanglement via the manipulation of a large number of qubits, QC systems promise to speed up the finding of solutions to the computational challenges faced in cryptography, optimization of different processes, and quantum systems simulation. These applications position the QC systems as powerful tools for humanity.

However, the design, assembly, deployment and operation of a QC system are not simple tasks. This is because QC devices, such as superconductive qubits or semiconductor quantum dots, require an ambient temperature lower than 100 mK in order to reduce the influence of heat sources that could disrupt the qubits state information and coherence. Also, the only practical way in which a QC device can be subjected to such low temperatures is by means of a dilution refrigerator, a complex machine with limited room for Devices Under Test (DUTs), electrical connections for DC and RF signals, and cooling power.

In order to increase the QC system performance, such a system must be composed by a high number of fault-tolerant qubits. As well as by hardware and software capable of enabling its scalability. Moreover, it is expected that by incorporating cryogenic CMOS ICs as part of QC systems, the number of connections between the qubits and the Room Temperature (RT) electronics will be reduced, relaxing the dilution refrigerator requirements and allowing the system scalability. In addition, the signal integrity of the signals controlling the qubits could be improved by the shorter interface with the local cryogenic electronics based on ICs. But the most important advantage offered by CMOS IC technology is its potential integration with qubit devices. In particular, the semiconductor gate defined quantum dot, a device that stores and controls an electron operating as qubit. Thus, the development of analog, digital, and mixed-signal cryogenic CMOS ICs has attracted significant attention in the last years. As it has been demonstrated that IC technology can be an important part and key enabler of the QC systems scalability.

This work contributes to cryogenic analog MOS circuit design discipline through the development, integration and test of a cryogenic Power Management Unit (PMU) composed by a CMOS IC and additional passive components. The cryogenic PMU is developed with a 22 nm FDSOI technology, as it supplies MOSFETs that can operate at Cryogenic Temperatures (CTs) without significant performance degradation. Ultimately, the goal is to provide a regulated and low noise voltage supply to other circuit blocks located at CT environments close to 4 K, reducing the amount of DC connections between the

RT equipment and the cryogenic electronics. Hence, the QC systems scalability efforts are thereby supported.

Zusammenfassung

Angesichts der post-Moore werden neue Rechenparadigmen entwickelt, die als leistungsstarke Alternativen zum klassischen Rechnen dienen könnten. Eines dieser Paradigmen ist das Quantencomputing (QC). Durch die Nutzung der quantenmechanischen Eigenschaften von Superposition und Verschränkung mittels der Manipulation einer großen Anzahl von Qubits versprechen QC-Systeme, die Suche nach Lösungen für die rechnerischen Herausforderungen in der Kryptographie, der Optimierung verschiedener Prozesse und der Simulation von Quantensystemen zu beschleunigen. Diese Anwendungen positionieren die QC-Systeme als leistungsstarke Werkzeuge für die Menschheit.

Die Entwicklung, der Aufbau, die Installation und der Betrieb eines QC-Systems sind jedoch keine einfachen Aufgaben. Das liegt daran, dass QC-Bauelemente, wie z. B. supraleitende Qubits oder Halbleiter-Quantenpunkte, eine Umgebungstemperatur von unter 100 mK benötigen, um den Einfluss von Wärmequellen zu reduzieren, die die Zustandsinformation und Kohärenz der Qubits stören könnten. Außerdem ist die einzig praktikable Möglichkeit, ein QC-Bauelement solch niedrigen Temperaturen auszusetzen, mit Hilfe eines Mischkryostaten, einer komplexen Maschine mit begrenztem Platz für Bauelemente (DUTs), elektrischen Anschlüssen für Gleichstrom- und Hochfrequenzsignale sowie Kühlleistung.

Um die Leistung von QC-Systemen zu steigern, muss ein solches System aus einer hohen Anzahl fehlertoleranter Qubits bestehen, sowie aus Hardware und Software, die dessen Skalierbarkeit ermöglichen. Darüber hinaus wird erwartet, dass durch die Integration kryogener MOS-ICs als Teil von QC-Systemen die Anzahl der Verbindungen zwischen den Qubits und der Raumtemperatur-Elektronik (RT-Elektronik) reduziert wird, wodurch die Anforderungen an den Mischkryostaten verringert und die Systemskalierbarkeit ermöglicht wird. Zusätzlich könnte die Signalintegrität der Signale, die die Qubits steuern, durch die verkürzten Signalleitungen zur lokalen kryogenen Elektronik auf Basis von ICs verbessert werden. Der wichtigste Vorteil der MOS-IC-Technologie ist jedoch ihr Potenzial zur Integration mit Qubit-Bauelementen, insbesondere dem durch Halbleiter-Gate definierten Quantenpunkt, einem Bauelement, das ein Elektron speichert und steuert, das als Qubit fungiert. Daher hat die Entwicklung von analogen, digitalen und Mixed-Signal-kryogenen MOS-ICs in den letzten Jahren große Aufmerksamkeit erregt, da gezeigt wurde, dass die IC-Technologie ein wichtiger Bestandteil und ein Schlüsselfaktor für die Skalierbarkeit von QC-Systemen sein kann.

Diese Arbeit trägt zur Disziplin des Designs kryogener analoger MOS-Schaltungen durch die Entwicklung, Integration und Erprobung eines kryogenen Systems zur Bereitstellung des Spannungsversorgung (PMU) bei, die aus einem MOS-IC und zusätzlichen pas-

siven Komponenten besteht. Die kryogene PMU wird in einer 22-nm-FDSOI-Technologie entwickelt, da diese MOSFETs bereitstellt, die bei kryogener Temperatur (CT) ohne nennenswerte Leistungseinbußen betrieben werden können. Letztendlich ist das Ziel, andere Schaltkreise, die sich in CT-Umgebungen nahe 4 K befinden, mit einer geregelten und rauscharmen Spannungsversorgung zu versorgen, wodurch die Anzahl der DC-Verbindungen zwischen der RT-Elektronik und der kryogenen Elektronik reduziert wird. Dadurch werden die Bemühungen um die Skalierbarkeit von QC-Systemen unterstützt.

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Acronyms

AC	Alternating Current
AWG	Arbitrary Wave-form Generator
BJT	Bipolar Junction Transistor
BNC	Bayonet Neill–Concelman
BOX	Buried Oxide Insulator
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CT	Cryogenic Temperature
CTAT	Complementary to Absolute Temperature
DAC	Digital to Analog Converter
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DMM	Digital Multimeter
DNL	Differential Nonlinearity
DTMOS	Dynamic Threshold MOS
DUT	Device Under Test
DW	Digital Word
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FDSOI	Fully Depleted Silicon On Insulator
FEP	Fluorinated Ethylene Propylene
FET	Field-Effect Transistor
Ge	Germanium
GM	Gifford-McMahon
g_m	Transconductance

He	Helium
I/O	Input-Output
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
I_{Load}	Load Current
JTAG	Joint Test Action Group
L^4He	Liquid Helium
LDO	Low-Drop-Out
LF	Low Frequency
LN_2	Liquid Nitrogen
LNA	Low Noise Amplifier
LR	Load Regulation
MC	Mixing Chamber
MOS	Metal Oxide Semiconductor
MPN	Manufacturer Part Number
MRI	Magnetic Resonance Imaging
PCB	Printed Circuit Board
PDK	Process Development Kit
PEEK	Polyether ether ketone
PID	Proportional-Integral-Derivative
PMU	Power Management Unit
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
PTAT	Proportional to Absolute Temperature
QC	Quantum Computing
qubit	Quantum bit
RC	Resistor-Capacitor
RF	Radio Frequency

RLC	Resistor-Inductor-Capacitor
RMS	Root Mean Square
RT	Room Temperature
RTN	Random Telegraph Noise
SDA	Semiconductor Device Analyzer
Si	Silicon
SiO_2	Silicon Dioxide
SMA	SubMiniature version A
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SSA	Signal Source Analyzer
STI	Shallow Trench Isolation
USB	Universal Serial Bus
UTB	Ultra-Thin Body
V_{Reg}	Regulated Output Voltage
V_{Sup}	Supply Voltage
V_{th}	Threshold Voltage

Chapter 1

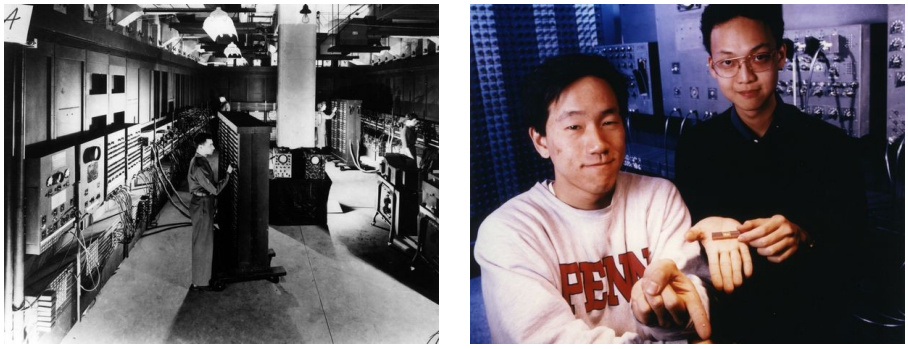
Introduction

1.1 Motivation

Nowadays most of the computing systems are based on a paradigm known as classical computing. In this paradigm the information is handled by using bits. In fact, a bit is the smallest representation of logic information, and it can represent the information as either a 0 or a 1. Furthermore, that information is processed through binary logic operations in order to perform some sort of calculation. The first classical computers were developed in the middle of the 20th century. They were large electro-mechanical machines that relied on components such as vacuum tubes and relays. These computers were able to perform basic arithmetic and logic operations. However, they were slow, power hungry and prone to failure. Perhaps the Electronic Numerical Integrator and Computer (ENIAC) is the most famous of the first classical computers [1]. A photograph of such a system is shown in Figure 1.1 (a).

Thanks to the introduction and adoption of the integrated circuit (IC), a device invented by Jack St. Clair Kilby and enhanced by Robert Noyce [2, 3], a reduction of the size and cost of the classical computers became possible. Also, their reliability and performance, have been enhanced due to the continuous improvement of the IC technology. Then, as the ICs manufacturing technology evolved, the quantity of components inside an IC increased. Hence, the computational power of classical computers using novel ICs also increased. A demonstration of this technological trend was performed in 1995 by electrical engineering students at University of Pennsylvania. They developed an IC in 0.5 µm CMOS technology, that recreates the architecture and building blocks of the original ENIAC system. In this way, the footprint of the ENIAC system was reduced from 180 m^2 to 0.004 m^2. Besides, a drastic reduction in weight and power consumption was also achieved [4]. The ENIAC-on-a-Chip system is shown in Figure 1.1 (b).

Regarding the IC technology evolution, Gordon Earl Moore pointed out that between 1964 and 1965 the amount of components (e.g., diodes, resistors and transistors) per function on ICs increased by a factor of two. Consequently, he predicted in 1965 that the number of components on ICs will double each year during the next ten years [5].



(a) (b)

Figure 1.1: (a) ENIAC system being operated in 1946. (b) Students from the University of Pennsylvania holding a functional IC containing the modules of the original ENIAC system in 1995; the IC is developed in 0.5 µm CMOS technology [8].

Later, in 1975, he adjusted his prediction to a doubling of the amount of components per IC by every two years [6]. With his prediction, commonly known as "Moore's law", Gordon Earl Moore set his expectations for the development of the IC as fundamental part of the semiconductor industry. Hence, the industry took Moore's law as a target for the constant development of new IC fabrication technologies that could keep up with it. Consequently, the transistor density (i.e. the number of transistors / mm^2) increased from 300 in 1970 to 185,460,000 by 2020. And by June 2023, the highest number of transistors in a consumer grade product is 134,000,000, belonging to the Apple M2 Ultra SoC (System on Chip); a dual-die microprocessor [7].

In order to continuously increase the transistor density, the semiconductor industry has adhered to Robert Heath Dennard et al. MOSFET scaling principles, thereby enhancing the computational power available in each new IC technology [9]. However, as transistor sizes reached the 65 nm - 40 nm range, inherent physical limitations began to emerge; e.g. the practical limit for thickness reduction of the SiO_2 gate dielectric and the increase in gate oxide current leakage. Moreover, challenges such as charge carrier mobility degradation and band-to-band tunneling have impeded further reductions of the threshold voltage (V_{th}) [10]. In addition to these physical constraints, factors such as interconnect scaling, increased heat dissipation, and the rising complexity and costs of manufacturing processes have diminished the efficiency of transistor density scaling, ultimately slowing the advancement of Moore's law and the enhancement of classical computers [11].

In view of the post-Moore's law era, heralded by the CMOS IC technology physical limits, the semiconductor industry has incorporated the use of complementary technolo-

gies that can sustain the performance gains in modern digital computational systems; e.g. multi-die heterogeneous integration, 3D integration and Si photonics. As a result, for the forthcoming technological developments the size reduction of the MOS device will no longer be the leading figure. But rather, it will be the application of different device technologies heterogeneously integrated for the development of computational architectures having optimized performance and energy efficiency [11]. Nevertheless, if humanity expects to have a continuous access to more powerful computational systems every few years during the next decades, long-term research focused on the development of novel devices and architectures is needed. Therefore, humanity must explore and develop new computational paradigms.

One of those paradigms is Quantum Computing (QC). In 1980, Paul Benioff introduced the idea of using quantum mechanics for the description of a computational process via a Hamiltonian model [12]. Later in 1981, Richard Phillips Feynman highlighted the fact that classical computers are not suited for the simulation of quantum mechanical systems due to the complexity and non-classical nature of quantum mechanics. Thus, as to find a solution to this problem, Richard Phillips Feynman proposed the usage of a computational system that could efficiently simulate quantum systems by applying quantum mechanics as its fundamental working principle; i.e. the quantum computer [13].

In a quantum computer, the quantum bit (qubit) is the fundamental unit of information. Unlike the classical bit, a qubit posses the quantum mechanical properties of superposition and entanglement. Superposition enables a qubit to represent multiple values at once. Thus, the information in a qubit can exists as a combination of two states; e.g. 0 and 1. Also, entanglement allows two or more qubits to be linked, such that the state information of one qubit is directly related to the state of another qubit. Both properties allow QC algorithms to efficiently solve certain problems that classical computers cannot [14].

Since its inception, QC has evolved and several systems have been developed [15, 16, 17]. The progress in QC has been so substantial that in 2019 a quantum processor composed by 53 qubits reached the quantum supremacy, demonstrating that a QC system can resolve a problem that no classical computer can solve in a feasible time lapse [15]. Moreover, the use of quantum physics phenomena via the manipulation of a large number of qubits performed by a QC system promises to speed up the finding of solutions to the computational challenges faced in fields like cryptography, optimization of different processes, and quantum systems simulation [18, 19]. These applications position QC systems as powerful tools with the potential to greatly benefit humanity.

However, the design, assembly, deployment and operation of a QC system are not simple tasks. This is because QC devices, like superconductive qubits and semiconductor quantum dots, need an ambient temperature lower than 100 mK for proper operation. Since, by operating these devices at deep cryogenic temperatures (CTs), the influence of

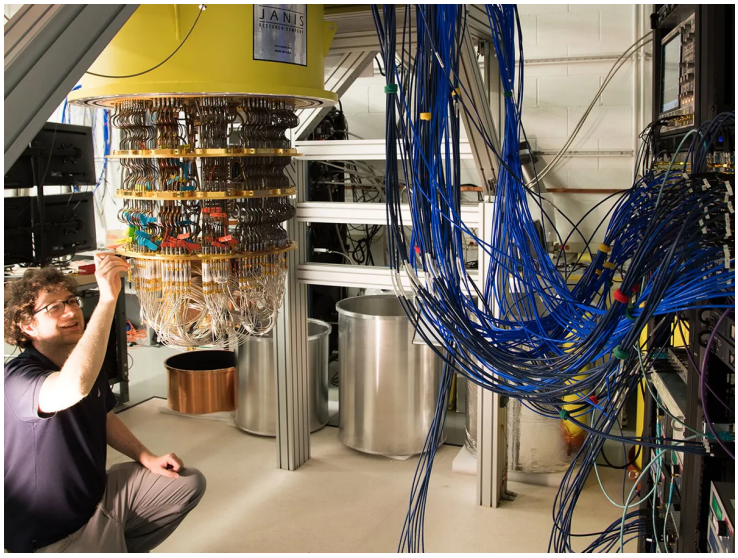


Figure 1.2: Google engineer examines his company QC system located inside the dilution refrigerator; only half of the connections feeding into the quantum processor are attached [21].

heat sources that could disrupt the qubits state information and coherence, is reduced; i.e. the lost of superposition and entanglement in a QC system is suppressed by the thermal energy reduction, achieved through a deep cryogenic cooling process of that system. Moreover, the only practical way in which a quantum processor can be subjected to such low temperatures is by means of a dilution refrigerator, a complex machine with limited room for Devices Under Test (DUTs), electrical connections for DC and RF signals, and cooling power. Figure 1.2 shows a QC system that follows this functional approach.

Furthermore, one method to increase the quantum volume, a holistic performance metric that measures the capabilities and error rates of a quantum computer, is through the construction of QC systems with a higher number of fault-tolerant qubits. Besides, the quantum volume cannot be improved by addressing just one aspect of the system, but rather it requires synergistic enhancements across all components; i.e. improvements in hardware and software [20]. Consequently, the scalability of QC systems is necessary for the development of high performance quantum computers that will serve as foundation for the production of an universal QC system.

Such a situation draws parallels with the development of the classical digital computers, as their performance has been enhanced through the scalability provided by the CMOS ICs, together with the integration of complementary technologies. Nonetheless, con-

temporary QC systems such as the one in Figure 1.2, employ control electronics located outside the dilution refrigerator at room temperature (RT). Thus, as to scale such a QC system is not only necessary to increase the number of qubits, but also the amount of electrical connections between the control electronics and the qubits. This approach set challenges for the scalability of the system due to the limited space and cooling power available inside dilution refrigerators. In addition, the qubits coherence may be affected due to an additional susceptibility to heat sources and signal integrity issues introduced by the increased amount of electrical connections.

Accordingly, as to enable the scalability of QC systems, Edoardo Charbon et al. proposed the development of cryogenic control electronics based on CMOS IC technology [22]. Since it is expected that by incorporating cryogenic CMOS ICs as part of QC systems, the number of connections between the qubits and the RT electronics will be reduced, relaxing the dilution refrigerator requirements and allowing the system scalability. Furthermore, the signal integrity of the signals controlling the qubits could be improved by the shorter interface with the local cryogenic electronics based on ICs. But the most important advantage offered by CMOS IC technology is its potential integration with QC devices. In particular, the semiconductor gate defined quantum dot, a device that stores and controls an electron operating as qubit [23].

Hence, the development of analog, digital, and mixed-signal cryogenic CMOS ICs has attracted significant attention in the last years [24, 25]. As it has been demonstrated that IC technology can be an important part and key enabler of the QC systems scalability [26, 27, 28]. Besides, the development of cryogenic CMOS ICs may benefit other sectors beyond QC since they also play a relevant role in applications such as astronomical detectors, space exploration and high-performance classical computing [29, 30, 31].

However, the ICs belonging to a QC system require a defined, stable and low noise supply voltage for proper operation [32]; e.g. the phase noise of RF oscillators is highly influenced by their power supply quality [33]. Moreover, this need will be challenging to satisfy in large scale QC systems by simply establishing a power supply bus between the power supply units (PSUs) located at RT and the ICs inside the dilution refrigerator. This is because the lines of the power supply bus can be prone to supply voltage ripples, ground loops, electromagnetic interference from neighboring lines and dynamic load currents. A solution to these issues is the employment of low noise PSUs with four-terminal sensing capability and usage of RF coaxial cables for power delivery inside the dilution refrigerator. But these approaches will not be practical in large scale QC systems [23], as the number of connections between the RT equipment and the CTs stages inside the commercial dilution refrigerators are limited and important assets. Moreover, a critical limitation to consider is the maximum heat load that electrical connections can introduce into the coldest stage of the dilution refrigerator, i.e. the mixing chamber at 100 m K - 10 m K.

As a proposed solution to the previously described issue, this work reports the research and development efforts performed for the assembly of a cryogenic Power Management Unit (PMU) composed by a CMOS IC and additional passive components. The main objective is to provide a regulated and low noise voltage supply to other circuit blocks located at CT environments close to 4 K, reducing in this way the amount of DC connections between the RT equipment and the cryogenic electronics.

For the development of the cryogenic PMU presented in this work, a 22 nm Fully Depleted Silicon On Insulator (FDSOI) technology is selected, as it supplies MOS transistors that can operate at CTs without a significant performance degradation [34, 35]. Also, the 22 nm FDSOI technology provides a V_{th} tuning functionality through the MOS transistor back-gate terminal [36]. Such a functionality allows the V_{th} reduction of the MOS transistors at CTs. Therefore, by setting $\mathrm{V_{th\ @7K}} \approx \mathrm{V_{th\ @297K}}$ via the transistors back-gate potentials, an enhancement of the design capabilities and overall power consumption reduction of the cryogenic electronics can be achieved. Thus, a DC characterization of this technology is reported for the 7 K - 300 K range; this characterization lower temperature is 7 K due to the empoyed GM cryocooler cooling power capability.

Similarly, the design and cryogenic electrical characterization of the main PMU components, a voltage reference and a linear voltage regulator, are presented. Moreover, the impact that MOS transistor cryogenic phenomena have over these circuits is reported. In particular, attention is placed on the cryogenic V_{th} saturation, the transconductance (g_{m}) increase and the low frequency (LF) excess noise. The experimental results indicate that the cryogenic V_{th} saturation and the g_{m} increase can be used as circuit design tools, while the LF excess noise is a performance handicap for cryogenic analog circuits. Additionally, an electronic system is presented as an application case: the cryogenic power-up of a voltage reference circuit used by a Digital to Analog Converter (DAC) via a PMU. This system is used for the study of the cryogenic multi-die heterogeneous integration, as well as the cryogenic electronics sensitivity to the electrical noise.

In the end, it is expected that the information and outcomes provided by this work support the advancement of the cryogenic analog MOS circuit design discipline. And perhaps, in the future, the development of new tools will follow.

1.2 Structure of This Work

After the introductory chapter, this work follows the next structure:

- Chapter 2 provides a description of the cryocoolers commonly used in the development of cryogenic electronics for QC applications. The cryocooling system employed in this work is also described. Moreover, the factors degrading the power integrity of

the cryogenic electronics are listed and described. Then, the development of cryogenic PMUs for power integrity enhancement of the cryogenic electronics is proposed.

- Chapter 3 describes the MOS transistors available in the 22 nm FDSOI technology. Furthermore, the measurement results obtained from a DC characterization of this technology at CTs are presented; the characterization outcomes served as reference for the design of a cryogenic PMU. The endeavours followed for the development of cryogenic simulations models are also addressed.

- Chapter 4 presents the design and cryogenic electrical characterization of a voltage reference and a linear voltage regulator at temperatures between 6 K and 300 K. Both circuits are used as evaluation circuits for the experimental performance evaluation of the 22 nm FDSOI technology when used as platform for the development of cryogenic analog circuits. Additionally, the development of a cryogenic PMU composed by the analog circuits studied in this chapter is proposed.

- Chapter 5 presents an application case of the cryogenic PMU addressed in Chapter 4: a cryogenic multiple ICs system. Additionally, this chapter reports the use of EMC techniques for the improvement of the signal and power integrity of the multiple ICs system when it is cooled by a GM cryocooler. Also, the efficiency of the EMC techniques is evaluated. In this way, a cryogenic heterogeneous integration between the electronics and the GM cryocooler is proposed in order to achieve an accurate, repeatable, and extrinsic noise-free performance test of the cryogenic electronics.

- Chapter 6 provides the final remarks and conclusions reached in this work, as well as a perspectives for future research activities.

Chapter 2

Power Integrity Challenges in Cryogenic Electronic Systems

Power integrity refers to the ability of a power distribution system to provide stable electrical power to the components of an electronic circuit. Thus, by maintaining the power integrity, it is ensured that the power distributed to the system components remain within acceptable voltage or current ranges, with minimal electrical noise and interference. Moreover, as to achieve power integrity in cryogenic electronics, it is necessary to know the characteristics of the environment where such systems are intended to be operated.

In consequence, the first part of this chapter provides a description of the cryogenic cooling systems commonly used for the development of cryogenic electronics for QC systems. Thereafter, the cryocooling system used in this work is described. In addition, the physical factors that can degrade the power integrity of the cryogenic electronics are listed and described. Finally, the development of cryogenic power management units for the enhancement of the power integrity of cryogenic electronics in QC systems, is proposed.

2.1 Cryogenic Cooling Systems

Although in QC applications the preferred cooling system is the dilution refrigerator, for an initial cryogenic electrical test of ICs based on CMOS technology, it may not be the most convenient approach. This due to complexities associated with the operation and setup of dilution refrigerators. From another perspective, if the evaluation of an IC is required at the 1 K-300 K range, other cooling approaches such as immersion cooling or closed cycle cryocoolers can be employed. The next subsections provides a brief description of such cooling approaches.

2.1.1 Immersion Cooling

A simple way to test an electronic system at CTs is by means of the sample immersion into a cryogenic liquid coolant. In this approach the sample is mounted at the end of a dipper probe and immersed into the coolant placed inside a cryogenic storage dewar, as illustrated in Figure 2.1. The sample immersion provides efficient cooling, independently of the sample shape. In addition, immersion provides high cooling power at low temperatures according to the cryogenic liquid coolant at use; e.g. 1 L of Liquid Helium (L^4He) can absorb more than 2500 Ws at 4.2 K [37].

In cryogenics, some of the most common cryogenic liquid coolants are Liquid Nitrogen (LN_2), L^4He and ^3He. At a pressure of 1 atm, the boiling temperature of LN_2 is 77.355 K, while the boiling temperature of the L^4He is 4.23 K. It is also possible to change the temperature of a sample immersed in L^4He by vacuum pumping the vapor space over the liquid coolant or by pressurizing the dewar up to 2 atm; a range of 1 K-5 K can be obtained. However, when pressurizing, it is generally best not to go above 2 atm due to the risk of blowing up the storage dewar. Alternatively, by changing the height of the dipper probe above the liquid coolant, the sample holder temperature can be modified due to the temperature stratification that occurs in the vapor space [37]; e.g. a range of 4.23 K-250 K can be obtained [38].

Moreover, the lighter isotope of helium, ^3He, has a boiling temperature of 3.1905 K at 1 atm and it can reach sub-Kelvin temperatures at low pressures; e.g. around 0.45 K at 98.7 µatm. However, ^3He is not an abundant material on Earth and it is mainly obtained through industrial processes; e.g. in the United States the federal government produces tritium for the assembly of nuclear warheads, where ^3He is a by product obtained from the tritium decay [39]. Besides, neutron detection commonly uses ^3He as reactive agent;

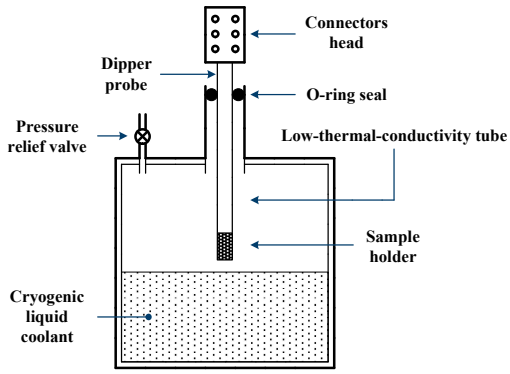


Figure 2.1: Cryogenic immersion cooling via a dipper cryostat.

neutron detection finds application in particle physics, material science and security detection systems for radioactive materials. Consequently, the market price of ^{3}He is higher than the ones of L^{4}He and LN_2.

Due to its physical characteristics, L^{4}He has become a popular coolant in sectors such as low temperature physics, chemistry, life-sciences experiments, medical MRI, aerospace and semiconductor manufacturing. However, the market price of L^{4}He has severely increased in the last decade due to higher demand and supply shortfalls [40]. This situation has encouraged many research labs to employ L^{4}He recovery and liquefaction systems in order to reduce operation expenses [41]. Moreover, since the dipper cryostats used in cryogenic immersion require a constant replenish of L^{4}He, due to L^{4}He evaporation and unintended release out of the dewar during normal operation, it is expected that in future the immersion cooling with L^{4}He will become an inconvenient approach, at least from the economics perspective of a small research lab.

2.1.2 Gifford-McMahon Closed Cycle Cryocooler

On the other hand, the use of cooling systems based on cryocoolers with Helium (He) gas circulating in a closed-cycle has become an attractive alternative for research labs seeking to perform cryogenic experiments with low cooling power requirements. And, despite the fact that cryocoolers require He gas to operate, ideally they do not lose it and do not need a constant replenish, in contrast to the L^{4}He requirements of dipper cryostats used in immersion cooling. Therefore, the operation costs of closed-cycle cryostats are expected to be lower than the ones of dipper cryostats using L^{4}He.

Different types of closed-cycle cryocoolers have been developed, being the most popular the Stirling, the pulse tube and the Gifford-McMahon (GM) [42]. Since this work is executed using a cooling system based on a GM cryocooler, in the following this kind of cryocooler will be described.

A descriptive view of a two stages GM cryocooler is shown in Figure 2.2. Its main parts are the He gas compressor and the cold head. The compressor provides a supply of compressed He and a low pressure return path for the gas coming out of the cold head. The inflow and outflow of gas is controlled by the compressor, or an alternative driver, via the rotary valve-motor. In the cold head, two stages with different temperature are enclosed by a vacuum shroud. Moreover, a second compressor generates a vacuum space in order to limit the heat load associated with the air or any other gas remaining inside the shroud; without a proper vacuum space the cold head stages cannot reach their optimal temperatures.

The first stage usually has a temperature close to 70 K and acts as a thermal anchor for the radiation shield that covers the second stage. In this way the second stage is isolated from the room temperature radiation emitted by the vacuum shroud. The second stage

of a commercial GM cryocooler can reach temperatures between 4.5 K and 5.5 K, while its cooling power can be in the range of 0.5 W to 2 W. The temperature and cooling power of the GM cryocooler stages are governed by the characteristics of the material used in the construction of the regenerator-displacer parts, in specific the heat capacity [43]. Once the cryocooler has completed its cooling down sequence and their stages have reached their base temperatures, the coldest area in the system will be the cold finger. It is in this area where the DUTs are usually placed via a sample holder.

The GM cryocooler is classified as a regenerative cooler. In these systems the working fluid is moved and compressed at oscillating flows and pressures during a Stirling like cooling cycle. The GM cooling cycle consists of four states in which the regenerator-displacer is moved pneumatically by an internal pressure differential of the He gas.

The first state of the cooling cycle starts with the rotary valve-motor opening the compressed (high pressure) He supply, allowing the gas to pass through the regenerator material and reach the expansion space at the top of the cooling stage. During this process the regenerator absorbs and holds the heat carried by the incoming gas flow. In the second state the pressure differential moves the regenerator-displacer part down, allowing the gas to expand and cool. Then, the cooling effect is produced.

During the third state the rotary valve-motor closes the high pressure gas flow and opens the low pressure return path. Therefore, the cold gas flows through the regenerator material. In this way the gas leaving the cooling stage takes out the heat stored by the regenerator-displacer part during the first cooling state. As a consequence, heat is removed from the system. In the last state, due to the pressure difference produced by the discharge of gas, the regenerator-displacer part moves back to its initial position. At this point the cooling cycle is completed.

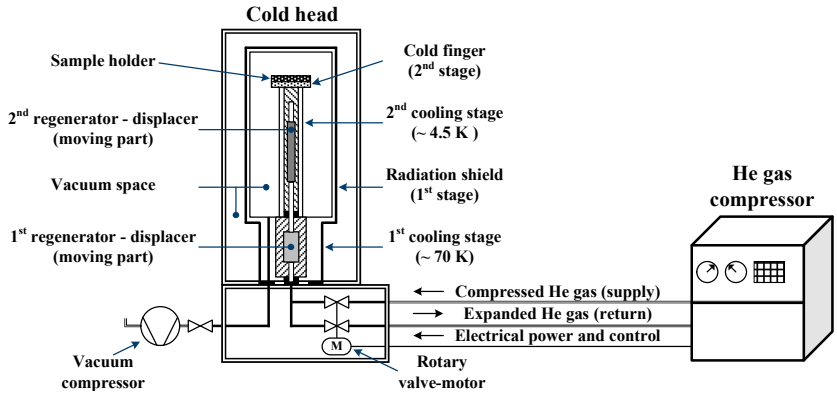


Figure 2.2: Two stages Gifford-McMahon (GM) cryocooler.

By repeating the cooling cycle, heat is constantly removed from the system until the cooling stages have reached their base temperatures. Is important to mention that the cooling cycle is also repeated during cryogenic experiments, in order to maintain the base temperature of the cooling stages. Moreover, the GM cooling cycle can be automated by means of an electronic control system. Consequently, one of the main advantage of GM cryocoolers is its convenience [37].

Conversely, the cooling down sequence requires a long time to reach the base temperature; e.g. 12 h. Additionally, a proper installation and thermalization of the DUT and its electrical connections, must be assured for proper sample cooling. Moreover, due to the movement of the regenerator-displacer parts, GM cryocoolers produce significant vibrations in the cold head; e.g. 100 µm amplitude and 9.81 m/s^2 acceleration. For some applications, this amount of vibration noise is unacceptable and vibration damping elements must be added to the setup. Other requirements of GM cryocoolers are electrical power for its electromechanical elements and cooling water supply for the He gas compressor [37, 42].

Finally, to set the DUT at different temperatures is common practice to place a heater resistor on the cold finger. In this way electrical power is dissipated as heat by the resistor, and if it is higher than the cryocooler cooling power, then the cold head temperature increases. The temperature of the cryocooler stages can be monitored by diode temperature sensors or resistor temperature sensors. In order to settle the cold finger to a stable temperature, an electronic PID controller is employed. This controller uses the heater resistor as actuator and the temperature sensor as feedback element. Therefore, with a PID controller, the GM cryocooler can offer at its cold finger a temperature range of 5.5 K-310 K [44].

2.1.3 Dilution Refrigerator

The dilution refrigerator, also known as ^{3}He-^{4}He refrigerator, is the only continuous refrigeration method capable of reaching temperatures lower than 0.3 K. And, currently is the most important refrigeration technology for the 5 mK-1 K temperature range. Its development started in the early 1950's, when Heinz London proposed the use of the heat of the mixing of two He isotopes to obtain low temperatures. Later, in 1965 a research group at Leiden University built the first refrigerator based on this principle, reaching a temperature of 0.22 K. Thereafter, in 1966 Oxford Instruments developed the first commercial dilution refrigerator together with Heinz London [45, 46]. By using Figure 2.3, a simplified description of a dilution fridge cooling cycle is next provided.

In the Mixing Chamber (MC), two phases of the ^{3}He-^{4}He mixture, the concentrated phase (100 % of ^{3}He) and the diluted phase (6.6 % of ^{3}He and 93.4 % of ^{4}He) are in equilibrium and separated by a phase boundary. Inside the MC, the ^{3}He is diluted as it flows

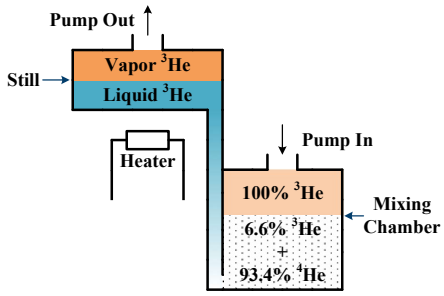


Figure 2.3: Endothermic flow of ^{3}He across the ^{3}He-^{4}He mixture allocated in the Mixing Chamber (MC), and its subsequent removal via a distilling process in the Still.

from the concentrated phase through the phase boundary into the diluted phase. The heat necessary for this dilution is the useful cooling power of the refrigerator, as the process of moving the ^{3}He across the phase boundary is endothermic and removes heat from the MC environment. The cooling power associated to this process is given by the enthalpy difference between the concentrated and diluted phases. As to remove only ^{3}He from the diluted phase, the MC is connected to a distiller element, also known as Still. The Still distils ^{3}He from the ^{4}He via a vapor pressure difference. In this process, heat is applied to the Still via an electrical heater. Subsequently, the ^{3}He is converted into vapor and taken out of the Still via a pumping system. In this way, ^{3}He is circulated along the fridge and the cycle is repeated [45, 46, 47].

From a technical perspective, a dilution refrigerator is a complex machine. This is because it employs three cooling circuits to reach sub-Kelvin temperatures. The circuits are the LN_2 circuit, the pulse tube circuit and the MC circuit. The LN_2 circuit pre-cools the dilution unit, while the pulse tube circuit maintains the temperature of the 50 K and 3 K stages. In the MC circuit, the dilution cooling cycle occurs. The liquids and gases employed by the LN_2 and MC cooling circuits, are controlled by a handling unit. Moreover, depending of the dilution refrigerator assembler, this unit may also control the vacuum space generation inside the system. In addition, the gas flow in the pulse tube circuit is controlled by a dedicated He compressor, as in GM cryocoolers.

For the purposes of this work, it is relevant to identify the temperature stages that comprise a dilution unit. Accordingly, the dilution unit of the CF-CS110-1500M-2PT system produced by Leiden Cryogenics, is shown in Figure 2.4 [48]. Most of the experiments seeking to test MOS based ICs at CTs place the DUTs on the 3 K stage. In contrast QC experiments place the DUTs such as quantum dot devices or super conductive quibits on the MC stage, since sub-Kelvin temperatures are needed for an optimal operation of the QC devices. Also, this distribution is governed by the limited amount of cooling power

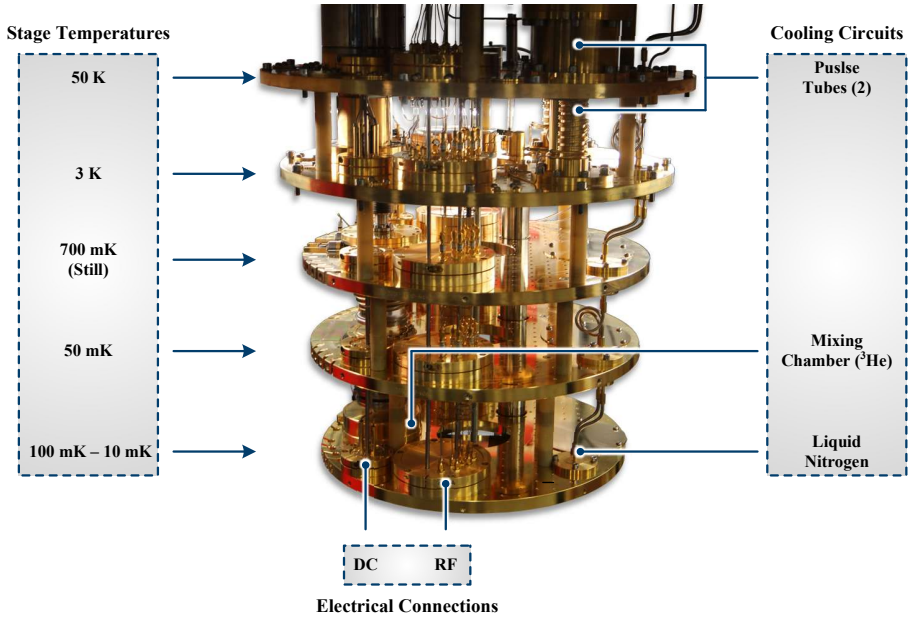


Figure 2.4: Dilution unit of the CF-CS110-1500M-2PT system; Leiden Cryogenics [48].

available in the MC, which is a function of the stage temperature. For example, if the MC temperature is 0.1 K the available cooling power is 1.5 mW, and if the temperature is 20 mK the available cooling power is around 36 µW. Since a power dissipation of 36 µW can easily be exceeded by a simple MOS circuit, ICs are commonly allocated on the 3 K stage where the available cooling power is higher and in the range of 1 W to 2 W due to the pulse tube cooling circuit [49].

As to electrically link the DUTs inside the dilution unit with the lab equipment at RT, DC and RF connection buses are used. The DC bus consists of several twisted wire pairs made of CuNi (1.6 Ω/m) or NbTi (super conductive alloy with critical temperature of 10 K, used for connections between the Still and the MC stages). In the case of the RF bus, it is comprised of semi-rigid coaxial cables made of CuNi (5.5 Ω/m). Moreover, each of the connection buses is mechanically anchored to each of the temperature stages for proper thermalization.

A dilution refrigerator also requires a dedicated supply of cooling water, electrical power, lab space and support peripherals; e.g. control computer, vibration dampers, insertable probe, super conductive magnets, LN_2 dewars, motorized lifting table or shielding cans [48]. Deeper details regarding the complex interactions between all the components of a dilution refrigerator and its operation, can be found in the specialized literature [45].

2.2 Cryocooling System Used in this Work

This section provides a brief description of the attoDRY800, the commercial cryocooling system used for the development of the low temperature electrical tests presented in this work. Produced by attocube systems AG, the attoDRY800 is a GM cryocooler adapted for the effortless execution of cryogenic electrical experiments [50]. An advantage offered by this system is its automated temperature control functionality. It must be mentioned that this system operates with the principles described in section 2.1.2.

The components of the cryocooling system are shown in Figure 2.5. The He compressor and cold head are the backbone of the attoDRY800 system. Both are manufactured by Sumitomo Heavy Industries, Ltd.; compressor MPN: CNA-11C and cold head MPN: RDK-101E [51]. Due to its audible noise production and cooling water requirements, the He compressor is separated from the cold head by approximately 12 m. These elements are mechanically and electrically connected through a pair of armored hoses that transport the He gas; potentially leading to the production of ground loop electrical noise, since the physical ground points of both elements are different.

The operation of the He compressor and the rotary valve motor inside the cold head is governed by attoDRY controller (digital system embedded in the cryogenic test station) via the attoDRY compressor controller (driver circuit). Regarding the cold head, it is mounted into a pneumatically damped table whose dampers effectively nullify the mechanical vibrations intrinsic to the cold head operation. Also, it is worth mentioning that the cryogenic test station also houses the compressors that produce the vacuum environment needed for the GM cryocooler operation.

As shown in Figure 2.6, the sample space area available in the coldest segment of the system, the quasi-circular sample holder, is around 4417.9 mm^2. While its lowest temper-

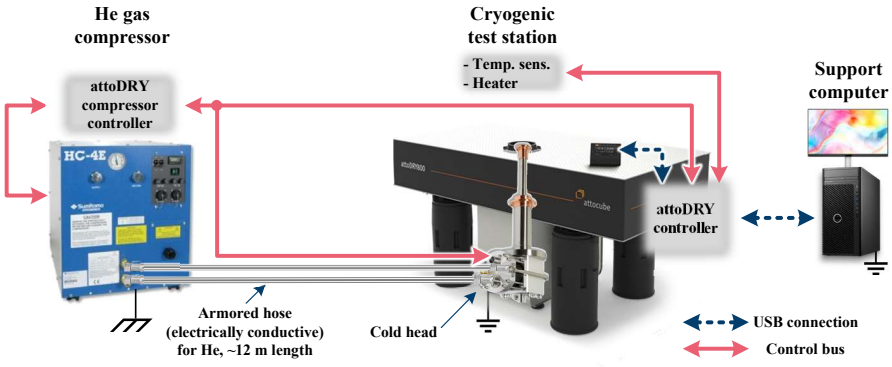


Figure 2.5: Depiction of the attoDRY800 cryocooling system set-up [50, 51].

ature is in the 5.5 K-6 K range, according to the thermal load applied to the cryocooler. As to monitor the sample holder temperature, a sensing Si diode (DT-670 from Lake Shore Cryotronics, Inc. [52]) attached under the sample holder, is employed. Moreover, a heating resistor driven by the attoDRY controller is used to increase the sample holder temperature, by dissipating electrical power as heat and increasing the thermal load applied to the cryocooler. In this way, the test of DUTs over the 6 K-300 K range is achieved. Under normal operation, the sample holder is covered by a radiation shielding shroud that is mechanically linked to the GM cryocooler first stage. Thus, its temperature is approximately 70 K during operation.

Regarding the electrical interface between the DUT inside the cryocooler and the measurment equipment at RT, a set of DC connections and RF semi-rigid coaxial cables are provided by the default attoDRY800 configuration. The DC set is composed by 30 twisted pair lines that are thermalized[1] to the first and second stages of the system via mechanical anchoring. Once the DC lines reach RT, they are confined into Fischer cables with a length of 5 m.

In order to interface with the Fischer connectors, a breakout box with BNC connectors is provided by the default attoDRY800 configuration. Concerning the RF cables, they are also anchored to the system stages for thermalization purposes. However, their distance to the RT is shorter thanks to feedthrough interfaces build in the outer shroud of the system. As a consequence, the distance between the sample holder space and RT is

[1] Thermalization refers to the process of ensuring that a component, such as a cable or circuit, reaches thermal equilibrium with its environment. In the case of the electrical connections in the attoDRY800 system, this is achieved by mechanically anchoring the cables to the first and second stage.

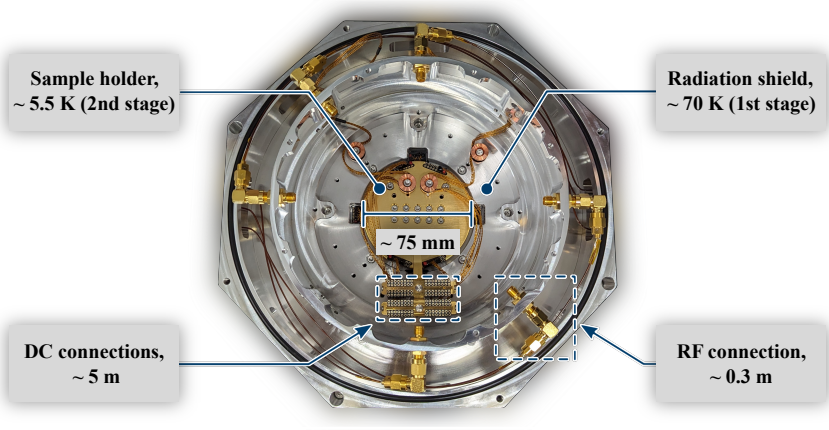


Figure 2.6: Sample space and electrical connections inside the attoDRY800 system.

around 0.3 m via the RF connections. Further details regarding the attoDRY800 system operation are provided through the thesis of A. Artanov [44].

2.3 Power Integrity Challenges

As to maintain the power integrity of a cryogenic electronic circuit employed in QC systems, it is necessary to understand which factors can degrade it. In the following a description of those factors is provided.

2.3.1 Electrical Noise in Cryogenic CMOS ICs

In electronic systems, noise is defined as any electrical signal present in a circuit other than the desired signal [53]. Noise is usually considered as an undesired phenomenon since it can disrupt the operation of a circuit, becoming then an interference. A harsh fact for circuit designers, instrumentation engineers and system integrators is that noise signals cannot be eliminated. But, the magnitude of the noise signals can be reduced until they no longer severely interfere with the circuit operation [53]. By doing such a reduction, an increase in the ratio between the circuit signal power and the noise signal power is obtained. Such a quantity is known as Signal-to-Noise Ratio (SNR).

The SNR of a circuit can be enhanced by the application of low noise circuit techniques during its design phase and Electromagnetic Compatibility (EMC) techniques at its system integration phase. However, a single unique solution to most of the noise problems does not exist [53]. Moreover, to identify a noise source and minimize its interference over a circuit is not an easy task. This is because noise can be found everywhere, in and out of an electronic system. As a consequence, noise is considered by some as **"the last barrier in circuit design"**, since all of the analog circuits (e.g. amplifiers, radio frequency transceivers and power managements systems) can be susceptible to noise or able to emit noise [54].

From the perspective of a circuit, a noise source can be classified according to its origin as an intrinsic noise source or as an extrinsic noise source. Intrinsic noise is produced by a physical mechanism intrinsically related to the working principles of the circuit components; e. g. the thermal noise produced by a resistor. In contrast, extrinsic noise is produced by a physical mechanism external to the circuit; e. g. electromagnetic waves emitted by a neighboring radio transmitter. Both kind of noise sources must be understood and their impact evaluated for the proper development of cryogenic electronic systems that are intended to operate in conjunction with RT electronics, cryogenic refrigerators and qubit devices. In the following, a review of the most relevant noise sources in the development of cryogenic electronic systems is presented.

2.3.1.1 Intrinsic Noise Sources

Most of the current state of the art cryogenic electronic systems rely on the use of IC technology based on MOSFETs, as they possess the required characteristics for the development of cryogenic electronic systems, especially in the field of QC. These characteristics are the high level of integration, low power consumption and proven operation capability at CTs [22].

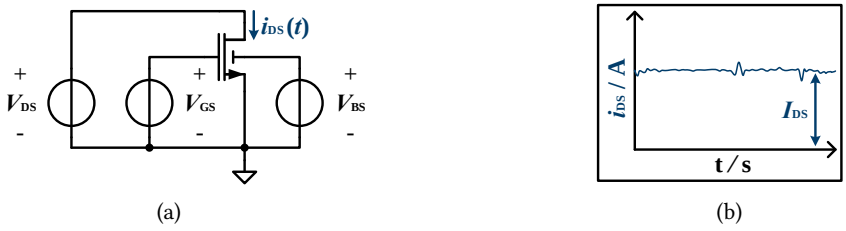
Due to the MOS transistor importance, a review of the intrinsic noise produced by the MOSFETs with an emphasis on its CT behavior, is provided. However, in order to deliver a comprehensive perspective, concepts like MOS transistor intrinsic noise, power spectral density and RMS noise, are established. Subsequently, the distinctive noise sources contributing to the MOS transistor intrinsic noise are considered.

For those purposes, a time dependent representation of the drain to source current of the NMOS transistor can be set as indicated by Eq. (2.1) [55].

$$i_{DS}(t) = I_{DS} + i_n(t) \tag{2.1}$$

Assuming that the NMOS transistor terminals are biased with DC noiseless voltage sources, as shown in Figure 2.7 (a), and that the device leakage currents are irrelevant, it is expected that a constant current I_{DS} flows between the drain and source terminals of the device. Nevertheless, I_{DS} will be in reality accompanied by a tiny current fluctuation $i_n(t)$, as sketched in Figure 2.7 (b).

It is important to mention that the instantaneous values of $i_n(t)$ cannot be predicted due to its random nature. In contrast, the average power of $i_n(t)$ can be calculated if the signal is observed for a long enough period of time T, as indicated by Eq. (2.2); taking the consideration that the current fluctuation is a stationary process [54]. Beyond this information, not much else can be extracted from $i_n(t)$ in the time domain.



(a) (b)

Figure 2.7: (a) NMOS transistor biased with noiseless DC voltage sources. (b) Drain to source current (I_{DS}) from the NMOS transistor in (a), together with its intrinsic current noise (i_n).

$$P_{\text{ave}} = \lim_{T\to\infty} \frac{1}{T} \int_0^T V_{DS} \cdot i_n(t)\, dt \tag{2.2}$$

However, much more information can be found in the frequency domain by means of the Fourier transform of the autocorrelation function of $i_n(t)$, thereby obtaining its spectrum $S_i(f)$. It is in this way that the spectrum of any signal, random or not, is defined as the energy carried by the signal at each frequency. A rigorous definition of the Fourier transform of the autocorrelation function and its application to the study of random signals can be found in [56].

Furthermore, in signal processing theory, the spectrum of a noise signal is commonly designated as Power Spectral Density (PSD) [54]. The PSD can be reported in terms of A^2/Hz or V^2/Hz, according to the physical magnitude of the noise signal. The importance of the PSD comes from its application into the signal processing theorem expressed by Eq. (2.3). This theorem indicates that if the spectrum of a signal $S_X(f)$ is applied to a linear time invariant system $H(s)$, for which $H(s = 2\pi jf) = H(f)$, the spectrum of the output signal $S_Y(f)$ will be directly shaped by the system transfer function $H(f)$ [57].

$$S_Y(f) = S_X(f)\,|H(f)|^2 \tag{2.3}$$

The spectrum-shaping theorem in Eq. (2.3) is commonly used in MOS transistor noise characterization to produce a spectral voltage noise representation $S_v(f)$ referred to the input port of the transistor under test; $S_v(f)$ is also known as equivalent input noise voltage [55]. This quantity represents the amount of noise voltage needed between the gate and source terminals of a noiseless transistor to produce the same spectral current noise that have being measured at its output port. In this case, the drain to source noise current $S_i(f)$. Therefore, if it is assumed that the transistor transfer function depends only on its g_m, $S_v(f)$ can be defined as expressed by Eq. (2.4).

$$S_v(f) = \frac{S_i(f)}{{g_m}^2} \tag{2.4}$$

Also, an alternative representation of the low frequency MOS transistor noise is the normalized drain current spectral density $(S_i(f)/{I_D}^2)$, as in Eq. (2.5), since it is strongly correlated to $(g_m/I_D)^2$ at 4.2 K, 77 K and 300 K [58].

$$S_i(f)/{I_D}^2 = S_v(f) \cdot (g_m/I_D)^2 \tag{2.5}$$

It must be mentioned that the equivalent input noise voltage is not a physical quantity that can be measured from an electronic device, but rather a quantity that allows the

noise performance comparison between different devices; e.g. by means of the SNR referred to their input ports. Moreover, it is common to find in the state of the art that the PSD of MOS devices is reported in terms of their $S_{\mathrm{i}}(f)$ or $S_{\mathrm{v}}(f)$. In this sense, as long as the g_{m} of the evaluated device is also reported, both spectra must communicate the same information.

Another important and useful concept is the mean square value of the PSD, $\overline{x_{\mathrm{n}}^2}$. This quantity is basically the integral of the noise spectrum $S_{\mathrm{v}}(f)$ over the frequency bandwidth (BW) set by $f_2 - f_1$. Moreover, in the case of noise current it is identified as $\overline{i_{\mathrm{n}}^2}$ and as $\overline{v_{\mathrm{n}}^2}$ for the case of the noise voltage. Another way in which the PSD can be represented is by means of the noise amplitude spectral density $X_{\mathrm{n}}(f)$, which is the square root of PSD ($X_{\mathrm{n}}(f) = \sqrt{S_{\mathrm{v}}(f)}$) and it is given in units such as $\mathrm{A}/\sqrt{\mathrm{Hz}}$ or $\mathrm{V}/\sqrt{\mathrm{Hz}}$. Thus, $\overline{x_{\mathrm{n}}^2}$ can be defined as indicated in Eq. (2.6) [55].

$$\overline{x_{\mathrm{n}}^2} = \int_{f_1}^{f_2} S_{\mathrm{n}}(f)\, df = \int_{f_1}^{f_2} {X_{\mathrm{n}}}^2(f)\, df \tag{2.6}$$

Also, in noise circuit analysis, $\overline{x_{\mathrm{n}}^2}$ is used in conjunction with the property described by Eq. (2.7), where A is the low frequency gain factor of the circuit. Moreover, A can represent a current, voltage, transconductance or transimpedance amplification factor. While $\overline{x_{\mathrm{n,in}}^2}$ and $\overline{x_{\mathrm{n,out}}^2}$ may represent the respective current or voltage noise quantities at the input and output of the circuit.

$$\overline{x_{\mathrm{n,out}}^2} = A^2 \overline{x_{\mathrm{n,in}}^2} \tag{2.7}$$

It can be observed that the property described by Eq. (2.7) resembles the spectrum-shaping theorem. However, the difference between the property in Eq. (2.7) and the theorem expressed in Eq. (2.3) lays on the fact that the application of the former is limited to moderate frequencies, while the later applies to all frequencies. Additionally, due to the fact that the value of A is commonly calculated from the DC operation conditions of the circuit and extrapolated to higher frequencies, the property expressed in Eq. (2.7) should only be considered as a tool for the noise performance estimation of a circuit. Nevertheless, this property is part of the analog circuit designer tool set [54, 59].

It is also common for the mean square value of the PSD to be provided in terms of its square root value. In this case it will be identified as the root-mean-squared value of the PSD, $X_{\mathrm{n,RMS}}$, also known colloquially as the RMS noise; Eq. (2.8) defines it for the sake of clarity.

$$X_{\mathrm{n,RMS}} = \sqrt{\overline{x_{\mathrm{n}}^2}} = \sqrt{\int_{f_1}^{f_2} S_{\mathrm{n}}(f)\, df} = \sqrt{\int_{f_1}^{f_2} X_{\mathrm{n}}^2(f)\, df} \tag{2.8}$$

The RMS representation of the PSD allows the comparison between the energy carried by the noise signal and the energy dissipated by a resistor excited with a sinusoidal or DC supply source. For this reason it is common that the noise performance of many electrical devices be reported as RMS noise for a defined frequency bandwidth (BW).

For illustrative purposes, a plot of the current PSD ($S_{\mathrm{n}}(f)$) obtained from the simulated operation of a NMOS transistor, belonging to a 22 nm FDSOI technology, is shown in Figure 2.8. In fact, according to the 22 nm FDSOI technology documentation, the MOSFET simulation models from this technology only consider the 1/f and thermal noise phenomena. In practice, the current PSD of a MOS transistor is characterized by means of a calibrated measurement system composed mainly by low noise voltage sources for MOS transistor bias and a Low Noise Amplifier (LNA) for noise amplification, using a configuration similar to the one shown in Figure 2.7 [60].

As can be observed in Figure 2.8, the PSD is composed by two distinctive regions separated by a reference point known as corner frequency f_{c}. In the first region, the current noise energy of the MOS transistor decreases as the frequency increases. Therefore, the PSD of this region is identified as the frequency dependent current PSD, $S_{\mathrm{i}}(\alpha f)$. In contrast, the noise energy in the second region remains constant and independent of frequency. Therefore, the PSD in this region is identified as the frequency independent current PSD, $S_{\mathrm{i}}(0)$. Then, Eq. (2.9) can be inferred.

$$S_{\mathrm{i}}(f) = S_{\mathrm{i}}(\alpha f) + S_{\mathrm{i}}(0) \tag{2.9}$$

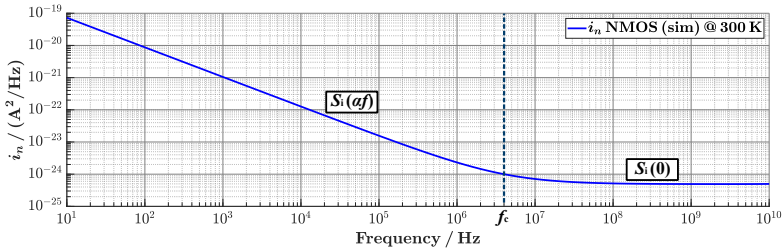


Figure 2.8: Intrinsic current noise of an I/O NMOS transistor. The data is obtained for 300 K via simulation with V_{FG} = 0.45 V, V_{DS} = 0.1 V and V_{BG} = 0 V. The simulation models from the 22 nm FDSOI technology only considers the flicker noise (1/f) and the thermal noise.

It must be mentioned that the location of the f_c and the amount of energy contained in the current PSD of the MOS transistors is dependent on the transistor type (e.g. NMOS or PMOS), construction characteristics (e.g. substrate crystal orientation or manufacturing defects), size, bias and temperature conditions [56, 55, 54]. This hint to the fact that distinct physical phenomena contribute to the current PSD of the MOS transistors. Thus, their energy contributions to the spectrum are commonly referred by a peculiar name. The main noise intrinsic sources contributing to $S_i(\alpha f)$ are the flicker noise (1/f) and the random telegraph noise (RTN). Conversely, the thermal noise and the shot noise are the relevant intrinsic noise sources contributing to $S_i(0)$.

Flicker Noise (1/f)

In 1925, John Erik Bertrand Johnson discovered the presence of flicker noise in vacuum tubes [61]. Later, Walter Hermann Schottky provided an initial mathematical treatment to this phenomenon [62]. Subsequently, the flicker noise was found in a plethora of electrical devices; e. g. carbon microphones and transistors. A peculiar characteristic of the flicker noise is that its spectrum varies in proportion to $1/f^{\gamma}$, with $\gamma = 1$. Therefore, the name $1/f$ noise is commonly used in literature in reference to the flicker noise. An interesting fact about the flicker noise is that it is widely spread in nature; e.g. the human heart beat fluctuations follow an spectrum distribution proportional to $1/f$ [63].

Regarding MOS transistors, two dominant theories exists for the explanation of the physical origin of the flicker noise. The first attributes the flicker noise to the charge carriers random fluctuations in the transistor channel due to charge traps located near the Si-SiO_2 interface. These traps randomly retain and release the carriers, producing surface potential fluctuations and consequently band bending distortions. While the second theory attributes the flicker noise to the mobility fluctuations of the charge carriers due to lattice scattering. As to represent the MOS transistor flicker noise, Ghibaudo et al. proposed the carrier number fluctuations with correlated mobility fluctuations model (CNF/CMF) [64]. This model considers the carrier number fluctuations and the mobility fluctuations as correlated phenomena that occur in the MOS transistor channel, and as such, contributors to the flicker noise.

Eq. (2.10) represents this model, where q is the magnitude of electronic charge, k the Boltzmann constant, T the temperature, N_{BT} is the volumetric gate dielectric trap density per unit energy, g_m is the transconductance, I_D is the drain current, C_{ox} the gate capacitance per unit area, f is the frequency, α is the exponent of the Wentzel-Kramers-Brillouin tunneling probability for rectangular barriers, Ω is a parameter related to the mobility fluctuation, W and L the width and length of the transistor [65].

$$S_{i,CNF/CMF}(f) = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha} \cdot \frac{1}{f} \cdot (1 + \Omega\frac{I_D}{g_m})^2 \cdot {g_m}^2 \tag{2.10}$$

When applied to modern technologies, such as 22 nm FDSOI, the CNF/CMF model represents the current flicker noise in good agreement with the noise measurements done at RT. However, differences between the CNF/CMF model and the measurements are evident for temperatures below 100 K, signaling the fact that a more complex phenomenon governs the MOS transistor flicker noise at CTs [34]. An interesting fact is that in modern technologies, such as 22 nm FDSOI, the magnitude of $S_{i}(f)/{I_{D}}^{2}$ increases with temperature reduction. In their investigation, Bruna Cardozo et al. [34] attributed this increase directly to the improvement of g_{m}/I_{D} that MOS transistors experience at CTs, even though an increase on the calculated oxide trap density (N_{trap}) is also noticed at 4.2 K. Ruben Asanovski et. al. and Takumi Inaba et. al. reached similar conclusions in their respective investigations .

Following the hypothesis that N_{trap} plays a relevant role in the cryogenic flicker noise phenomenon, Hiroshi Oka et al. [66] performed an investigation in which the low frequency current noise spectrum ($S_{i,LF}(f)$) of several MOS transistors, with different N_{trap} and W/L = 100 µm/2 µm, was characterized; different trap densities are induced into the MOS transistors by using Si substrates with different crystal lattice orientations in their fabrication. H. Oka et al. [66] reported that the correlation between $S_{i,LF}(f)/{I_{D}}^{2}$ and $(g_{m}/I_{D})^{2}$ holds at 300 K and 2.5 K for all the tested devices, without importance of the crystal substrate orientation; linking in this way their results to the finding from Bruna Cardozo et al [34]. But more importantly, Hiroshi Oka et al. noticed that at RT the difference in traps densities do not impact the g_{m} normalized low frequency current noise ($S_{i,LF}(f)/{g_{m}}^{2}$, as in Eq. 2.4) of the evaluated devices. However, the noise characterization performed at 2.5 K reveals that the magnitude of $S_{i,LF}(f)/{g_{m}}^{2}$ is strongly dependent of N_{trap} and the DC current flowing through the MOS transistor channel.

In consequence, Hiroshi Oka et al. [66] theorized that a MOS transistor exposed to CTs with $V_{GS} \approx V_{th}$, experiences at its Si-SiO_2 interface an energy difference reduction between the Fermi energy level and the conduction band. Due to this, the Fermi energy level has a stronger interaction with the energy states located near the conduction band edge and that are produced by Si-SiO_2 interface defects, generating in this way higher low frequency current noise at CT than at RT. Similar conclusions were reached by Ruben Asanovski et al. and Takumi Inaba et al. in their respective investigations [65, 67].

Finally, Hiroshi Oka et al. [66] also observed a direct correlation between the N_{trap} of the MOS transistors and the amount of deviation that their subthreshold swing factors (SS), have at CTs. These results strongly supports the hypothesis presented by Arnout Beckers et al. for the explanation of the cryogenic SS deviation, which is suggested to occurs due to the temperature dependent occupation of the interface traps [68]. Although the scientific evidence signals a strong correlation between the cryogenic $S_{i,LF}(f)$ and the cryogenic increase of g_{m}/I_{D}, as well as between the SS deviation and the charge traps

states – Fermi energy interactions, a low frequency cryogenic noise model linking these phenomena has not yet been developed.

Random Telegraph Noise

In MOS transistors, the Random Telegraph Noise (RTN) is an stochastic phenomenon in which the channel carriers are captured and emitted by oxide or border traps of the gate dielectric. In other words, a trap in the SiO_2 or close to the Si-SiO_2 interface, can occasionally capture a charge carrier from the MOS transistor channel. Consequently, the captured carrier can be emitted back to the channel after a period of time. Hence, the capture and emission of charge carriers produce discrete I_D fluctuations. This is illustrated by the RTN signature shown in Figure 2.9, which is obtained from an NMOS transistor through the time domain measurement of its I_D [69].

As shown in Figure 2.9, a two-level RTN signal is defined by three parameters. These are the current amplitude change (ΔI_D), the average times that the signal holds the high state (τ_c), and the low state (τ_e). Thus, τ_c correspond to an empty trap and it indicates the time required by that trap to capture a charge carrier. Similarly, τ_e relates to an occupied trap and it indicates the time needed for the charge carrier emission. Further, the length of the times in which an RTN signal holds the high and low states follows a Poisson probability distribution. Moreover, an interesting fact is that the RTN parameters often show a strong dependence of the MOS transistor operation conditions; e.g. V_{DS}, V_{FGS}, V_{BG} and temperature. Additionally, an RTN signal can be studied in the frequency domain via its Fourier transform of the autocorrelation function. Thus, in the case of a simple two-level RTN signal, its PSD is a Lorentzian type that is characterized by a constant value at low frequencies and a subsequent decay proportional to $1/f^2$, whose corner frequency (f_c) is related to τ_c and τ_e. A mathematical model for the current PSD of a single trap RTN signal is provided by Eqs. (2.11) and (2.12) [69, 70, 71].

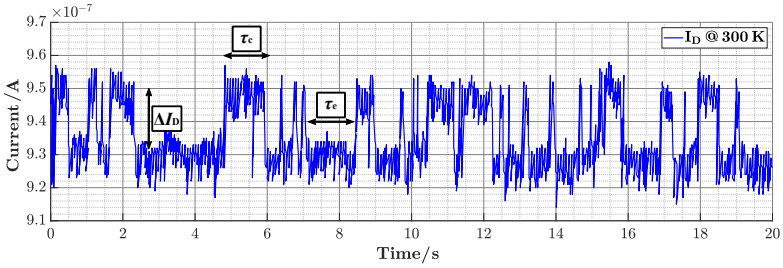


Figure 2.9: RTN signature measured from an NMOS belonging to a 22 nm FDSOI technology; V_{FGS} = 0.5 V and V_{DS} = 0.1 V. The plotted data values are obtained from information depicted in graphical format; the data is only used for illustrative purposes [69].

$$f_c = \frac{\tau_c + \tau_c}{\tau_c \tau_e} \tag{2.11}$$

$$S_{i,RTN}(f) = 4\Delta I_D^2 \cdot \left[\frac{1}{f_c} \left(\frac{1}{\tau_c + \tau_c} \cdot \frac{1}{1 + (2\pi f / f_c)^2} \right) \right] \tag{2.12}$$

Besides, if a MOS transistor has many traps with different time constants, the superposition of their individual RTN signals produces a flicker noise ($1/f$) signature. Then, flicker noise is associated with MOS transistor manufacturing imperfections and material defects, as they work as charge carrier traps. Also, as the MOS transistor scaling progresses towards smaller device areas, the gate oxide composition becomes more complex due to the usage of high-k materials, and the current signals amplitude reduces. Thus, as the quality of oxide interface is degraded and the current signals get smaller, the RTN rises as a relevant reliability issue in modern CMOS IC fabrication technologies. Hence, the RTN characterization is usually employed as a tool for the quality evaluation of MOS fabrication processes. For example, Marquez et al. reported in their experimental study that only 1/3 of the 336 evaluated MOS transistors, manufactured with a 22 nm FDSOI technology and evenly distributed across the testing Si wafer, are trap free [69].

In recent years, the study of the RTN in MOS devices operating at CTs has attracted significant attention. This is not only due to its potential impact over the performance of cryogenic CMOS ICs, but also RTN may pose a challenge for the implementation of QC systems that rely on qubit devices using semiconductor quantum dots manufactured with standard CMOS IC processes. As experimental data indicate that an electron spin confined in a Si/SiGe quantum dot device, experiences a loss of phase coherence caused by $1/f$ charge noise [72]. Therefore, different studies have characterized and analyzed the RTN of MOS transistors belonging to 180 nm, 90 nm and 28 nm planar-bulk technologies [67, 73, 74]. Because, by identifying the intrinsic noise sources of cryogenic MOS devices, the knowledge required for the development of quantum dot devices with improved coherence times can be obtained. So far the experimental evidence indicates that with temperature reduction the LF noise sources transition from inner-oxide traps to interface traps, and below 50 K, to band-edge localized states close to the conduction band-edge [67].

Thermal Noise

Thermal noise is an electrical noise signal generated by the random thermal motion of the charge carriers inside an electrical conductor, and it occurs regardless of the voltage applied to the conductor. Thus, for an ideal resistor (R), its thermal noise is represented as a current source in parallel to it. And, for such a source, its PSD is as in Eq. (2.13), where k is the Boltzmann constant and T the absolute temperature of the conductor [55]. Suffices to mention that in 1928, John Erik Bertrand Johnson reported the discovery and

measurement of the thermal noise in a conductor [75], while Harry Nyquist provided a formal treatment to this phenomenon based on thermo dynamics and statistical mechanics [76]. Thus, it is for these reasons that the thermal noise is also known as the Johnson-Nyquist noise.

$$S_{\mathrm{i,t}} = 4kT \cdot \frac{1}{R} \tag{2.13}$$

In the case of a MOS transistor, its current PSD is defined by Eq. (2.14), for $R_{\mathrm{dif}} = \partial V_{\mathrm{D}} / \partial I_{\mathrm{D}}$ and $V_{\mathrm{D}} = 0\,\mathrm{V}$. However, if $V_{\mathrm{D}} \neq 0\,\mathrm{V}$, Eq. (2.14) must be modified as in Eq. (2.15); $R_{\mathrm{ch}} = V_{\mathrm{D}} / I_{\mathrm{D}}$, is the chord resistance, and $R_{\mathrm{ch}} \neq R_{\mathrm{dif}}$ [56, 77]. Interestingly, it has been reported that the relationship between the thermal noise and the MOS transistor temperature hold from 300 K down to 3 K. But, as the temperature and thermal noise of a MOS transistor reduce, the effect of its intrinsic shot noise becomes relevant[78, 79].

$$S_{\mathrm{i,t\,MOS}\,@\,V_{\mathrm{D}}=0\,\mathrm{V}} = 4kT \cdot \frac{1}{R_{\mathrm{dif}}} \tag{2.14}$$

$$S_{\mathrm{i,t\,MOS}} = 4kT \cdot \frac{R_{\mathrm{ch}}}{R_{\mathrm{dif}}^2} \tag{2.15}$$

Shot Noise
In MOS transistors, shot noise is associated with the DC current flow produced by the diffusion of charge carriers crossing a potential barrier, such as the one between source and the device channel [55, 80]. Then, the shot noise current PSD of a MOS transistor is given by Eq. (2.16), where q is the fundamental charge of the electron and I_{D} is the DC drain current of the transistor.

$$S_{\mathrm{i,s\,MOS}} = 2qI_{\mathrm{D}} \tag{2.16}$$

2.3.1.2 Extrinsic Noise Sources

As previously mentioned, any electrical circuit can experience the interference generated by extrinsic noise sources. Moreover, according to the circuit characteristics and application requirements, the extrinsic noise interference can or cannot be tolerated. Even so, a positive aspect of the extrinsic noise signals is that its interference can be suppressed through the use of EMC techniques during the system integration phase.

However, in order to enhance the efficiency of the EMC techniques, it is necessary to identify the physical mechanisms that produce the extrinsic noise signals. In the case

of cryogenic electronics, the most common extrinsic noise sources are the vibration induced noise and the ground loop noise. Besides, these noise sources are related to the cryocooling system operation and physical characteristics. Therefore, they are described in the following.

Vibration Induced Noise

As described in section 2.1, dry cryocooling systems such as the pulse tube and GM cryocooler operate with a cooling cycle in which He gas is constantly compressed and expanded inside the cryocooler structure. Hence, mechanical vibrations and audible noise are produced during the cryocooler operation. This intrinsic phenomenon is well documented by the cryocoolers manufacturers and systems integrators.

In particular, it is known that pulse tube systems generate less vibrations than GM cryocoolers. Mainly due to the fact that the rotary valve-motor can be detached from the pulse tube main structure, which is a feat not possible in GM cryocoolers. Furthermore, the cold head of a pulse tube does not have internal moving parts that can produce vibrations, in contrast to the GM cryocooler which employs regenerator-displacer parts [81]. Consequently, the pulse tube cryocooler has been the preferred choice for the development of dry dilution refrigerators. Although, dilution refrigerators still experience the mechanical vibrations produced by their pulse tube cryocoolers.

Nevertheless, GM cryocoolers offer the advantage of being less expensive and can be oriented at any direction; these are relevant qualities for the development of scientific equipment with particular requirements. Moreover, according to the system integrator design choices, the mechanical vibrations produced by the GM cryocooler can be attenuated through the coupling of pneumatic dampers or lead weights [50].

Regarding the mechanical vibrations inside dilution refrigerators, it has been demonstrated by Kalra et al. in [82] that they induce electrical noise signals on the control lines that are used to interface the RT electronics with single electron transistors (SETs); a semiconductor device commonly used in QC experiments. But most importantly, Kalra et al. also demonstrated that the vibration induced electrical noise can contribute to the spin decoherence of the electron held by the SET, if not suppressed [82].

The mechanism by which the mechanical vibrations induce electrical noise signals is the triboelectric effect. According to Kalra et al., if the dielectric material of a coaxial cable is rubbed against the inner or the outer conductor by mechanical vibrations, the friction will ease a charge transfer that can manifest as a current or voltage signal. Moreover, as the dielectric material shrinks with temperature reduction, the friction between the dielectric and the conductors becomes easier. Then, higher amount of mechanical induced noise is produced at CTs [82].

In order to reduce the induction of vibration noise signals, Kalra et al. recommend the flattening of semi-rigid cables or the jacketing of flexible cables, as to restrict the movement within the cables [82]. Other approaches include the use of active mechanical dampers as a subsystem of the dilution refrigerator. As well as the use of two pulse tube cryocoolers with offset He gas compression-expansion cycles, in order to cancel their mechanical vibrations [48].

Ground Loop Noise

In an electrical system a ground loop occurs when two points in the system, which ideally should have the same reference potential, have different reference potentials. Thus, a ground loop can become a source of noise and produce interference. Specially when multiple reference ground points are separated by a large distance and are connected to the AC power ground, or when low-level analog circuits are used [53].

This situation is displayed in Figure 2.10, where the system circuits are grounded at two different reference points; indeed, two different ground symbols are used to emphasize the fact that the ground points are physically separated and have different potentials. Furthermore, as shown in Figure 2.5, the cryocooling system used in this work may be prone to ground loop noise due to its physical characteristics. Hence, a system similar to the one in Figure 2.10 may face the following:

- The ground potential (V_{Ground}) between the ground points, resulting from different currents flowing through the ground impedance, may couple a noise voltage signal (V_{Noise}) into the system.
- A strong magnetic field can induce a voltage noise signal into the loop formed by the signal conductors and the system ground (ground loop in Figure 2.10).
- Multiple returns paths exist for the signal current, and at low frequencies, the signal current may return through the system ground and not through the return conductor.

Most of the ground loop noise impact occurs at frequencies lower than 100 kHz, affecting sensitive analog and instrumentation systems. In contrast, ground loops are seldom a

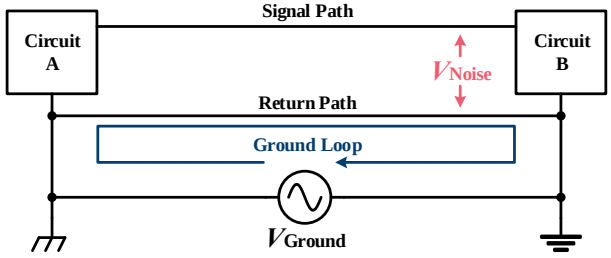


Figure 2.10: Ground loop between two circuits.

problem for digital and high frequency systems [53]. As to deal with ground loops, one of the following EMC approaches can be undertaken:

- Use of single-point or hybrid ground.
- Increment of the system tolerance to ground loop noise, by minimizing the ground impedance or by boosting the SNR through the use of higher amplitude signals.
- Breaking of the ground loop through the use of transformers, common-mode chokes or optical couplers.

Beyond common electrical systems, ground loop noise may be an issue in QC systems such as quantum dots. This is because semiconductor based quantum dot devices are usually biased with DC voltages as to form gate-defined quantum dots, which store the quantum information used in QC calculations via the spin of an electron. However, low frequency noise in these DC potentials may unintentionally distort the quantum information. Since dilution refrigeration systems are complex machines composed by several electro-mechanical sub-systems, care must be placed on the detection and suppression of ground loops during the QC system physical integration phase in order to prevent the quantum information distortion.

2.3.2 Limited Connections in Cryocooling Systems

The main requirements that a dilution refrigerator must satisfy in QC applications are low base temperatures and high cooling powers, because quantum physics phenomena can only be exploited by the qubit devices at extremely low temperatures. And, in order to scale up the QC systems, high cooling power is needed to dissipate the thermal load associated to the qubit devices, support cryogenic electronics and electrical connections, whilst maintaining the fridge base temperatures. For example, a commercial dilution refrigerator can hold a base temperature of 100 mK with 1.5 mW of cooling power [48].

However, dilution refrigerators are not only limited by their temperature and cooling power characteristics. These cooling systems are also constrained by the number of electrical connections and space available for the development of experiments. This is because the twisted-pair and coaxial cables, which are commonly used in QC systems, must be thermalized and passively filtered as to prevent the injection of noise signals generated at RT and the over heating of the fridge stages. Thus, as the thermalization and filtering of the cables require the use of fridge space and cooling power, the amount of connections going in and out of the dilution refrigerators is limited.

For instance, the cabling approach employed in contemporary QC systems is illustrated in Figure 1.2 [21]; the control electronics is placed at RT and only the support electronics (e.g. attenuators, amplifiers and passive filters) is placed inside the dilution refrigerator as indicated by the schematic representation in Figure 2.11. Such an approach is

expected to be adequate for the development of QC system having up to 1000 qubit devices. However, it will not accommodate the connections needed for system consisting of thousand or millions of qubits, representing a bottleneck that will hinder the scalability of QC systems in the future.

One solution to this situation is the development of dilution refrigerators with bigger experimental space and higher cooling power. For example, IBM has developed a dilution refrigerator with 1.7 m^3 available for experiments placement and 10 mW of cooling power at 100 mK base temperature [83]. Considering its cost, this is not an approach that could be followed by most of the QC research groups.

Alternatively, the use of cryogenic CMOS ICs is expected to decrease the amount of connections between the RT systems and the qubit devices, enabling the reduction of

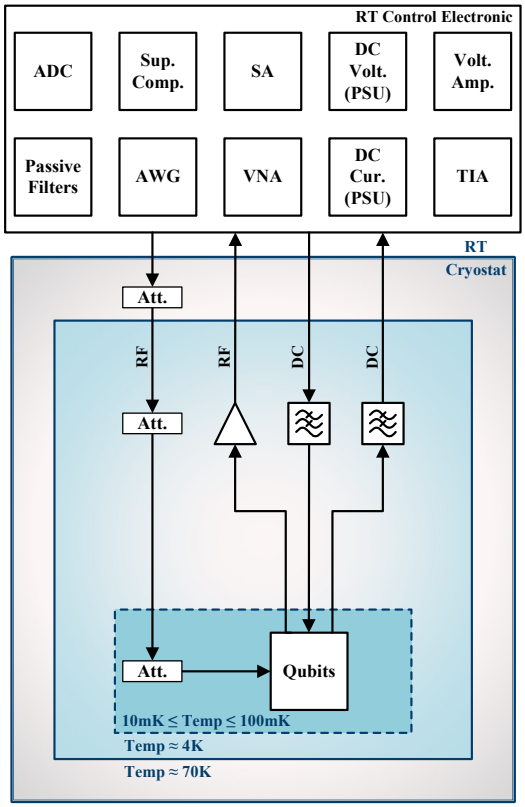


Figure 2.11: Components distribution in contemporary QC systems.

the space required for QC experiments or an increase in the number of qubits available in future QC systems [22].

Regarding power distribution for cryogenic CMOS ICs, instead of dedicating individual connections for each power domain, a cryogenic PMU could locally provide different regulated voltages for each power domain. Reducing in this way the amount of connections between the RT systems and the electronics inside the fridge.

2.3.3 Lack of Commercial Cryogenic DC-DC Converters

Beyond QC, other systems that may benefit from the development of CMOS ICs that are able to operate at temperatures lower than 10 K, are the astronomical detectors, high performance computing and space exploration systems [31, 30, 29]. Due to the aerospace sector commercial relevance, this sector has the most developed cryogenic electronics ecosystem. However, in most of the aerospace systems the lowest operation temperature is around 77 K.

Although commercial cryogenic DC-DC converters are offered in the market, they are not rated for operation at temperatures lower than 77 K; e.g. Modular Devices, Inc. offers a family of radiation hardened DC-DC converters rated for 77 K [84]. Even if they are not currently demanded, it is expected that cryogenic DC-DC converters will be needed for power distribution in scalable QC systems.

2.3.4 Lack of Cryogenic MOSFET Simulation Models Supported by Commercial ICs Manufacturers

The development of modern CMOS ICs relies on the availability of MOSFET simulation models that accurately represent the electrical behavior of the devices over a plethora of operation conditions. Simulation models are an essential part of the MOS circuits design and verification process. Without them, it is not possible to accurately evaluate the performance and reliability of a circuit prior to its prototyping or production (pre-silicon verification).

Therefore, it is a common practice from the commercial CMOS ICs manufacturers to develop simulation models that represent the characteristics of their fabrication processes; which are also known as technologies. In this way, the DC, AC, RF and process variation characteristics of the MOS devices can be considered during the ICs design procedure.

But most importantly, the commercial MOSFET simulation models are commonly rated for operation at temperatures between 233.15 K to 393.15 K (−40 °C to 120 °C). Hence,

the simulation of the MOS transistor electrical characteristics at CTs is not supported by commercial ICs manufacturers. Mainly due to the costs associated to the development of cryogenic simulation models and its low demand in the market.

Beyond the commercial interests, not all the CMOS IC technologies can be adopted for cryogenic applications. For example, it has been documented that the electrical performance of old technologies gets degraded at CTs [85, 86]. Moreover, the equations set used by most of the commercial MOSFET simulation models cannot represent the cryogenic electrical behavior of the devices, as their equations do not converge at CTs.

Fortunately the devices belonging to modern commercial technologies, such as planar-bulk CMOS [68, 87], FDSOI-CMOS [88, 34], Fin FET [89, 90] and Gate-All-Around [91, 92], can operate at temperatures lower than 10 K without a severe performance degradation.

Moreover, some research groups have achieved the development of in-house cryogenic MOS simulation models [93]. In addition, some commercial ICs manufacturers had announced their plans for the development of cryogenic simulation models together with academic and research institutions [94, 95]. Nevertheless, many design teams are still constrained to developing ICs without a reliable cryogenic pre-silicon verification due to the restrictive access to cryogenic simulation models.

2.4 Proposal: Cryogenic Power Management Unit

A current technology trend is the development of cryogenic CMOS ICs for the control of qubits, as ICs are expected to allow the development of scalable QC systems consisting of thousands of physical qubits. This implies that the control ICs must be placed as close as possible to the qubits operated at CTs [24, 96].

Nevertheless, in order to maintain a proper thermal management and avoid a distortion of the qubit states, a distributed approach of the cryogenic control electronics inside the fridge may be adopted as depicted in Figure 2.12. In such an approach, the die containing the qubits devices is placed in the sub-Kelvin stage (100 mK-10 mK) of the dilution refrigerator together with low power control electronics (QCON Sub-K); e.g. reading resonators, switching matrices, and DC bias voltage generators [97, 27, 98, 99].

Higher temperature stages must accommodate high performance cryogenic electronics (QCON 4K), since the cooling power demanded by these systems cannot be supplied by the sub-Kelvin stage. Besides, it has been demonstrated that high performance cryogenic ICs can enable the control and read out of the qubit states [100, 28].

Furthermore, these cryogenic ICs (QCON 4K and QCON Sub-K) are composed of analog, digital and mixed-signal circuits that require undistorted electrical power supply feeds

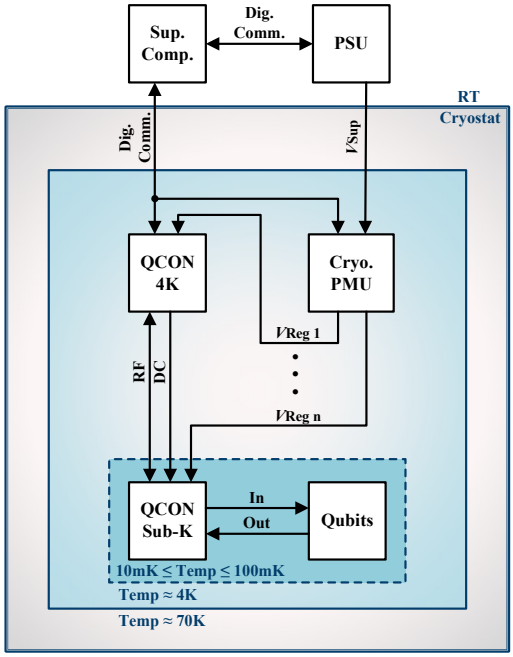


Figure 2.12: Cryogenic electronics distribution for the scalability of QC systems.

for optimal performance. However, since the power supply feeds required by the cryogenic electronics are typically provided by Power Supply Units (PSUs) located at RT, several lines of the dilution refrigerator setup are solely dedicated for power delivery. Consequently, this approach reduces the amount of connections and space available in the setup, inhibiting the QC system scalability.

Furthermore, since the physical distance between the PSUs and the control cryogenic electronics can be in the order of meters, and the delivered power in the order of mW, the power supply lines can be considered as transmission lines prone to distortions and losses [101]. Equally important is the fact that commercial DC-DC converters are not able to operate at temperatures as low as 4 K, stressing the need for cryogenic PMUs [32, 102]. All of these indicate that PMUs, with elements (e.g. current reference, passive components, voltage reference and voltage regulator) capable of cryogenic operation, are needed for the assembly of scalable QC systems.

Hence, in this work the development of a cryogenic PMU composed by a CMOS IC and some passive components, is proposed. Moreover, as to prevent the production of interference by the different noise sources, the application of EMC techniques is also

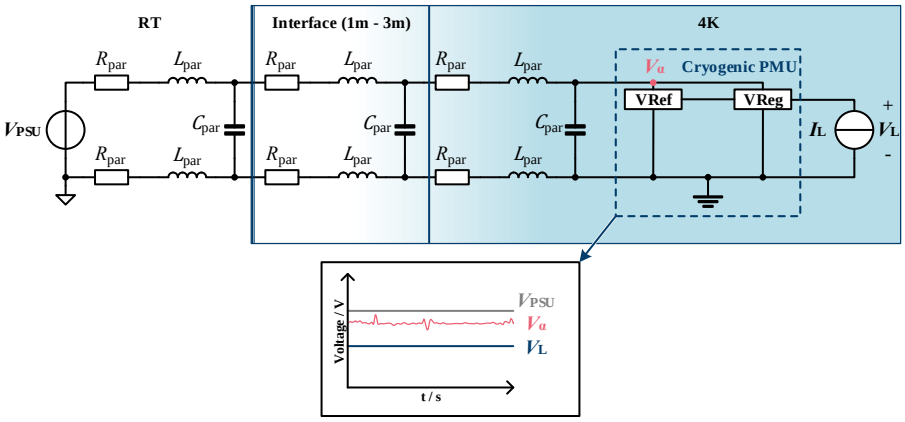


Figure 2.13: Cryogenic Power Management Unit (PMU) concept.

Table 2.1: Required nominal electrical specifications of the proposed cryogenic PMU.

Parameter	**Magnitude**
Supply voltage (V_{Sup})	2 V
Regulated output voltage (V_{Reg}) range	0.7 V-1 V
Load current (I_{Load}) range	1 µA-10 mA
Load regulation (LR) @ ΔA = 10 mA	50 mV/A
Power supply rejection ratio (PSRR)	−50 dB
Integrated output noise @ BW= 10 Hz-10 kHz	200 μV_{rms}

considered. Such a PMU must be able to provide a defined, clean and regulated voltage to the cryogenic control electronics, as indicated by the conceptual schematic shown in Figure 2.13. As to achieve that goal, the cryogenic PMU must satisfy the electrical specifications indicated in Table 2.1.

Chapter 3

Cryogenic DC Characterization of 22 nm FDSOI Technology

In order to develop a cryogenic PMU, it is necessary to know the characteristics and the electrical behavior of its components at CTs. Since in this work the IC technology of choice is 22 nm FDSOI, the first section of this chapter presents a brief description of the MOSFETs belonging to such a technology. This is done with the intention to provide a technical frame of reference to this work.

The second section of this chapter presents a DC characterization of some of the components belonging to the 22 nm FDSOI technology. Specifically, the DC characteristics of poly-Si resistor, NPN-Si BJT in diode configuration, dynamic V_{th} MOS P-type (DTMOSP) as diode and I/O super low V_{th} (IOSLV) NMOS, are provided for temperatures between 7 K and RT. Besides, the outcomes of this characterization are employed as reference for the design of the cryogenic PMU presented in Chapter 4.

In the final section of this chapter, the endeavours focused on developing cryogenic simulation models for the 22 nm FDSOI technology are addressed.

3.1 22 nm FDSOI Technology

As depicted in Figure 3.1, 22 nm Fully Depleted Silicon On Insulator (FDSOI) MOSFETs are built over an insulating layer known as Buried Oxide Insulator (BOX); usually SiO_2. Hence, the channel body and the drain/source regions of those transistors are separated from the die substrate by the BOX layer, the thickness of which is close to 20 nm. Also, in FDSOI MOSFETs the channel body thickness is very thin and it is commonly defined as the Ultra-Thin Body (UTB). Since the UTB has an average thickness of 6 nm, the depletion region covers the whole of the UTB. Therefore, it does not need an additional electrical connection and can be left floating. Besides, for the sake of clarity, the UTB is the Silicon On Insulator (SOI). Due to these physical properties, the FDSOI MOSFETs provide several performance improvements over bulk-CMOS transistors [36].

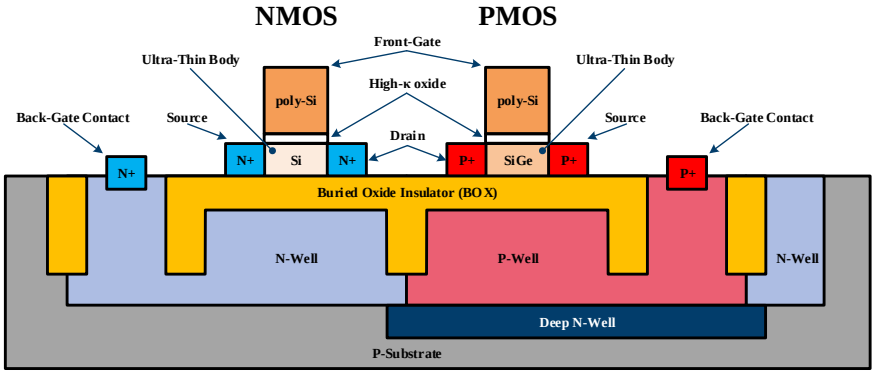


Figure 3.1: Cross-section view sketch of the NMOS and PMOS transistors in the 22 nm FDSOI technology. The devices use the flip well configuration as in [36].

In fact, as FDSOI technology uses undoped channel bodies, its MOSFETs have superior immunity to the V_{th} variation; i.e. the random dopant fluctuation is reduced. This is in contrast to the bulk-CMOS transistors which require channel doping via ion implantation [103]. Moreover, during the FDSOI MOSFETs fabrication the undoped UTBs are formed with an integration scheme known as shallow trench isolation after SiGe epitaxial growth (STI - last) [104].

Additionally, by having undoped UTBs with reduced thickness, the FDSOI MOSFETs provide an improved control over the channel electrostatics. Therefore, the impact of short channel effects like the drain induced barrier lowering (DIBL), is reduced [105]. Also, the transistors g_{ds} and g_m, are reduced and increased respectively [36]. Moreover, since the drain/source regions are isolated from the well, the impact of some of the transistor parasitic elements is greatly reduced, as there is no drain/source - well junction. Accordingly, in FDSOI MOSFETs the forward biasing range is not limited by the junctions latch-up, as with bulk-CMOS transistors. Besides, the drain/source - well capacitor is bias independent, contrary to the case of bulk-CMOS transistors [36].

Regarding the technology capability for RF applications, the transition frequency (f_T) of its core NMOS and PMOS transistors can achieve a value as high as 375 GHz and 260 GHz, respectively. While the maximum oscillation frequency (f_{MAX}) of such transistors, is around 290 GHz and 250 GHz [36]. It is important to mentioned that the UTB of the FDSOI PMOS transistors is made of a SiGe alloy, as PMOS transistors with SiGe UTB posses an improved drive current than PMOS transistors with Si UTB [104].

But perhaps more interesting is the fact that the FDSOI MOSFETs posses two terminals for the control of the current flowing between the drain and source regions [106]; such devices are also known as planar double-gate MOSFETs [107]. The main control terminal

is the front gate, which is set up as an stack made of the high-κ oxide and poly-Si slabs placed on top of the UTB, as shown in Figure 3.1. In the case of the core transistors, which are intensively used in digital and RF applications, the high-κ oxide slab has an average thickness of 1.35 nm. On the other hand, the average thickness of the input-output (I/O) transistors high-κ oxide is 3.53 nm. Due to its thicker front gate oxide, I/O transistors can handle up to 2 V on their front gates before their oxides fracture, while the core transistors can only support up to 0.9 V before an oxide fracture occurs.

The second control terminal is the back gate, which is composed by the BOX and N/P well layers placed below the UTB. Furthermore, the back gate can also control the flow of current in a FDSOI transistor. However, due to the 20 nm thickness of the BOX layer, its electrostatic strength is lower than the one of the front gate. Besides, the material used in the construction of the front oxide and BOX layers is not the same, and neither are their dielectric constants. Thus, if the I_{DS} is intended to be controlled with only one gate, the back gate will not be as effective as the front gate; i.e. the g_m of the back gate is lower than the one of the front gate. Conversely, the BOX thickness allows that the back gates of the FDSOI MOSFETs can handle up to +/- 3.98 V before an oxide fracture.

It is relevant to mention that the back gate voltage polarity goes according to the transistor well type, as to prevent the activation of parasitic P-N junctions. In the case of the well configuration shown in Figure 3.1, the back gate voltage of the NMOS can be set between 0 V and + 3.98 V. While the PMOS back gate voltage can be set between - 3.98 V and 0 V. For both cases, it is assumed that the die P-Substrate is tied to 0 V and the Deep N-Well around the PMOS P-Well is tied to a positive potential.

The main utility of the back gate is its capability to modify the V_{th} of a FDSOI MOSFET, when it is used together with the front gate. This is because the UTB thickness allows that the front and back gates be electrostatically coupled; i.e. the depletion regions of both gates merge inside the UTB, producing in this way a FDSOI film. Then, due to the charge coupling of both gates, the distribution of the energy bands in a FDSOI MOSFET is determined by the voltages placed at the front and back gates. As a consequence, the front gate V_{th} depends on the bias voltage set at the back gate [108, 109].

The V_{th} functionality offered by the 22 nm FDSOI technology is showcased by the simulation results displayed in Figure 3.2, which correspond to the I_{DS} curves of an I/O NMOS transistor operated at two back gate voltage (V_{BG}) conditions, 0 V and 1 V. Here, the transistor V_{th} reduces from 370 mV to 190 mV, when the V_{BG} changes from 0 V to 1 V. In general, the V_{th} tuning capability of FDSOI MOSFETs is used to manage the power consumption of different systems inside an IC.

Another feature of the 22 nm FDSOI technology is that its MOS transistors can operate at CTs without substantial performance loss [34, 35]. This is in contrast to the cryogenic electrical behavior of higher dimension planar-bulk MOS technologies; e.g. the presence

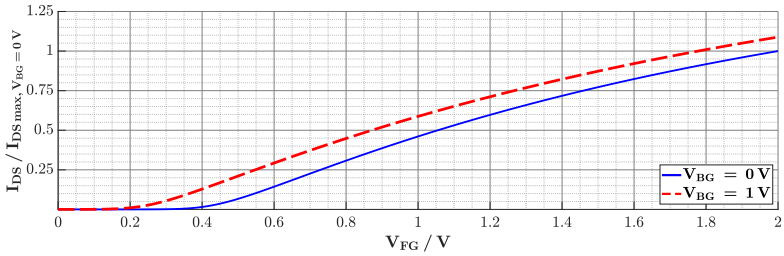


Figure 3.2: Normalized I_{DS} of an I/O FDSOI NMOS transistor obtained via simulation. The data correspond to 300 K, V_{DS} = 0.1 V, and V_{BG} set to 0 V and 1 V.

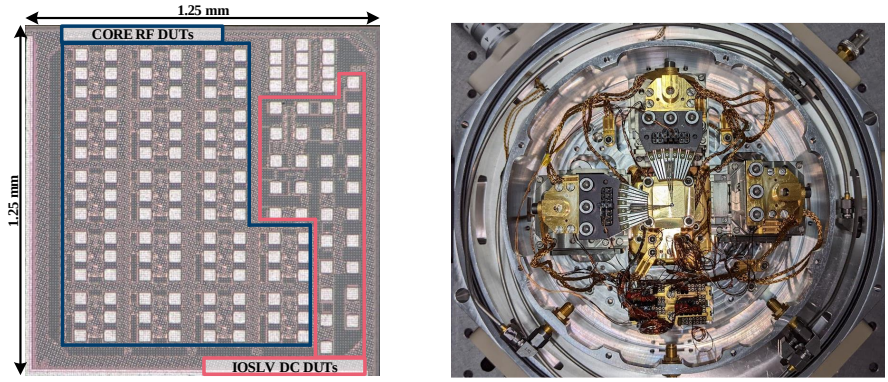
of drain current kink, overshoot and hysteresis effects had been reported for a 0.7 µm CMOS technology at 4.2 K [86].

And, even though the V_{th} of FDSOI MOSFETs increases at CTs just as in other MOS technologies, its V_{th} tuning capability can be used to compensate for such increase. It is for this reason that the 22 nm FDSOI technology has become an attractive option for the development of cryogenic ICs. Nevertheless, the development costs and heat management at the UTB due to the BOX thermal resistance, must be considered.

3.2 Cryogenic DC Characterization

In order to develop a cryogenic PMU, it is necessary to verify that the components that could be part of it have adequate electrical characteristics at CTs; e.g. V_{th}, g_m and temperature coefficient [110]. Thus, the experimental measurements reported in this section focus on the DC electrical characteristics of some of the components included in a 22 nm FDSOI technology, at temperatures ranging from RT down to 7 K. Specifically, the characteristics of poly-Si resistor, NPN-Si BJT in diode configuration, dynamic V_{th} MOS P-type (DTMOSP) as diode and I/O super low V_{th} (IOSLV) NMOS, are provided.

With the goal of performing the cryogenic electrical characterization of the passive and active components, a die containing RF and DC devices has been designed and fabricated; Figure 3.3 (a) shows a micrograph of the prototype die. It must be mentioned that the cryogenic electrical characteristics of the RF devices are reported in [44]. The dimensions of the components studied in this work are indicated in Table 3.1. In order to perform the DC electrical characterization of the DUTs, a semiconductor device analyzer (SDA) B1500A from Keysight is used [111]. To control the environmental temperature and perform the needle probing of the die containing the DUTs, the attoDRY800 station described in section 2.2 is used; Figure 3.3 (b) shows a photography of the cryogenic probing station.



(a) (b)

Figure 3.3: (a) Prototype die containing the components of the 22 nm FDSOI technology evaluated in this work. (b) Cryogenic cooling station used for needle probing of the DUTs; attoDRY800 cryocooling system.

Table 3.1: I/O super low V_{th} (IOSLV) DC DUTs.

DUT	Width	Length	Multiplicity
High res., w/o silicide, N+ poly-Si resistor	1 µm	40 µm	1
NPN-Si BJT	3.2 µm	3.2 µm	1
DTMOSP-1 (IOSLV)	1 µm	1 µm	4
DTMOSP-2 (IOSLV)	1 µm	1 µm	32
NMOS (IOSLV)	1 µm	0.32 µm	1

The results obtained from the experimental measurements performed over the DUTs, from RT down to 7 K, are presented in the following sections.

3.2.1 Poly-Si Resistor

The measured electrical resistance obtained from the N+ poly-Si resistor at different environmental temperatures, with a testing current sweep going from 1 µA up to 70 µA, is shown in Figure 3.4. As can be observed, under low testing currents, the resistor exhibits a nonlinear electrical resistance at all temperatures; the resistance has an approximate change of 1 %. Such a phenomenon is associated to the silicide-Si interface

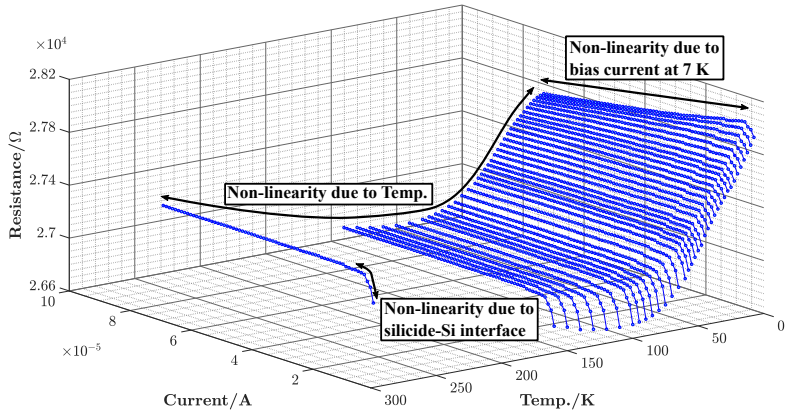


Figure 3.4: Electrical resistance measured from N+ poly-Si resistor at different bias current and temperature conditions. The resistor is evaluated from 7 K to 295 K, with bias currents going from 1 µA to 70 µA.

used to contact the poly-Si resistor slab [112].

Additionally, at moderate and high testing currents the electrical resistance of the N+ poly-Si resistor shows a nonlinear behavior with respect to temperature, with percentage changes between 1.13 % and 1.75 % along the 7 K to 295 K range. This is a phenomenon related to the doping concentration levels applied to the poly-Si resistor [113] [114]; i.e. the amount of impurity atoms (dopants) introduced into the poly-Si material per unit volume in order to alter its electrical conductivity.

Another aspect to consider from the results shown in Figure 3.4, is that at temperatures close to 7 K the N+ poly-Si resistor has a nonlinear resistance that strongly depends on the testing current magnitude. For example, at 7 K the resistor resistance has a maximum change of 1 %, when biased between 4 µA and 70 µA. This behavior may be related to a self-heating effect in doped poly-Si resistors that is exacerbated at CTs; this phenomenon requires further investigation in order to be understood.

3.2.2 NPN-Si BJT

Figure 3.5 shows the measured drop voltage of the NPN-Si BJT when configured as a diode, at different temperatures and current testing conditions. As can be seen, this component exhibits a linear complementary to absolute temperature (CTAT) behavior in the temperature range going from 70 K down to 295 K. However, along this temperature range, the linearity of the drop voltage varies with the testing current magnitude.

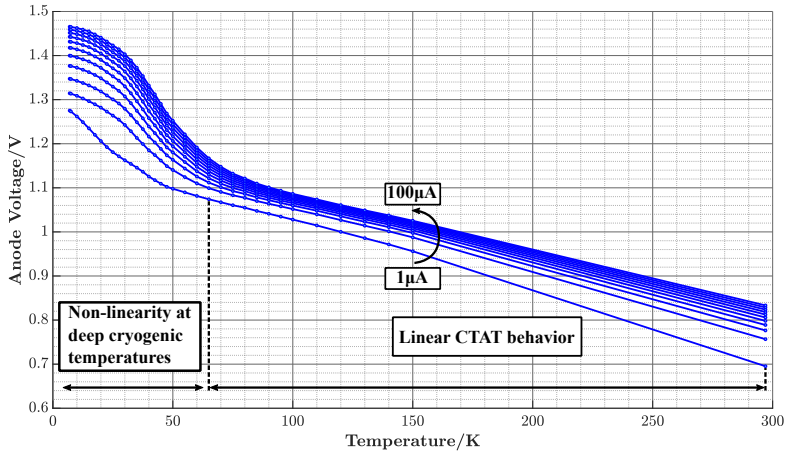


Figure 3.5: Drop voltage of NPN-Si BJT in diode configuration, at different bias current and temperature conditions. The component is evaluated from 7 K to 295 K, at bias currents of 1 µA and from 10 µA to 100 µA with steps of 10 µA.

In addition, at temperatures below 70 K, the drop voltage possesses a strong nonlinear behavior. Therefore, the NPN-Si BJT in diode configuration is an unreliable device for deep cryogenic temperatures. Consequently, its use in the development of cryogenic voltage reference circuits is not recommended. Moreover, these results are in agreement with findings previously reported for integrated PNP-Si BJTs [32].

3.2.3 DTMOSP (IOSLV)

In the dynamic threshold MOS (DTMOS) configuration a planar-bulk MOSFET has its gate and body terminals short-circuited. Consequently, such a transistor experience a V_{th} modification with every change in its V_{SG} [115]. Additionally, a DTMOS transistor can operate as an active device similar to a diode by having its gate, body and drain terminals tied together. In such a case, when the DTMOS transistor is biased with a constant current its V_{SG} exhibits a CTAT behavior. Due to its electrical characteristics, MOSFETs in DTMOS configuration have been used in the production of low power voltage references and temperature sensors [115, 116].

Also, it has been reported that a DTMOSP transistor manufactured in standard 0.16 µm CMOS technology maintains its CTAT behavior when it is operated as a diode between 4 K and 300 K [117]. Besides, the development of cryogenic voltage references with DTMOSP transistors from a 40 nm CMOS technology has been proposed [118, 119].

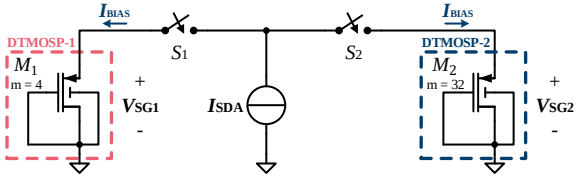


Figure 3.6: Simplified schematic representation of the setup used in this work for the evaluation of the DTMOSP (IOSLV) devices.

This work evaluates the electrical behavior of DTMOSP (IOSLV) transistors fabricated in 22 nm FDSOI technology, when operated as diodes between 7 K and 295 K. For that purpose two DTMOSP transistors configured as diodes, DTMOSP-1 and DTMOSP-2, are included in a prototype die and electrically evaluated as in Figure 3.3. A simplified schematic circuit representation of the evaluation setup is provided in Figure 3.6. Here, the front gate, back gate and drain terminals are tied together to the circuit ground. Also, each DTMOS device is individually biased and measured by a source-measurement unit of the SDA (I_{SDA}). And for each temperature point, the DTMOSP-1 is evaluated at first with a bias current of 1 µA, and later with 10 µA to 100 µA at steps of 10 µA. Subsequently, the DTMOSP-2 device is evaluated in the same way.

Figure 3.7 shows the measurement data obtained from the evaluation of the DTMOSP-1 (IOSLV) transistor. Specifically, its source to gate voltage (V_{SG1}) when used as a diode. These measurement results indicate that the DTMOSP-1 can generate CTAT or proportional to absolute temperature (PTAT) voltages, according to its current bias conditions. Thus, when the DTMOSP-1 is biased with 1 µA, its V_{SG1} exhibits a highly linear CTAT behavior between 7 K to 295 K. This is a relevant characteristic that could be exploited in the design and development of wide range temperature sensors with low power consumption in 22 nm FDSOI technology. However, further characterization regarding the current bias conditions and process variations, is required to validate this device as a reliable alternative to the temperature sensing Si diode.

When the DTMOSP-1 bias current is increased, the behavior of its V_{SG1} shifts from CTAT to PTAT, in the range between 50 K and 295 K. Also, it is pertinent to point out that for bias currents between 20 µA and 30 µA, V_{SG1} fluctuates around 1 mV in the range between 7 K to 50 K. This is also an important characteristic, as it could be used for the generation of voltage references intended to operate in this cryogenic temperature range.

Furthermore, Figure 3.8 shows the difference between the V_{SG} of the DTMOSP-1 and DTMOSP-2, with respect to temperature and when both devices are biased with the same current magnitude; i.e. $\Delta V_{SG} = V_{SG1} - V_{SG2}$. As can be seen, ΔV_{SG} exhibits a PTAT behavior whose linearity depends on the bias current conditions of both DTMOSP devices. However, the PTAT voltages are not completely linear with respect to temperature

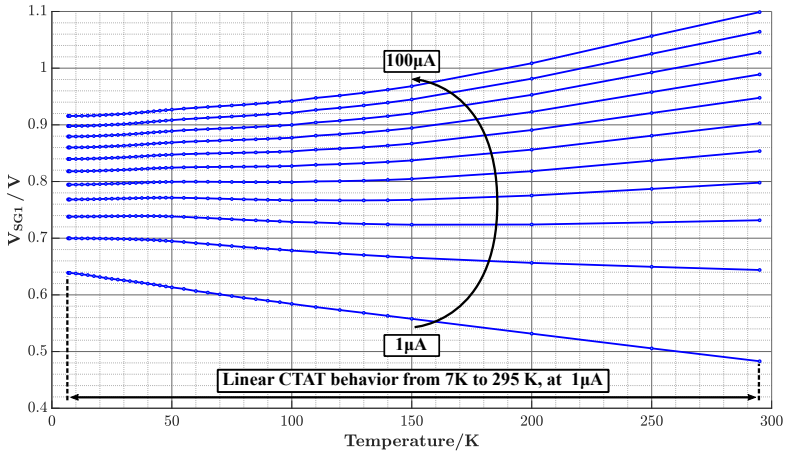


Figure 3.7: Source to gate voltage (V_{SG1}) of DTMOSP-1 (IOSLV) transistor when used as diode. The component is evaluated from 7 K to 295 K, at bias currents of 1 µA and from 10 µA to 100 µA with steps of 10 µA.

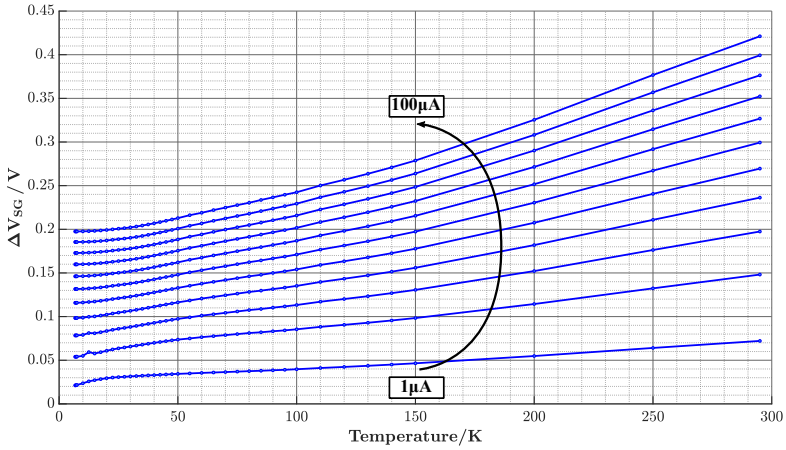


Figure 3.8: Source to gate voltage difference between the DTMOSP-1 (IOSLV) and DTMOSP-2 (IOSLV) transistors when used as diodes; i.e. $\Delta V_{SG} = V_{SG1} - V_{SG2}$. The component are evaluated from 7 K to 295 K, at bias currents of 1 µA and from 10 µA to 100 µA with steps of 10 µA.

as they possess a slight curvature.

In conclusion, the measurement results obtained from the evaluation of the DTMOSP

(IOSLV) devices, performed in this work between 7 K and 295 K, indicate that the DTMOS transistor can be a key component for the production of wide range temperature sensors and cryogenic voltage references in the 22 nm FDSOI technology. Therefore, further studies of the DTMOS configuration in cryogenic FDSOI MOSFETs may provide significant contributions to the cryogenic analog MOS circuit design discipline.

3.2.4 NMOS (IOSLV)

The I_D characteristic curves of the NMOS (IOSLV) transistor, with the front gate voltage (V_{FG}) and environmental temperature as main variables, are shown in Figure 3.9. From these measurements, it can be observed that at CTs this component exhibits an electrical behavior similar to the one reported for FDSOI MOSFETs from another technology [88]. Thus, compared to its electrical characteristics at RT, the evaluated transistor exhibits at 7 K a higher on-state current, superior g_m performance, an improved subthreshold slope. However, the transistor also exhibits a V_{th} increase with temperature reduction. Besides, for all the evaluated temperatures, the V_{th} of the transistor can effectively be reduced by increasing its back gate voltage (V_{BG}).

In addition, Figure 3.10 compares the g_m/I_D characteristic curves of the NMOS (IOSLV) transistor at 7 K and 297 K, for $V_{BG} = 0\,V$ and $V_{BG} = 1\,V$. It is important to point out that, even though it is possible to match $V_{th\,@7K} \approx V_{th\,@297K}$ by setting $V_{BG} = 1\,V$, $g_m/I_{D\,@7K} \neq g_m/I_{D\,@297K}$ for the given DC operation point, due to cryogenic effects in the FDSOI MOS transistor. For example, the increase in charge carrier mobility at CTs due

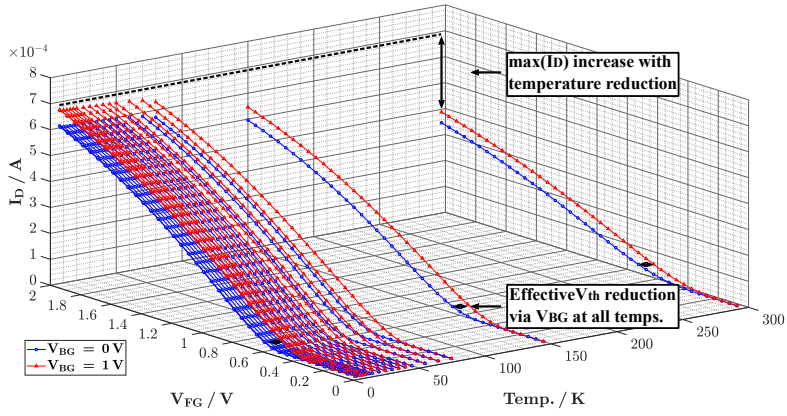


Figure 3.9: I_D characteristic curves of the NMOS (IOSLV) transistor with respect to V_{FG}, from 7 K up to 297 K; $V_{DS} = 400\,mV$, $V_{BG} = 0\,V$ and $V_{BG} = 1\,V$.

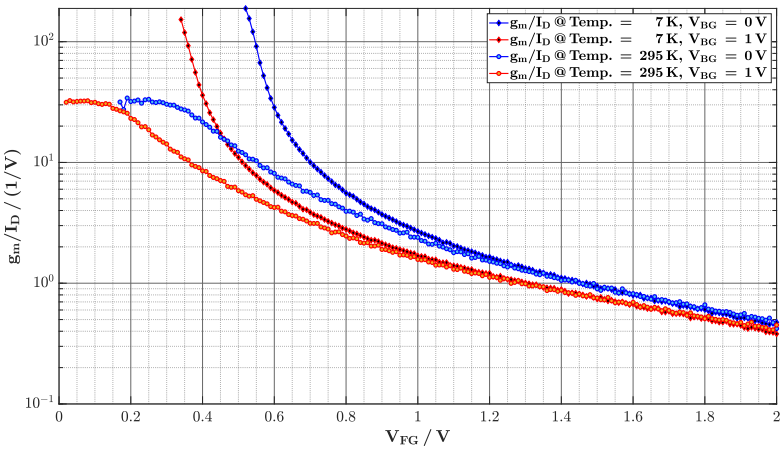


Figure 3.10: g_m/I_D characteristic curves of the NMOS (IOSLV) transistor with respect to V_{FG}, at 7 K and 297 K; $V_{DS} = 400\,mV$, $V_{BG} = 0\,V$ and $V_{BG} = 1\,V$.

Table 3.2: V_{th} of NMOS (IOSLV) transistor and its corresponding g_m/I_D, regarding temperature and V_{BG}. g_m/I_D values are obtained for $V_{FG} = V_{th}$ and $V_{DS} = 400\,mV$.

	V_{th}		g_m/I_D	
Temp.	297 K	7 K	297 K	7 K
V_{BG} **= 0 V**	0.43 V	0.58 V	18.16/V	41.49/V
V_{BG} **= 1 V**	0.25 V	0.39 V	18.64/V	43.85/V

to reduced phonon scattering results in $g_{m\,@7K} > g_{m\,@297K}$ [114, 120]. The V_{th} values of the evaluated transistor, and its corresponding g_m/I_D with respect to temperature and V_{BG}, are reported in Table 3.2. Here, the g_m/I_D values are obtained for $V_{FG} = V_{th}$ and $V_{DS} = 400\,mV$.

Moreover, a relevant characteristic of the g_m/I_D curves shown in Figure 3.10 is that when the NMOS (IOSLV) transistor is highly saturated, for example with $V_{FG} \geq 1.2\,V$, $g_m/I_{D\,@7K} \approx g_m/I_{D\,@297K}$. However, at these bias conditions the transistor is set for high power consumption. This, in turn, increases the heat generated by the transistor and the cooling power required from the cryogenic cooling system.

All of the presented facts must be considered during the development of cryogenic analog circuits with FDSOI MOSFETs. Since many performance metrics of the analog circuits depend on g_m/I_D[121]. Finally, the information obtained from the cryogenic characterization of the NMOS (IOSLV) transistor was employed in the development of the cryogenic PMU reported in Chapter 4.

3.3 Progress in the Development of Cryogenic Simulation Models

Although the MOSFETs provided by the 22 nm FDSOI technology are able to operate at CTs, their available simulation models are not rated for such temperatures. Therefore, these models cannot be used for the accurate design and pre-silicon verification of cryogenic ICs, since they do not represent the cryogenic electrical behavior of the FDSOI MOSFETs; i.e. the cryogenic phenomena that alter the MOS transistor operation are not considered by these simulation models, a circumstance common among many commercial IC technologies.

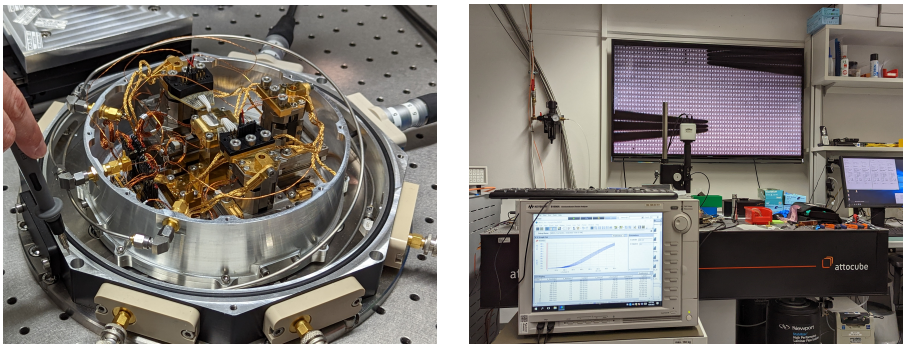
This is because the commercial IC manufacturers provide only simulation models that are rated for the 233.15 K to 393.15 K (−40 °C to 120 °C) range. Thus, the majority of the commercial IC design houses are seeking to develop electronic systems that operate inside such a temperature range. While the parties interested in the availability of cryogenic simulation models are mostly universities and research institutions that do not represent a relevant market segment. Consequently, the economic costs associated to the development of a cryogenic Process Development Kit (PDK) for ICs cannot be justified, at least from the financial perspective of the IC manufacturers. This circumstance will probably change with the appearance of commercial QC systems in the future.

Consequently, the research groups focused on the development of cryogenic ICs have decided to develop their own cryogenic simulation models [95]. One of those groups is QSolid, a consortium composed by 25 german institutions, from science and industry, that seek to develop the technologies needed for the construction and operation of a quantum computer [94].

The QSolid member institutions involved in the development of a cryogenic PDK for the 22 nm FDSOI technology are the Forschungszentrum Jülich - Central Institute of Engineering, Electronics and Analytics, Electronic Systems (ZEA-2), Fraunhofer - Institut für Photonische Mikrosysteme (IPMS), AdMOS, Racyics and Global Foundries [122]. Together, these research and industry institutions have designed different prototype dies for the cryogenic characterization, performance evaluation and modeling of the 22 nm FDSOI technology.

Figure 3.11 (a) shows one of the prototype dies mounted on the attoDRY800 cryocooling system for needle probing at different CTs. In particular, this die contains several semiconductor devices belonging to the 22 nm FDSOI technology. Furthermore, Figure 3.11 (b) shows the DC characterization process of an NMOS transistor contained in the prototype die, performed at a temperature close to 8 K.

An extensive DC characterization of the core MOSFETs has been conducted at RT and CTs. And, preliminary simulation models have been developed by using the BSIM-IMG



(a) (b)

Figure 3.11: (a) 22 nm FDSOI prototype die with several semiconductor devices, mounted on the attoDRY800 cryocooling system for needle probing. (b) DC characterization process of an NMOS transistor inside the die, at 8 K.

102-9.6 model. This is the first version of the multigate BSIM model with a built-in cryogenic extension [93]. As a result, the preliminary models are able to represent the electrical behavior of the core MOSFETs of the 22 nm FDSOI technology at CTs [123].

Even though the preliminary simulation models can only represent the cryogenic DC behavior of the core MOSFETs, this models may be employed as reference design tools for the development of cryogenic ICs. But most importantly, they are an initial milestone towards the development of a complete cryogenic PDK for the 22 nm FDSOI technology. Unfortunately, the cryogenic simulation models were not available during the design process of the cryogenic PMU presented in this work.

Chapter 4

Design and Electrical Characterization of Cryogenic PMU

This chapter presents the design and cryogenic electrical characterization of a voltage reference and a linear voltage regulator for temperatures between 6 K and 300 K. Both circuits are employed as evaluation circuits for the experimental performance evaluation of the 22 nm FDSOI MOS technology when used as platform for the development of cryogenic analog circuits, whose role is expected to become relevant for the development of future QC systems.

Also, the impact that MOSFET cryogenic phenomena have over these circuits is reported. Moreover, some of those phenomena are utilized for the cryogenic PMU design. In particular, focus is placed on the cryogenic threshold voltage (V_{th}) saturation, the g_m increase and the low frequency (LF) excess noise. The experimental results indicate that the cryogenic V_{th} saturation and the g_m increase can be used as circuit design tools, while the LF excess noise is a performance handicap for cryogenic analog circuits.

Additionally, the development of a PMU capable of cryogenic operation is proposed. For that purpose, the analog circuits studied in this chapter are employed as the main elements of the cryogenic PMU. Finally, a performance evaluation and comparison of the proposed cryogenic PMU with commercial PSUs and the state of the art voltage regulation systems, are provided.

4.1 Design and Characterization Methodology

As addressed in Chapter 3, a die containing super-low V_{th} I/O MOS devices is employed for the DC characterization of the 22 nm FDSOI technology in the 7 K-300 K range [124]. These type of devices are selected for developing a cryogenic PMU due to their reduced V_{th} and dielectric breakdown voltage, reaching 0.4 V and 2 V respectively at RT. Thus the DC parameters extracted from an NMOS device ($W/L = {}^{1\,\mu m}/_{0.32\,\mu m}$) are used as a reference in this work.

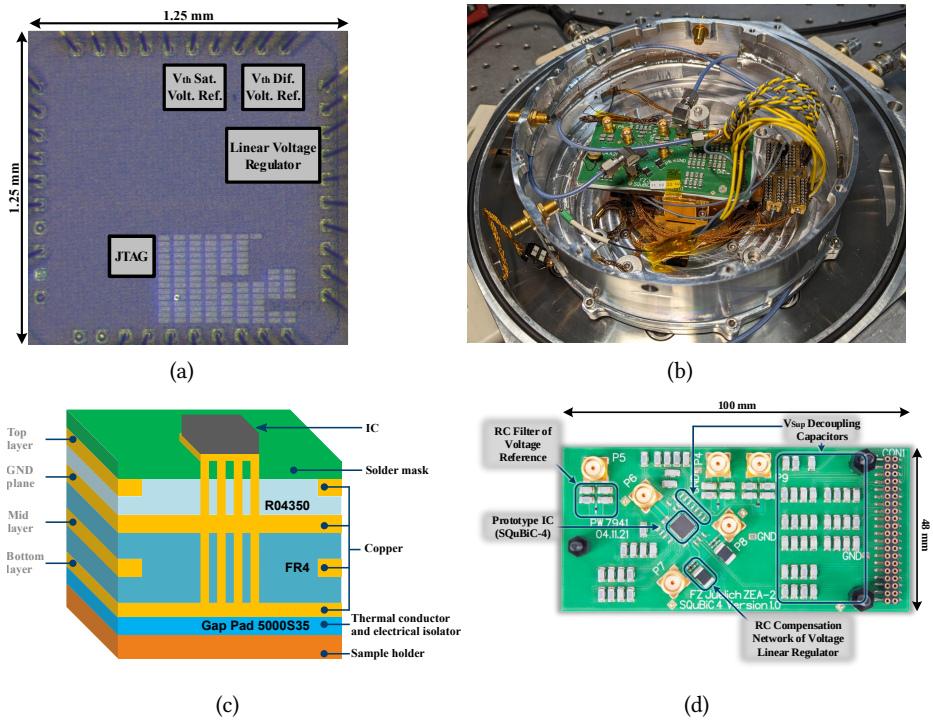


Figure 4.1: (a) Micrograph of prototype IC. (b) Experimental setup: PCB with prototype IC, mounted onto the GM cryocooler. (c) PCB stack used for the IC cryogenic thermalisation with electrical isolation from cold finger for ground loop noise coupling avoidance. (d) Detailed view of PCB used in the experiments.

With the information obtained by the 22 nm FDSOI technology characterization, a voltage reference and a linear voltage regulator configured via a JTAG digital communication interface, have been designed for cryogenic operation. It must be mentioned that the JTAG interface is only used for an initial configuration of the analog circuits. These circuits are incorporated into a prototype IC as in Figure 4.1 (a).

The experimental setup is displayed in Figure 4.1 (b). Inside the cryocooling station, the prototype ICs are mounted on PCBs specially designed for good thermal coupling with the cryocooler cold finger; Figure 4.1 (c) shows a sketch of the employed PCB stack. A detailed view of the PCB employed in this experiment is shown in Figure 4.1 (d). Due to the PCB size, a copper platform is used to mechanically couple it to the sample holder.

Since the cryocooling station uses a modified GM cold head unit (RDK-101E) employing

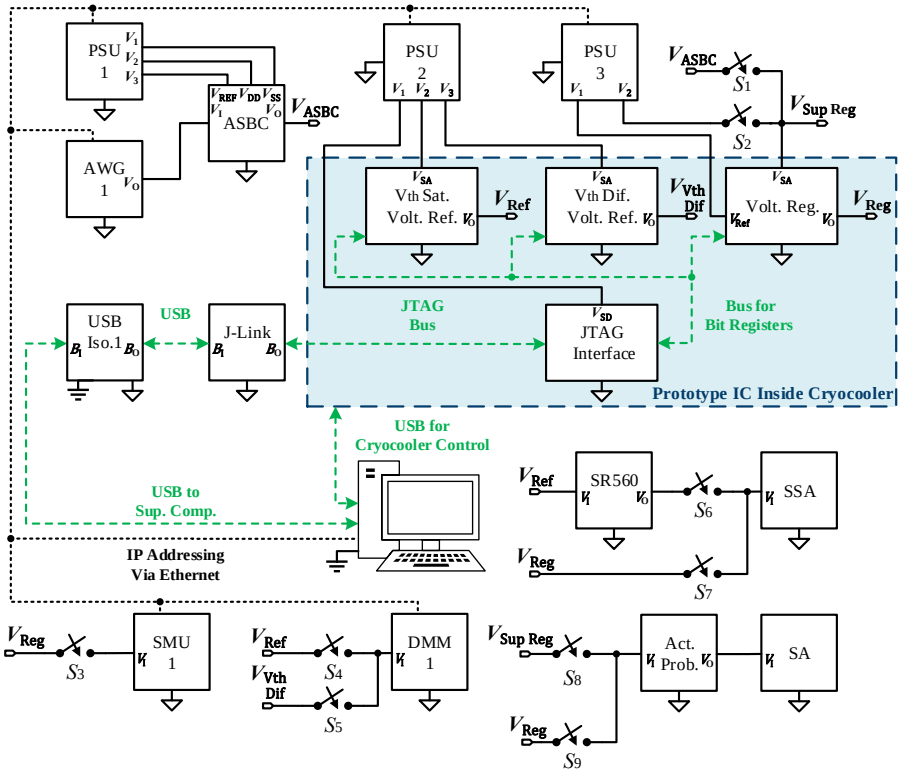


Figure 4.2: Simplified schematic representation of the setup used for the cryogenic test of the prototype IC.

a rotatory valve motor attached to its chassis, the setup coldest stage is electrically linked to the lab physical ground. As explained in section 2.3.1.2, such a condition leads to ground loop noise coupling and hence interference in the LF noise measurements [53].

In order to break the ground loop between the cryocooler cold plate and the prototype chip, a thermally conductive-electricallly isolating layer (Gap Pad 5000S35) is used as indicated in Figure 4.1 (c); an alternative layer, with similar properties, can be obtained by applying GE 7031 varnish over a cigarette paper substrate [37]. Moreover, the cables thermalisation is done without an electrical short between the test circuit ground and the lab physical ground. However, the minimum PCB temperature that can be reached with this ground isolation approach is 8 K. In contrast, without these ground isolation measures, the lowest PCB temperature in our setup is 6 K; a limit set by the cooling power of the cryocooler.

Also, to measure and control the PCB temperature, a sensing silicon diode (DT-670) is attached on the PCB and monitored during the electrical tests. So as to heat the PCB and perform electrical tests at higher temperatures, a heating resistor (PWR220T-35) attached to the cryocooler cold plate is used. For the electrical test of the prototype chips, DC supply voltage sources (N67050), digital multimeters (34470A), a spectrum analyzer (R&S FSU), a signal source analyzer (E5052B), a low noise amplifier (SR560), a JTAG debugger (J-Link PRO), an USB isolator (CN0550, evaluation board) and a support PC, are used. Figure 4.2 represents the testing scenarios addressed in this chapter. Here, switches ($S_1 - S_9$) are employed to indicate the connections requiring manual attachment in each test.

Notably, the experimental setup is presented prior to the circuit designs as to establish the framework in which the circuits operate. Moreover, due to the absence of suitable FDSOI MOSFETs simulation models for CTs, no cryogenic simulation results are provided. Hence, this limitation makes the experimental validation process a critical aspect of this work. Thus, the practical constraints influencing the circuit design choices and performance evaluation are expected to be clearly understood. Nonetheless, Appendix A compares the data obtained from the experimental evaluation of the analog circuits inside the prototype IC with the post-layout simulation results obtained by using the process corners. The comparison is performed at 300 K, 273.15 K and 233.15 K. In this way, the effectiveness of the IC design flow used in this work is demonstrated.

4.2 V_{th} Saturation Based Voltage Reference

Typically, MOS transistors experience changes of their electrical characteristics when operated at different temperatures. It is also known that the V_{th} of MOS transistors increases with temperature reduction [114]. In the case of the super-low V_{th} I/O NMOS transistor of the 22 nm FDSOI technology, Figure 4.3 shows the extracted V_{th} values over temperature via the linear extrapolation method [125].

As expected, the device V_{th} increases with temperature reduction; from 430 mV at 297 K, up to 578 mV at 60 K. However, it can be noticed that the V_{th} saturates from 60 K downwards. This phenomenon also occurs when the back-gate of the device is set to 1 V, with a V_{th} saturation of 387 mV. It is noteworthy that V_{th} tuning via the back-gate terminal is a characteristic offered by FDSOI MOS devices [36]. The cryogenic V_{th} increase and saturation is attributed to the ionization energy increase and the charger carriers freeze-out [126]. Furthermore, [120] argues that the cryogenic V_{th} behavior is due to the temperature dependence of the bulk Fermi potential and the density of interface traps. Besides, the V_{th} saturation has been reported for other technologies, including commercial 28 nm and 40 nm bulk CMOS technologies [120, 38]. While the cryogenic V_{th} saturation of 22 nm FDSOI technology is reported in [35], to the best of the author

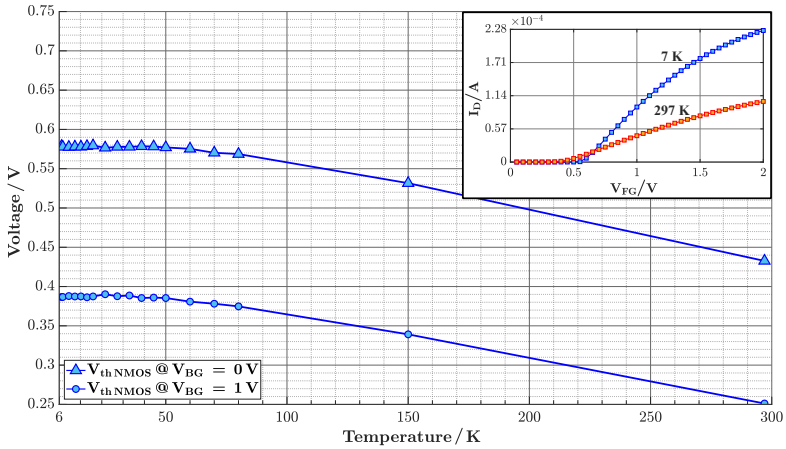


Figure 4.3: V_{th} extracted from an I/O NMOS ($W/L = {}^{1\,\mu\text{m}}/_{0.32\,\mu\text{m}}$) via the linear extrapolation method over temperature, for $V_{\text{BG}} = 0\,\text{V}$ and $V_{\text{BG}} = 1\,\text{V}$. Inset displays the I_{D} versus V_{FG} curve for 297 K and 7 K, at $V_{\text{DS}} = 0.1\,\text{V}$ and $V_{\text{BG}} = 0\,\text{V}$.

knowledge, it has not being intentionally used in the design of cryogenic analog circuits.

The circuit shown in Figure 4.4 exploits the cryogenic V_{th} saturation for the generation of a reference voltage. Here, the beta-multiplier and self-bias V_{FGS} current sources bias together a diode connected NMOS transistor to yield the reference voltage (V_{Ref}). When the transistors in Figure 4.4 operate in saturation, the self-bias V_{FGS} and beta-multiplier circuits will generate the currents I_{B1} and I_{B2}, as in Eqs. (4.1) and (4.2) [127, 59]. These currents are mirrored and supplied to M_{REF} via M_3 and M_4. Consequently, V_{Ref} can be approximated by means of Eq. (4.3).

$$I_{\text{B1}} = \frac{V_{\text{GS7}}}{R_1} = \frac{V_{\text{th}} + V_{\text{ov7}}}{R_1} \approx \frac{V_{\text{th}}}{R_1} \tag{4.1}$$

$$I_{\text{B2}} \approx \frac{L}{2 \cdot R_2^2 \cdot \mu C_{\text{ox}} \cdot W} \tag{4.2}$$

$$V_{\text{Ref}} \approx \sqrt{\frac{(I_{\text{B1}} + 0.25 \cdot I_{\text{B2}}) \cdot 2 \cdot L}{\mu C_{\text{ox}} \cdot W}} + V_{\text{th}} \tag{4.3}$$

In order to improve the circuit noise performance, an off-chip RC low-pass filter with a 5.2 Hz cut-off frequency, is added to its output; $R_{\text{Fil}} = 32.4\,\text{k}\Omega$ (metal film) and $C_{\text{Fil}} =$

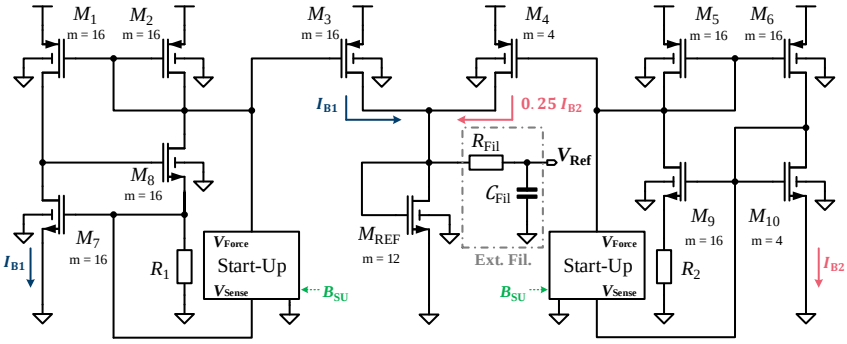


Figure 4.4: Voltage reference based on cryogenic V_{th} saturation.

940 nF (C0G). The voltage reference circuit is simple and does not employ calibration techniques to improve its V_{Ref} drift over temperature. It relies on the fact that a constant current biases and saturates the diode connected NMOS (M_{REF}) when the circuit is operated inside the V_{th} saturation temperature regime (6 K-50 K). This is a common situation for ICs intended to be used in large scale QC systems, since they are placed close to the physical quantum bits at environmental temperatures between 4 K and 10 K.

Although self-heating is a concern at CTs, its effect is also proportional to the electrical power dissipated by the devices [128, 129, 130]. Due to its low power dissipation, estimated to be 70 µW during the circuit design flow, a negligible self-heating is expected from this circuit. Additionally, start-up circuits are used to prevent the current sources from latching-up. They can either operate autonomously or be manually triggered through configuration bits via the JTAG interface.

The measured response of a prototype reference circuit to a supply voltage (V_{Sup}) sweep at 6 K, is shown in Figure 4.5. The output voltage (V_{Ref}) and supply current consumption (I_{Sup}) indicate that the circuit starts operating at V_{Sup} = 1.25 V with V_{Ref} = 576 mV and I_{Sup} = 38.3 µA. Besides, this operation condition is reached once the start-ups are no longer forcing the gates of the M_1-M_6 transistors to ground, as to prevent a zero current condition in the beta-multiplier and self-bias V_{FGS} circuits. Hence, the start-ups action is noticed as a swift increment of V_{Ref} and I_{Sup} in Figure 4.5, when V_{Sup} is between 1 V-1.2 V. Once the V_{FGS} of M_7 and M_{10} have reached saturation levels due to enough V_{Sup} available for the circuits operation, the start-ups stop forcing the M_1-M_6 gates to ground, as the zero current condition has been prevented.

Figure 4.6 shows the measured V_{Ref} over temperature, together with the V_{th} extracted from the I/O NMOS device (Figure 4.3). As it can be observed in Figure 4.3, V_{Ref} of sample 1 follows a trend similar to the one of the I/O NMOS V_{th} and deviates on average by

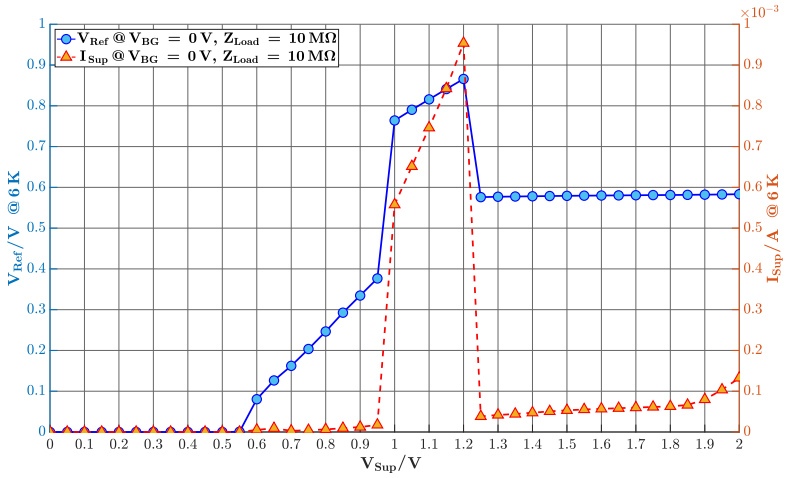


Figure 4.5: Measured output voltage and current consumption of voltage reference (sample 1) with respect to supply voltage (V_{Sup}), at 6 K.

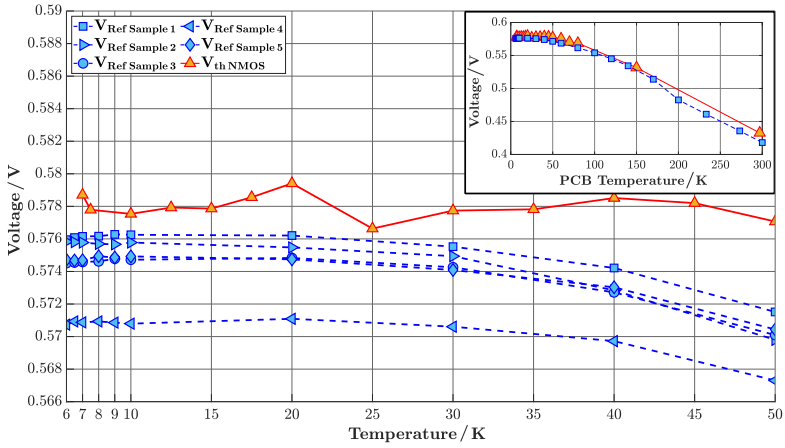


Figure 4.6: Measured output of voltage reference circuit over the temperature range of interest (6 K-50 K), with V_{Sup} = 1.25 V and V_{BG} = 0 V. The results correspond to 5 sample chips. Extracted V_{th} of I/O NMOS is added for comparison. Inset displays sample 1 data over a wider range (6 K-300 K).

2.5 mV from it at temperatures between 6 K to 50 K. A total of 5 reference circuits, embedded in different ICs, were tested. The responses of these samples are shown in Figure 4.6 and they differ slightly between each other, but all follow the I/O NMOS V_{th} trend

over temperature. Hence, these measurements demonstrate the reference feasibility at environmental temperatures between 6 K and 50 K.

4.2.1 Saturated V_{th} Difference as Alternative Working Principle

An alternative approach for the generation of a voltage reference quantity in CMOS ICs is the V_{GS} difference of two MOS transistors with different V_{th} characteristics. Thus, under the consideration that the transistors operate in saturation regime, their V_{GS} difference will render the V_{th} difference between both devices. And, if both V_{th} quantities have similar temperature sensitivities, the V_{th} difference will be a quantity with low temperature dependency. Figure 4.7 (a) shows an ideal circuit implementation that can produce the V_{GS} difference of two NMOS transistors as an output ($V_{Vth\,Dif}$). In this case, high threshold voltage (HV_{th}) and low threshold voltage (LV_{th}) devices are employed. Thus, for such a circuit, Eq. 4.4 can be defined via loop inspection.

$$V_{Vth\,Dif} = V_{GS1} - V_{GS2} \approx V_{HVth} - V_{LVth} \tag{4.4}$$

It is important to mention that the usage of the V_{th} difference for the generation of a voltage reference quantity was introduced by Robert A. Blauschild et al. [131] through the use of enhancement and depletion mode NMOS transistors. However, Robert A. Blauschild et al. pointed out that the V_{GS} difference has temperature sensitivity to the V_{th} quantities, bias drain currents and charge carriers mobilities of each device. Nevertheless, the V_{th} difference concept had been used in different ICs [132, 133].

In this work, the use of the V_{th} difference concept together with the cryogenic V_{th} saturation, is proposed for the generation of a voltage reference quantity suitable for the 6 K-50 K range. In such a temperature range, the V_{GS} difference temperature sensitivity to the V_{th} quantities is reduced due to the cryogenic V_{th} saturation of the two NMOS transistors. With that goal, the circuit shown in Figure 4.7 (c) is implemented.

In this circuit two transistors of equal size, but with different V_{th}, are biased via regulated cascode current sources (I_{Source} in Figure 4.7) and NMOS transistors. In this way, the diode connected transistors (M_1 and M_2) are biased in saturation to generate the output voltage $V_{Vth\,Dif}$. Also, Figure 4.7(b) shows a detailed view of the I_{Source} unitary cell used in this work [127]. The bias current flowing into M_1 and M_2 is controlled by configuration bits on-chip. These bits, set via a JTAG interface, determine the number of I_{Source} unitary cells and NMOS transistors that are connected in parallel. Besides, the V_{th} difference reference circuit in Figure 4.7 (c) is included into the prototype IC shown in Figure 4.1 (a), and it is electrically tested by following the methodology described in section 4.1.

The measured response of the V_{th} difference reference circuit to a DC sweep of V_{Sup} at 6 K, and under three current bias conditions of the diode connected transistors (M_1 and M_2),

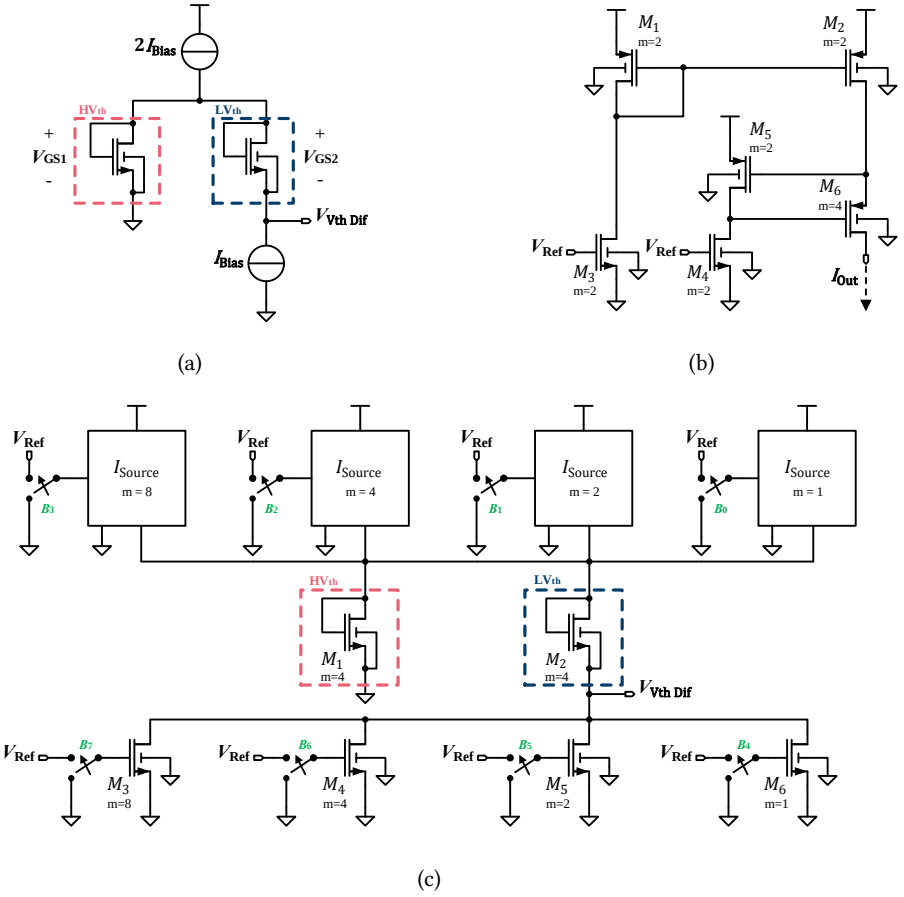


Figure 4.7: (a) Ideal V_{th} difference voltage reference. (b) Regulated cascode current source unitary cell ($I_{\text{Source, m = 1}}$). (c) Implemented V_{th} difference reference.

is shown in Figure 4.8. As it can be observed, at 6 K the proposed circuit starts operation with V_{Sup} = 1.25 V, similarly to the voltage reference circuit described in section 4.2.

This occurs because the output voltage generated by the V_{th} saturation reference is used to bias the V_{th} difference reference. Further, the output voltage ($V_{\text{Vth Dif}}$) and power consumption of the V_{th} difference reference changes with the DC bias current and V_{Sup} conditions. Thus, $I_{\text{Source, m = 2}}$ is the current bias condition with the lowest V_{Sup} sensitivity and power consumption characteristics. Consequently, when V_{Sup} = 1.65 V, the circuit line regulation and power consumption are 8.36 %/V and 48.15 µW, respectively.

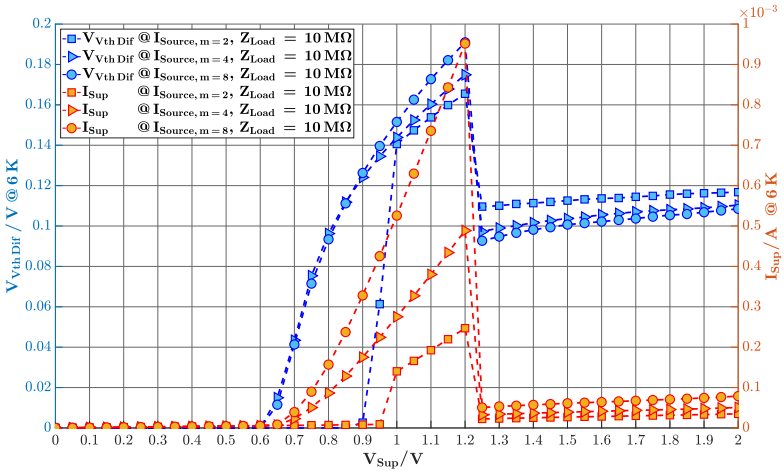


Figure 4.8: Measured output voltage and current consumption of V_{th} difference voltage reference circuit with respect to supply voltage (V_{Sup}), at 6 K. Three current bias configurations are evaluated: $I_{Source,\,m=2}$, $I_{Source,\,m=4}$ and $I_{Source,\,m=8}$.

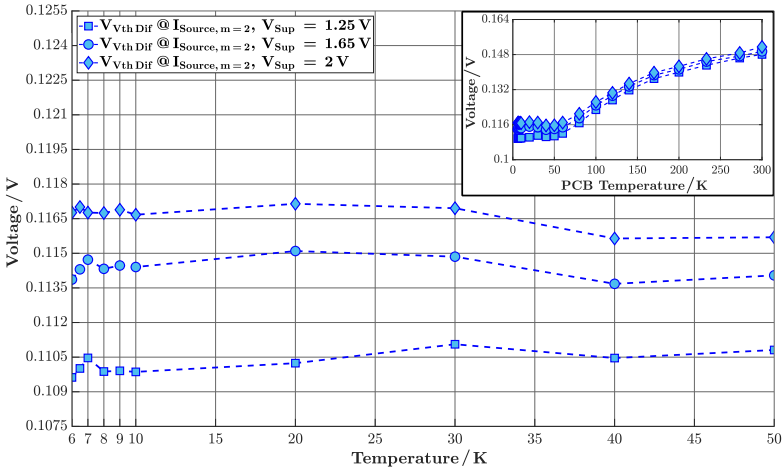


Figure 4.9: Measured output of V_{th} difference voltage reference circuit over the temperature range of interest (6 K-50 K), for V_{Sup} = 1.25 V, V_{Sup} = 1.65 V, and V_{Sup} = 2 V. The bias current condition is set to $I_{Source,\,m=2}$. Inset displays the measured data over a wider range (6 K-300 K).

Table 4.1: Measured electrical characteristic of V_{th} difference voltage reference.

	$I_{Source,\, m=2}$		
$V_{Sup.}$	**1.25 V**	**1.65 V**	**2 V**
$V_{Ref.}$ **@ 6 K**	109.6 mV	113.9 mV	116.8 mV
Pow. cons. @ 6 K	28 µW	48.15 µW	69.9 µW
Line regulation @ 6 K	8.69 %/V	8.36 %/V	8.15 %/V
Temp. coefficient @ 6 K-50 K	297.79 ppm/K	283.54 ppm/K	292.43 ppm/K

Figure 4.9 shows the output voltage measured from the V_{th} difference reference over temperature with $I_{Source,\, m=2}$, while V_{Sup} is set to 1.25 V, 1.65 V, and 2 V. As can be observed, in the 6 K-50 K temperature range, the output voltage remains stable with respect to temperature, as long as the V_{Sup} is fixed. This is because the output voltage sensitivity to V_{Sup} is associated to the NMOS transistors sinking the bias current of the LV_{th} devices, since the NMOS transistors do not operate as ideal current sources.

The temperature sensitivity of the output voltage correlates with the cryogenic V_{th} saturation phenomenon that is described in section 4.2, hinting to the fact that the HV_{th} NMOS and LV_{th} NMOS transistors experience the V_{th} saturation at the same temperature range. The reference output voltage changes between 7 mV to 5 mV, with respect to the established V_{Sup} value, over the temperature range of interest. Moreover, the reference circuit has a temperature coefficient of 283.54 ppm/K, when operated in the 6 K-50 K temperature range with $V_{Sup} = 1.65$ V.

The performance metrics, collected by the cryogenic electrical test of the circuit shown in Figure 4.7 (c), indicate that the V_{th} difference concept can be used to generate a voltage reference quantity over the 6 K-50 K temperature range with the 22 nm FDSOI MOS technology. However, the proposed saturated V_{th} difference voltage reference circuit is far from optimal, specially due to its sensitivity to V_{Sup}. In addition, a reference quantity close to 100 mV is relatively low. As to overcome these constraints, differential amplifiers could be employed in a subsequent design. Finally, Table 4.1 provides a summary of the cryogenic electrical characteristic of the saturated V_{th} difference voltage reference circuit proposed in this work.

4.3 Linear Voltage Regulator

Another electrical characteristic that changes in a MOS transistor facing CTs is its g_m [114]. Figure 4.10 shows the maximum g_m values obtained from the super-low V_{th} I/O NMOS device at different temperatures. As can be noticed, the device maximum g_m value increases by 184 % at 7 K, when compared to its value at 297 K. A similar scenario

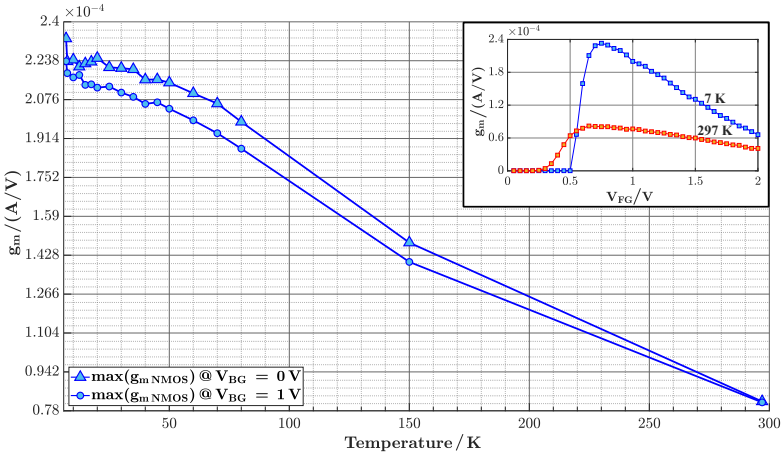


Figure 4.10: Maximum g_m of the I/O NMOS ($W/L = {}^{1\,\mu m}/_{0.32\,\mu m}$) over temperature, for $V_{BG} = 0\,V$ and $V_{BG} = 1\,V$. Inset displays the g_m versus V_{FG} curve for 297 K and 7 K, at $V_{DS} = 0.1\,V$ and $V_{BG} = 0\,V$.

occurs when the device back-gate is set to 1 V, but with a slight reduction of its maximum g_m value.

The g_m increase at CTs is linked to the carriers mobility increase due to reduced phonon scattering, while the shape change in the g_m vs V_{FG} curve (Figure 4.10, inset) is due to the Fermi-Dirac distribution exponential scaling [120]. As reported by [35], the cryogenic g_m increase phenomenon is expected in NMOS and PMOS devices of the 22 nm FDSOI technology.

In order to study the effects that the cryogenic g_m increase phenomenon has on an analog circuit, a linear voltage regulator is used as a evaluation circuit. Its circuit diagram is shown in Figure 4.11. If this circuit uses a high gain amplifier, its regulated DC output voltage can be approximated as in Eq. (4.5).

$$V_{Reg} \approx V_{IN\,Ref} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \tag{4.5}$$

The regulator uses an NMOS pass element whose back-gate terminal connection can be changed by an analog multiplexer controlled via JTAG interface. In this way it is possible to compensate for the V_{th} increase experienced by the pass element at CTs and to reduce the supply voltage level required by the regulator to start its operation. Although the use of an NMOS pass element will lead to a higher dropout voltage in contrast to a PMOS, it

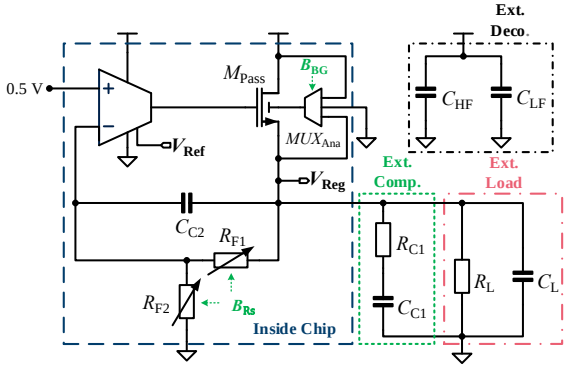


Figure 4.11: Linear voltage regulator circuit composed of an error amplifier, an NMOS pass element, a multiplexer, and a resistive feedback network. Off-chip compensation elements (metal film R_{C1} and polyphenylene-sulphide C_{C1}), with stable electrical characteristics over temperature, are used in as to guarantee stability at CTs.

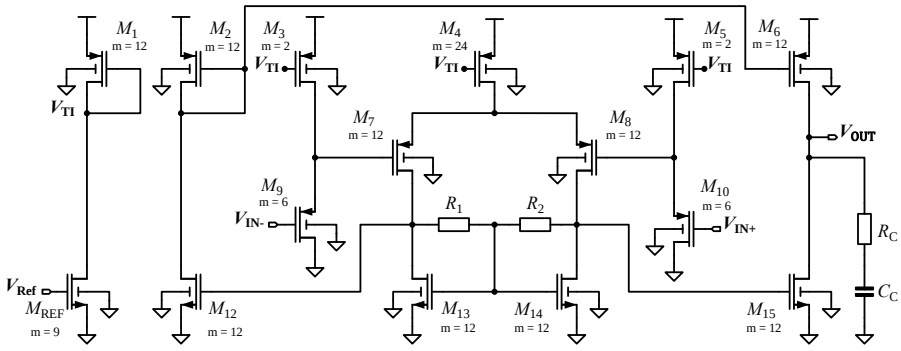


Figure 4.12: Differential amplifier in linear voltage regulator; its tail current is biased by the reference circuit (see Figure 4.4).

will also provide a superior power supply rejection ratio (PSRR); a requirement needed to supply high performance analog circuits [134].

Further, the feedback resistors values (R_{F1} and R_{F2}) can be modified for output voltage tuning via JTAG. Additionally, an off-chip compensation network with temperature stable electrical parameters, made up of a metal film resistor ($R_{C1} = 6.25\,\Omega$) and a polyphenylene-sulphide film capacitor ($C_{C1} = 47\,\text{nF}$), is used for stability at CTs [102].

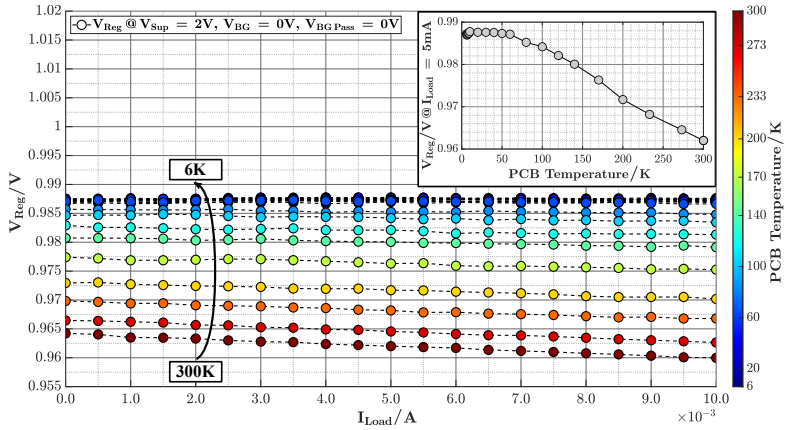


Figure 4.13: Measured regulator output voltage (V_{Reg}) in relation to current load (I_{Load}) and temperature; $V_{\text{IN Ref}} = 0.5\,\text{V}$, $R_{\text{F1}} = R_{\text{F2}}$, $V_{\text{BG}} = 0\,\text{V}$ and $V_{\text{Sup}} = 2\,\text{V}$. Inset shows V_{Reg} versus temperature; $I_{\text{Load}} = 5\,\text{mA}$.

The differential amplifier of the linear voltage regulator, shown in Figure 4.12, employs voltage followers for level shifting at their inputs and a resistive local common mode feedback at its core. Its open loop gain (A_{DA}) is approximated by Eq. (4.6) [135]. Since the regulator loop gain (A_{LG}) is proportional to A_{DA} as in Eq. (4.7), the load regulation (LR) and PSRR are also depending on A_{DA} via A_{LG}; as shown by Eqs. (4.8) and (4.9) [134].

As A_{DA} is proportional to the g_{m} of the MOS devices, it is expected that at CTs its magnitude increases due to the g_{m} increase with temperature reduction. This results in an improvement of the regulator LR and PSRR.

$$A_{\text{DA}} \approx g_{\text{m}_{7,8}} \cdot g_{\text{m}_{12,15}} \cdot (R_{1,2} || r_{o_{7,8}} || r_{o_{13,14}}) \cdot Z_{\text{out}} \tag{4.6}$$

$$A_{\text{LG}} \approx A_{\text{DA}} \cdot \frac{R_{\text{F2}}}{R_{\text{F1}} + R_{\text{F2}}} \tag{4.7}$$

$$\text{LR} \approx \frac{1}{g_{\text{m}_{\text{M Pass}}} \cdot A_{\text{LG}}} \tag{4.8}$$

$$\text{PSRR} \approx \frac{1}{g_{\text{m}_{\text{M Pass}}} \cdot r_{o_{\text{M Pass}}} \cdot A_{\text{LG}}} \tag{4.9}$$

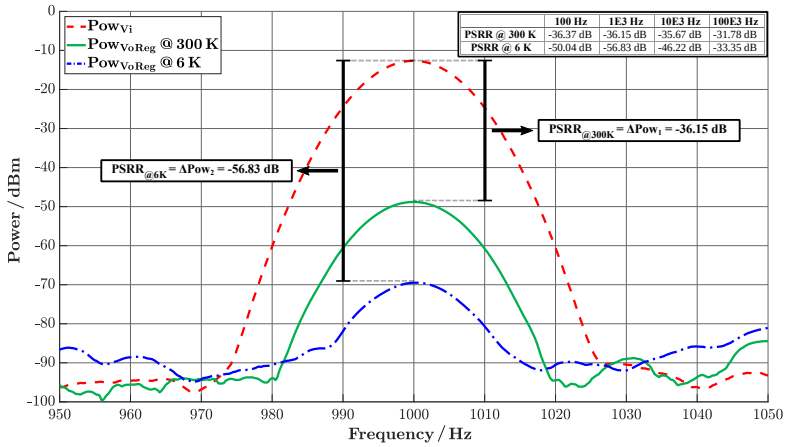


Figure 4.14: Measured regulator PSRR via spectrum analysis at 1 kHz, at 6 K and 300 K; $V_{\text{IN Ref}} = 0.5\,\text{V}$, $R_{\text{F1}} = R_{\text{F2}}$, $V_{\text{BG}} = 0\,\text{V}$, $V_{\text{Sup}} = 2\,\text{V}$. Inset provides the PSRR values measured at other frequencies.

Figure 4.13 shows the measured response of the prototype regulator in relation to load current (I_{Load}) and temperature, with $V_{\text{IN Ref}} = 0.5\,\text{V}$, $R_{\text{F1}} = R_{\text{F2}}$, $V_{\text{BG}} = 0\,\text{V}$ and $V_{\text{Sup}} = 2\,\text{V}$. $V_{\text{IN Ref}}$ is set to 0.5 V by an external voltage source in order to evaluate the regulator performance with regard to temperature. The mean regulator output voltage (V_{Reg}) is 962 mV at 300 K and it increases to 987 mV at 6 K. These changes indicate that an increase in A_{LG} reduces the regulator error and sets V_{Reg} closer to 1 V, the ideal output value. However, due to the amplifier input offset voltage, the voltage regulator cannot reach its ideal output voltage; i.e. $V_{\text{Reg}} \neq 1\,\text{V}$. Similarly, the regulator LR changes from 424 mV/A at 300 K, to 30 mV/A at 6 K; an improvement of 92.92 %.

The regulator PSRR is shown in Figure 4.14 for 1 kHz, at 300 K and 6 K. At 300 K, the measured PSRR is −36.15 dB, while at 6 K it is −56.83 dB, corresponding to an improvement of 20.68 dB. The inset in Figure 4.14 indicates the measured PSRR for additional frequencies. Suffices to mention that the active signal biasing circuit described in Appendix B is used for the voltage regulator PSRR characterization, together with an active probe (41800A) and a spectrum analyzer (R&S FSU). Based on the measurements results previously described and Eqs. (4.6) – (4.9), it can be inferred that the g_{m} increase is the main factor leading to the cryogenic improvement of the regulator LR and PSRR.

Furthermore, Figure 4.15 shows the regulator response to a voltage supply sweep at 6 K, with different pass element back-gate configurations. With the back-gate set to ground, the regulator needs $V_{\text{Sup}} = 1.75\,\text{V}$ to start operation. In contrast, by setting the back-gate to the supply rail, the regulator needs $V_{\text{Sup}} = 1.5\,\text{V}$ to operate. Hence, a reduction of

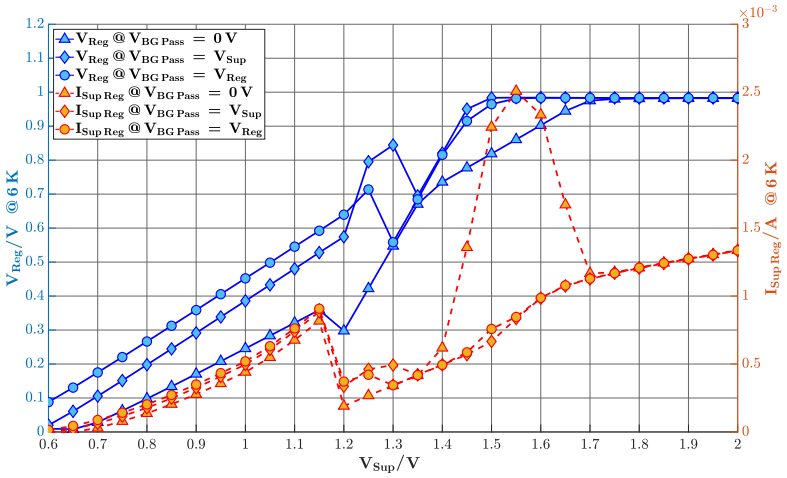


Figure 4.15: Measured regulator output voltage (V_{Reg}) and supply current ($I_{Sup\,Reg}$) at 6 K, in relation to supply voltage (V_{Sup}) and several back-gate settings for the NMOS pass element.

250 mV is obtained. The regulator has an idle power consumption of 3.3 mW. Most of this consumption is produced by the enforced operation of the pass element in saturation due to cryogenic stability concerns, while our design estimations indicate that the error amplifier consumes 0.1 mW. An improvement in power consumption can be achieved by incorporating cryogenic simulation models into the regulator design flow. Unfortunately, cryogenic simulation models have not been available for the development of the prototype chip presented in this work. Despite this, the regulator operates at temperatures between 6 K and 300 K.

4.4 Low Frequency Electrical Noise

In electronics, noise is defined as any electrical signal present in a circuit other than the desired signal, and is considered an undesired phenomenon since it can disrupt the functionality of a circuit [53]. Regarding cryogenic ICs for QC systems, it is expected that MOS transistors will produce most of their intrinsic noise. Moreover, since the noise produced by these ICs may interfere with the qubit devices operations, the study of the MOS transistor cryogenic LF noise has gained relevance [72, 66, 79].

According to Ghibaudo et al., the MOS transistor LF noise is dominated by the carrier number fluctuation and the mobility fluctuation phenomena, with a linear temperature

dependence [64]. Therefore, a decrease of the MOS transistor LF noise is expected with temperature reduction. However, it has been found that this is not the case for temperatures lower than 100 K. A higher amount of LF noise has been measured at 4 K than at 300 K in FDSOI and planar-bulk MOS technologies [34, 65].

Moreover, it was recently demonstrated that at 2.5 K the LF noise is correlated with the MOS transistor SiO_2 interface traps density [66]. These traps produce energy states localized near the conduction-band, which at CTs have a strong interaction with the Fermi energy level. Hence, the capture and release of charge carriers induced by these traps substantially contribute to the MOS transistor LF noise.

Even though the mechanism generating the cryogenic LF excess noise has been identified, a model that can describe it has not been developed. On this basis, it is logical to assume that the LF noise produced by analog MOS circuits developed in 22 nm FDSOI is higher at CTs than at room temperature. However, how much difference exists between the LF noise spectra produced by a circuit operated at these temperatures is unknown. So as to shed light on this uncertainty, the LF noise produced by the prototype circuits is characterized at 8 K and 300 K. Moreover, while performing the characterization of the intrinsic LF noise from the prototype circuits, the ground isolation approach described in section 4.1 is used.

Due to the voltage reference circuit limited current drive capability and the noise measurement equipment input characteristics (SSA, E5052B with $C_{\text{in}} = 1410\,\mu\text{F}$ and $R_{\text{in}} = 50\,\Omega$ for AC coupling), a low noise amplifier (LNA, SR560 with $C_{\text{in}} = 25\,\text{pF}$, $R_{\text{in}} = 100\,\text{M}\Omega$ and $R_{\text{out}} = 50\,\Omega$) is added to the noise measurement setup as intermediate stage. Additionally, the SR560 has a 1 MHz bandwidth and an average input noise voltage amplitude spectral density of $4\,^{\text{nV}}/\sqrt{\text{Hz}}$, when set to a voltage gain of 60 dB; a description of the voltage noise measurement setup calibration procedure is provided in Appendix C.

Figure 4.16 shows the voltage noise spectra measured at the output of the voltage reference circuit while operated at 8 K and 300 K. As can be observed, for low frequencies the voltage amplitude spectral density produced by this circuit at 8 K is higher than the one at 300 K. The difference between both spectra can be quantified by means of their RMS voltage noise evaluated at the 10 Hz – 10 kHz LF bandwidth, as indicated by Eq. (4.10); the RMS voltage noise definition provided by Eq. (2.8) in Chapter 2, is considered.

$$V_{\text{n,rms}} = \sqrt{\int_{f_1}^{f_2} v_n^2(f)\,df} \tag{4.10}$$

Beyond 10 kHz both spectra are covered by the measurement equipment noise floor. It suffices to mention that the measured noise spectra are integrated by means of the trapezoidal numeric method. Thus, $V_{\text{Ref, n @ 8 K}} = 9.08\,\mu\text{V}_{\text{rms}}$ and $V_{\text{Ref, n @ 300 K}} = 4.73\,\mu\text{V}_{\text{rms}}$, indicating that the LF noise at 8 K is 1.92 times higher than the one at 300 K. Concerning

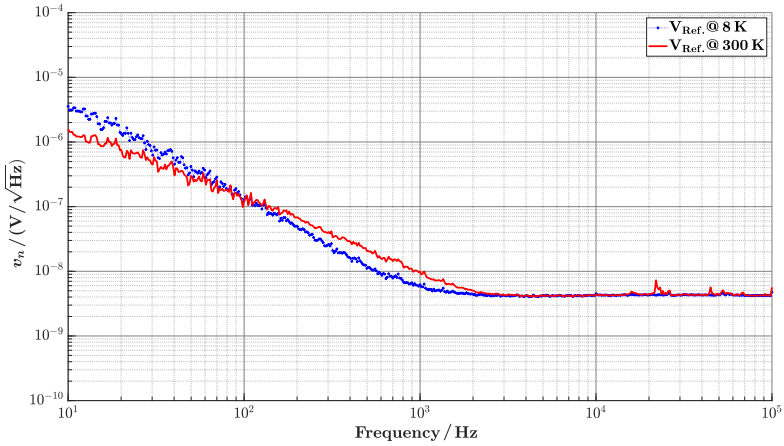


Figure 4.16: Voltage noise amplitude spectral density measured from the voltage reference circuit output at 8 K and 300 K; $V_{BG} = 0$ V and $V_{Sup} = 2$ V.

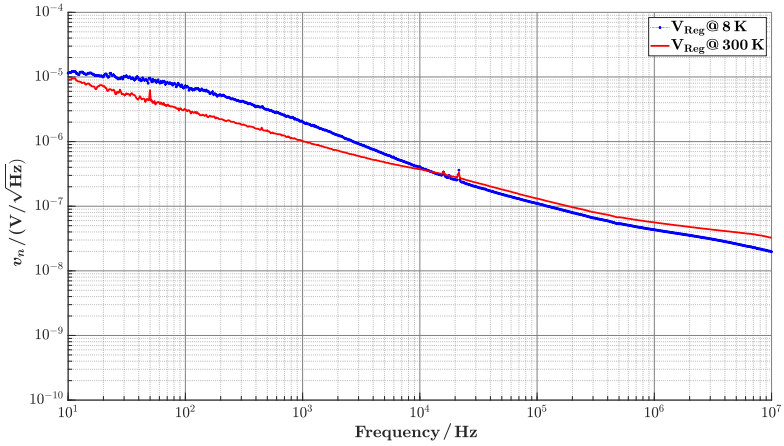


Figure 4.17: Voltage noise amplitude spectral density measured from the voltage regulator circuit output at 8 K and 300 K; $V_{IN\,Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V, $I_{Load} = 5$ mA and $V_{Sup} = 2$ V.

the regulator, since it can drive the input port of the E5052B, it does not require the SR560 as an intermediate stage. Figure 4.17 shows the voltage noise spectra measured from the regulator output at 8 K and 300 K. Similarly to the previous case, in the LF bandwidth the noise spectrum at 8 K is higher than the one at 300 K.

Table 4.2: Measured RMS voltage noise values in the study.

BW	10 Hz – 10 kHz		10 Hz – 10 MHz	
Temp.	8 K	300 K	8 K	300 K
$V_{\mathbf{Ref,\,n}}$	9.08 μV_{rms}	4.73 μV_{rms}	N. A.	N. A.
$V_{\mathbf{Reg,\,n}}$	157.90 μV_{rms}	83.97 μV_{rms}	194.79 μV_{rms}	173.39 μV_{rms}

Though, around 10 kHz both spectra reach similar values and at higher frequencies the 8 K noise spectrum is lower than the 300 K one. This behavior signals a decrease in the contribution of the LF noise and an increase of the white noise contribution to the voltage noise spectrum at 8 K. Since the measured decrease in voltage noise above 10 kHz is similar to the white noise reduction reported for MOSFETs at CTs [79].

By evaluating the regulator RMS noise at the LF bandwidth via Eq. (4.10), it is found that $V_{\mathrm{Reg,\,n\,@\,8\,K}} = 157.90\,\mu V_{rms}$ and $V_{\mathrm{Reg,\,n\,@\,300\,K}} = 83.97\,\mu V_{rms}$. The regulator LF noise at 8 K is 1.88 times higher than the one at 300 K. It is worth noting that in both circuits the LF RMS voltage noise increases roughly by 90 % at 8 K, when compared to its value at 300 K. Correlating with the cryogenic LF excess noise behavior reported for FDSOI transistors [34]. Table 4.2 provides the RMS noise values measured in this study.

4.5 Discussion and Performance Comparison

The cryogenic V_{th} increase is a phenomenon experienced by all the cryogenic analog MOS circuits. Thus, their voltage supply requirements becomes higher. This situation will encourage the use of low voltage supply circuit techniques in cryogenic analog systems [136]. In the case of circuits based on FDSOI MOS transistors, back-gate V_{th} tuning is an effective way for the voltage supply requirements reduction of the cryogenic analog MOS circuits. This is demonstrated by the linear voltage regulator studied in section 4.3. Regarding bulk-MOS technologies, V_{th} tuning at CTs can be achieved via the forward body biasing [137]. Therefore, it is expected that the next generation of cryogenic analog MOS circuits uses the V_{th} tuning as a fundamental circuit technique.

Concerning the cryogenic V_{th} saturation, although it can be used as working principle for the generation of a reference voltage, its use also involves some limitations. For instance, the measurement results provided in section 4.2 indicate that the reference circuit is sensible to process variations. In addition, the cryogenic V_{th} saturation may not occur in all the MOS technologies. Hence, the development of a robust cryogenic voltage reference circuit demands the use of a MOS technology that has been characterized and modeled for cryogenic operation.

Table 4.3: Voltage reference comparison with the state of the art.

	[138]	[118]	[119]		This work
Technology	SiGe BiCMOS	40 nm CMOS	40 nm CMOS		22 nm FDSOI
Ref. device	SiGe HBT	DTMOS	PMOS	DTMOS	NMOS
Temp. operation range	0.7 K – 293 K	4 K – 300 K	4 K – 300 K	4 K – 300 K	6 K – 50 K
V_{Sup} min.	3.3 V	1.8 V	0.97 V	0.9 V	1.25 V
V_{Ref}	1.156 V @ 0.7 K	0.81 V @ 4 K	0.71 V @ 4 K	0.6 V @ 4 K	0.576 V @ 6 K
Pow. cons.	130.35 µW	132 µW	7.37 µW	7.26 µW	47.88 µW
Line regulation	N.A.	8.3 %/V	1.2 %/V	1.1 %/V	1.652 %/V
Temp. coefficient	160 ppm/K	834 ppm/K	539 ppm/K	436 ppm/K	300 ppm/K
PSRR	N.A.	−23.4 dB	N.A.	N.A.	−46.14 dB @ 6 K, 1 kHz
Low frequency RMS noise	N.A.	N.A.	N.A.	N.A.	9.08 μV_{rms} @ 8 K, 10 Hz – 10 kHz
Area inside IC	N.A.	0.0004 mm^2	0.009 mm^2	0.009 mm^2	0.006 mm^2

The g_m increase experienced by MOS transistors at CTs is a phenomenon that can be used to increase the gain of cryogenic amplifiers, as demonstrated by the results presented in section 4.3. However, for many topologies the gain is not the only electrical parameter relying on g_m; e.g. the circuit stability may also be influenced by it [54]. Thus, a sensitivity analysis of the circuit parameters with regard to higher g_m values must be added into the design process of cryogenic amplifiers.

Regarding the LF excess noise, based on the information available in the state of the art literature and the results presented in section 4.4, it is clear that it will affect most of the cryogenic analog MOS circuits. Hence, the LF excess noise can become a hindering performance factor for many circuit blocks in cryogenic analog and mixed-signal ICs; e.g. current biases and voltage references circuits. Potentially influencing the performance of applications like quantum dot formation in semiconductor qubits, where DC voltages generated at CTs are supplied to the gates of the qubit devices [139]. Consequently, low noise circuit techniques and topologies must be implemented to counteract this cryogenic MOS phenomenon.

A comparison between the circuits studied in this work and the state of the art is provided in the Tables 4.3 and 4.4 [102, 138, 118, 119]. The voltage reference in this work is simple and has a competitive temperature coefficient of 300 ppm/K, when operated in the 6 K-50 K range. Moreover, its PSRR is −46.16 dB at 6 K, while its LF RMS voltage noise is 9.08 μV_{rms} at 8 K. Regarding this work voltage regulator, its LR, PSRR, and

Table 4.4: Voltage regulator comparison with the state of the art.

	[102]		This work
Technology	Discrete components based design		22 nm FDSOI
Pass element	NMOS (TSM2314)		NMOS
Nominal V_{Sup}	V_{DD} = 3.3 V (Error amplifier) V_{IN} = 1.5 V (Pass element)		2 V
Error amplifier	AD8605	TLV271	Custom
V_{Reg}	1.0086 V @ 4 K, V_{Ref} = 0.6 V, Z_{Load} = 100 Ω	1.0106 V @ 4 K, V_{Ref} = 0.6 V, Z_{Load} = 100 Ω	0.987 V @ 6 K, $V_{Ref.}$ = 0.5 V, I_{Load} = 5 mA
Idle pow. cons.	4.46 mW @ 4 K	0.1 mW @ 4 K	3.3 mW @ 6 K
Max. load current	300 mA @ 4 K	300 mA @ 4 K	10 mA @ 6 K
Load regulation	1.59 mV/A @ 4 K	0.81 mV/A @ 4 K	22 mV/A @ 6 K
PSRR	−75.1 dB @ 4 K, 1 kHz	−76.4 dB @ 4 K, 1 kHz	−56.83 dB @ 6 K, 1 kHz
Low frequency RMS noise	2.64 μV_{rms} ★ @ 4 K, 100 Hz – 100 kHz	7.03 μV_{rms} ★ @ 4 K, 100 Hz – 100 kHz	157.90 μV_{rms} @ 8 K, 10 Hz – 10 kHz
Area inside IC	N.A.	N.A.	0.075 mm^2

★ Values calculated from data depicted in a graphical format.

LF RMS voltage noise metrics fall behind the state of the art performance. However, the solutions presented in [102] rely on discrete components and need at least 3.3 V of voltage supply. In contrast, this work regulator operates with lower V_{Sup} and, excluding the compensation network, its components are integrated on chip. In addition, it is important to highlight that the regulator presented in this work can operate along the 6 K-300 K range, a feature not common in commercial monolithic regulators [102].

Furthermore, the circuits studied in this work served as evaluation circuits for gaining an insight into the design and electrical characterization of cryogenic analog CMOS ICs. Allowing the acquisition of experience and knowledge required for the development of optimized cryogenic analog circuits.

4.6 Cryogenic PMU

After evaluating the electrical performance of the V_{th} voltage reference and linear voltage regulator circuits from RT down to 6 K, their operation as a system is tested for the proposed cryogenic PMU. For that purpose, the simple system design shown in Figure 2.13 is employed. Thus, the output voltage generated by the V_{th} saturation reference

is used as the linear regulator input. Besides, only one supply rail biases both circuits. Therefore, since $V_{Ref} = V_{IN\,Reg} \approx 576\,mV$ at 8 K, it is expected that the cryogenic PMU regulated output (V_{PMU}) be close to 1.2 V when $R_{F1} = R_{F2}$. It is important to note that V_{Ref} also biases the tail current of the differential amplifier used in the linear voltage regulator.

In order to test the cryogenic PMU functionality and stability, this system is electrically tested with a V_{Sup} activation pulse that transitions from 0 V to 2 V, while the back-gate terminal of M_{Pass} device used in the voltage regulator is tied to V_{Sup}; by setting $V_{BG\,Pass} = V_{Sup}$, the regulator supply requirements are reduced, as shown in Figure 4.15. Moreover, $V_{BG} = 0\,V$, $Z_{Load} = 220\,\Omega$, and Temperature $= 8\,K$ are set as testing conditions. Hence, Figure 4.18 shows the measured transient response of the cryogenic PMU, obtained by means of a digital oscilloscope (InfiniiVision 4000 X-Series) and a high-sensitivity current probe (N2820/1A) [140, 141]. As can be observed, V_{PMU} reaches an stable condition after its activation transition, which has a approximate length of 20 ms. The duration of this transition is associated to the V_{th} saturation reference slow response, since its output does not have a high current drive capability. In contrast, the measured I_{Sup} quickly stabilizes to an average value of 6.7 mA, indicating that the activation of the linear regulator is faster. After the cryogenic PMU activation transition, the measured mean value of V_{PMU} is 1.19 V.

As to adjust V_{PMU}, the values of R_{F1} and R_{F2} are modified via JTAG interface. The tuning functionality is showcased by the transient measurement displayed in Figure 4.19, in which V_{PMU} is changed to different values between 0.8 V and 1.15 V. Moreover, it is possible to set $V_{PMU} \approx 1\,V$ with $V_{IN\,Reg} \approx 576\,mV$. Thus, in this case the voltage regulator characteristics should be similar to the ones presented in section 4.3.

A significant characteristic of any voltage regulation system is its output voltage noise. Consequently, the measured voltage noise spectrum from the cryogenic PMU, at 300 K and 8 K, is shown in Figure 4.20, with $V_{Sup} = 2\,V$, $V_{PMU} \approx 1\,V$, $V_{BG\,Pass} = V_{Sup}$, $V_{BG} = 0\,V$, and $Z_{Load} = 220\,\Omega$ set as electrical testing conditions. In addition, the output voltage noise of several commercial PSUs (B2902A, E3634A, E36312A and N6705C) is also characterized at 300 K, with $V_{Out} = 1\,V$ and $Z_{Load} = 220\,\Omega$ [142, 143, 144, 145]. As to complete the performance comparison, the reported voltage noise spectra from the cryogenic voltage regulators presented by Homulle et al., are also added [102]; in this case, the data plotted in Figure 4.20 is obtained from information depicted in graphical format. In order to perform a quantified comparison of all the voltage regulation systems under consideration, their noise spectra are integrated by means of Eq. 4.10. As a result, the integrated voltage noise ($V_{n,rms}$) values reported in Table 4.5 are obtained. Also, relevant technical information associated with each voltage regulation system is also included in Table 4.5.

It can be noticed that when the B2902A PSU is coupled with its low pass filter add-on, this unit provides the lowest $V_{n,rms}$, when the evaluation BW covers the 10 Hz-100 MHz range. However, one inconvenience of the B2902A is the fact that the ground reference

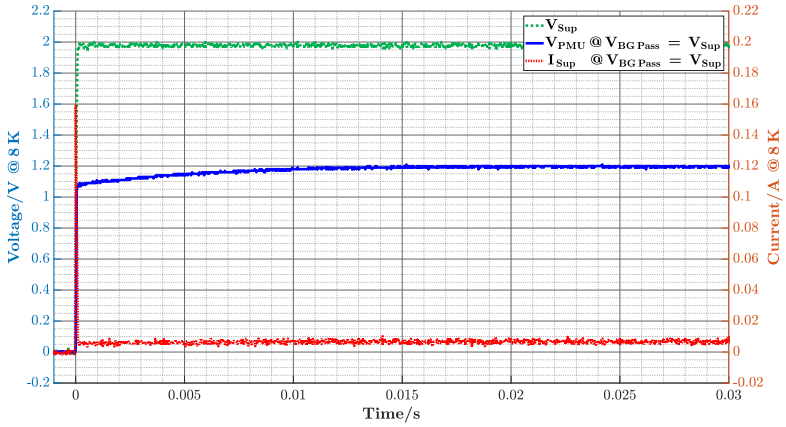


Figure 4.18: Cryogenic PMU transient response to a voltage supply (V_{Sup}) activation pulse, from 0 V to 2 V, measured at 8 K. The regulated output voltage (V_{PMU}) and current consumption (I_{Sup}) of the cryogenic PMU, correspond to $V_{\text{BG Pass}} = V_{\text{Sup}}$, $V_{\text{BG}} = 0\,\text{V}$, $R_{\text{F1}} = R_{\text{F2}}$ and $Z_{\text{Load}} = 220\,\Omega$.

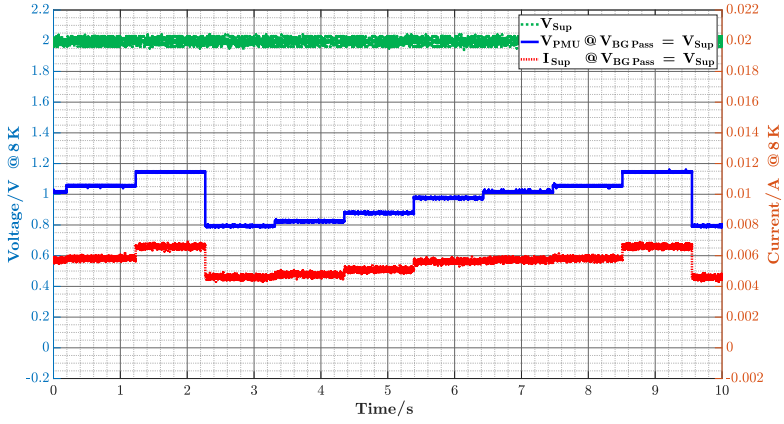


Figure 4.19: Measured transient response of the cryogenic PMU for the demonstration of its output voltage (V_{PMU}) tuning functionality at 8 K, when $V_{\text{BG Pass}} = V_{\text{Sup}}$, $V_{\text{BG}} = 0\,\text{V}$ and $Z_{\text{Load}} = 220\,\Omega$.

of its output voltage port is linked to the physical ground of its AC power supply port, representing a potential ground loop noise source. In contrast, the E36312A is the PSU with the lowest $V_{\text{n,rms}}$ that posses an output voltage port that is isolated from its AC power supply port. Nevertheless, both PSUs are bulky compared to an IC and they need

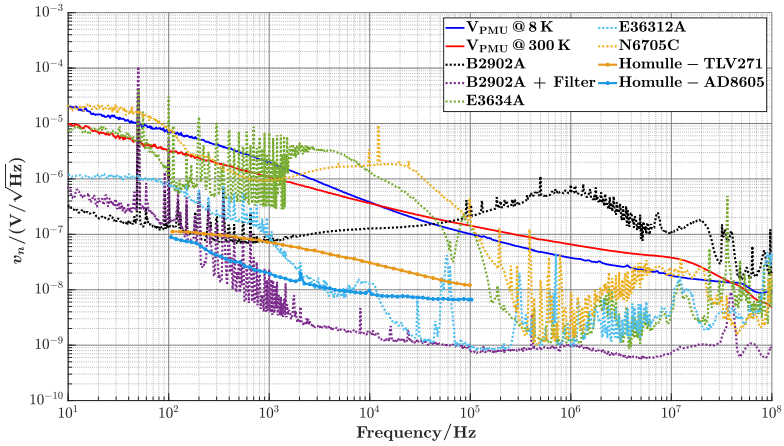


Figure 4.20: Noise performance comparison of the cryogenic PMU with commercial PSU and the state of the art [102]. The regulated output voltages of the cryogenic PMU and all the commercial PSU evaluated in this work, are set to 1 V and loaded with $Z_{Load} = 220\,\Omega$. Besides, for the cryogenic PMU, $V_{Sup} = 2\,V$, $V_{BG\,Pass} = V_{Sup}$ and $V_{BG} = 0\,V$.

to be operated at RT; characteristics that are not ideal for the scalability of future QC systems.

Conversely, the cryogenic PMU in this work has an smaller size and can be operated at CTs close to 8 K. However, when compared to the commercial PSUs, its load regulation and output voltage tuning characteristics show lower performance. Its $V_{n,rms}$ is slightly higher that the one from the E36312A PSU. And, when considering the fact that the cryogenic voltage regulators implemented with commercial discrete components by Homulle et al. produce low voltage noise, the possible implementation of a high performance and low noise monolithic cryogenic PMU seems strongly feasible.

Nonetheless, the cryogenic PMU presented in this work is the outcome of a first IC design trial, and it is expected that the results obtained by this investigation support the advancement of the cryogenic analog MOS circuit design discipline.

Table 4.5: Noise performance comparison of the cryogenic PMU with commercial PSU and the state of the art [102]. Integrated voltage noise ($V_{n,rms}$) correspond to the information depicted in Figure 4.20.

	Integrated voltage noise ($V_{n,rms}$)	Technical details
This work PMU	240.02 μV_{rms} @ 300 K, 10 Hz – 100 MHz 227.10 μV_{rms} @ 8 K, 10 Hz – 100 MHz	Powered by batteries during electrical test
B2902A	1200 μV_{rms} @ 300 K, 10 Hz – 100 MHz	Output is not isolated from AC supply ground
B2902A + Filter	109.85 μV_{rms} @ 300 K, 10 Hz – 100 MHz	Output is not isolated from AC supply ground
E3634A	525.94 μV_{rms} @ 300 K, 10 Hz – 100 MHz	Output is isolated from AC supply ground
E36312A	159.76 μV_{rms} @ 300 K, 10 Hz – 100 MHz	Output is isolated from AC supply ground
N6705C	401.86 μV_{rms} @ 300 K, 10 Hz – 100 MHz	Output is isolated from AC supply ground
[102] - TLV271	7.03 μV_{rms} @ 4 K, 100 Hz – 100 kHz	Based on commercial discrete components
[102] - AD8605	2.64 μV_{rms} @ 4 K, 100 Hz – 100 kHz	Based on commercial discrete components

Chapter 5

Cryogenic Heterogeneous Integration of Multiple ICs

In order to achieve an accurate, repeatable, and extrinsic noise-free performance test of a cryogenic electronic system, it is essential to ensure its power and signal integrity. For that purpose, the use of EMC techniques for the improvement of the signal and power integrity of a multiple ICs system cooled by a GM cryocooler is reported in this chapter. Consequently, a cryogenic heterogeneous integration between the electronics and the GM cryocooler is proposed to improve the system signal integrity.

The electronic system at test is composed of several elements, and it is shown in Figure 5.1. In particular, the main ICs are a charge redistribution based Digital to Analog Converter (DAC) and a PMU. Both ICs are developed by the ZEA-2 IC design group at Forschungszentrum Jülich [99, 146]. In addition, two commercial ICs containing matched resistors (LT5400-4) and several RLC low-pass filters, are included into the system. A schematic view of the multiple ICs system is shown in Figure 5.2. Here, the PMU provides a DC bias voltage to the resistor network, which generates the reference voltages required by the charge redistribution DAC for its operation.

By developing a cryogenic heterogeneous integration between the electronics and the GM cryocooler, two technical objectives are meant to be accomplished. These are:

- To demonstrate the combined operation, at CTs, of the charge redistribution DAC and the PMU.
- To evaluate the efficiency of the EMC techniques applied for the improvement of the signal and power integrity of the electronic system cooled by the GM cryocooler.

The first section of this chapter provides a brief description of the charge redistribution DAC employed in this work. The second section discusses the signal integrity issues faced by the cryogenic electronic system evaluated in this work. Subsequently, the EMC techniques used to improve the signal and power integrity of the cryogenic electronics are presented in the third section. Thereafter, an evaluation of the efficiency of these techniques is provided in the fourth section. The last section of this chapter addresses

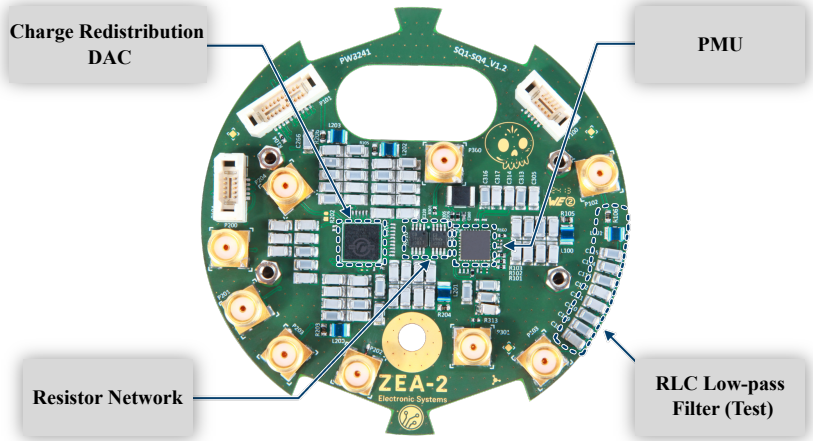


Figure 5.1: Multiple ICs PCB for cryogenic heterogeneous integration.

the testing of the multiple ICs system which is heterogeneously integrated with the GM cryocooler.

5.1 Charge Redistribution DAC

In the multiple ICs system the PMU excites, with approximately 1 V, a network consisting of eight resistors arranged in serial connection. Each resistor has a magnitude of 1 kΩ, and two commercial ICs are employed to set the resistor network (LT5400-4). Consequently, eight voltages are generated. The magnitudes of these voltages are equally spaced due to the use of matched resistors, which is the main attribute offered by the LT5400-4 ICs. Moreover, the voltages generated by the resistor network are used as reference quantities by the charge redistribution DAC.

The DAC used in this work is developed in 65 nm bulk-CMOS technology [99, 147]. It employs a charge redistribution topology, also known as split array, to exploit the simplicity of the charge scaling DAC topology, without needing big capacitors for the implementation of high resolution converters. This advantage is possible due to addition of the attenuation capacitor (C_{Att}) [59].

$$V_{\mathrm{o_{DAC}}} = \sum_{\mathrm{k}=0}^{\mathrm{N}-1} D_{\mathrm{k}}\, 2^{\mathrm{k}-\mathrm{N}} \cdot \left(V_{\mathrm{Ref,U}} - V_{\mathrm{Ref,L}}\right) \tag{5.1}$$

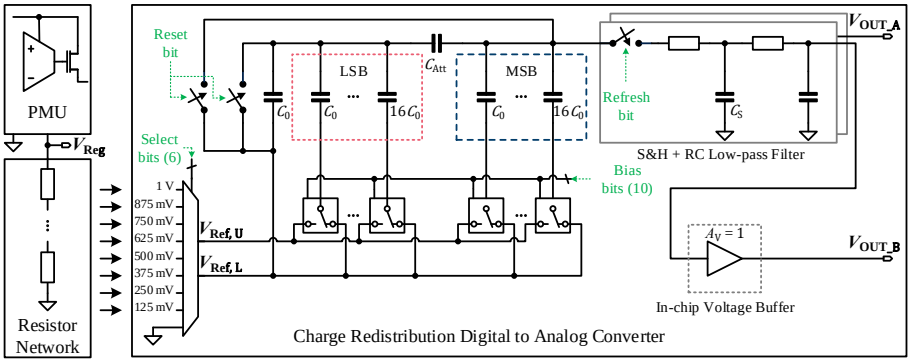


Figure 5.2: Simplified schematic representation of the multiple ICs system. Vliex et al. provide a detailed description of the charge redistribution DAC in [99].

Table 5.1: Value combinations of $V_{Ref,U}$ and $V_{Ref,L}$, in DAC operation without interpolation algorithm.

Option	1	2	3	4	5	6	7	8
$V_{Ref,U}$	125 mV	250 mV	375 mV	500 mV	625 mV	750 mV	875 mV	1 V
$V_{Ref,L}$	0 V	125 mV	250 mV	375 mV	500 mV	625 mV	750 mV	875 mV

For the DAC in Figure 5.2, its output voltage ($V_{o_{DAC}}$) is defined by Eq. (5.1); considering $C_{Att} = (\sum \mathrm{LSB}_{Caps} / \sum \mathrm{MSB}_{Caps}) \cdot C_0$, where $\sum \mathrm{MSB}_{Caps} = \sum \mathrm{LSB}_{Caps} - 1$ [59]. N is the total number of bits, and k represents the n-th bit D_k. While $V_{Ref,U}$ and $V_{Ref,L}$ are the reference voltages. Thus, according to the schematic in Figure 5.2, k can take any value between 0 and 9. And accordingly with the digital input word, D_k can be 0 or 1. Also, N = 10.

The number of bits controlling the charge redistribution DAC is increased by three bits via the analog multiplexer defining the values of $V_{Ref,U}$ and $V_{Ref,L}$. Six bits control the analog multiplexer output voltages. In this way $V_{Ref,U}$ can take any value between 125 mV and 1 V. Conversely, $V_{Ref,L}$ can take any value between 0 V and 875 mV. However, during DAC operation without an interpolation algorithm, the combination of values that $V_{Ref,U}$ and $V_{Ref,L}$ can take is restricted to eight options, as indicated in Table 5.1. Consequently, the output voltage of the DAC used in this work is defined by digital words composed by 13 bits.

The main advantage of the charge redistribution DAC is that it does not produce a significant static power dissipation. Also, at CTs the properties of the Metal - Insulator - Metal capacitors used by the DAC, do not have substantial variations in regards to RT. Though, once $V_{Ref,U}$ and $V_{Ref,L}$ are set to a voltage level, due to the capacitors mismatch the DAC resolution is limited to 10 bits if no calibration algorithm is employed [99].

Table 5.2: Power consumption of charge redistribution DAC, at CT and $f_R = 3.9\,\text{kHz}$.

Block	Power consumption
DAC total	21.1 µW (2.63 µW per channel)
Clock buffer	4.3 µW
Total	25.4 µW (3.18 µW per channel)

The output voltage produced by the DAC is distributed to multiple output channels via a demultiplexing process. And, each channel stores the output of the DAC in a sample and hold structure, where the output voltage is held by an storage capacitor (C_S). The voltage in C_S increases at discrete steps each time the DAC drives the specific output channel. Moreover, a periodical refresh of each output channel is needed due to leakage currents and distortions impacting C_S, and the ideal refresh rate (f_R) of each output channel is 3.9 kHz. Additionally, the output of one of the channels is driven by a voltage buffer in order to perform electrical measurements demanding high output currents; e.g. voltage noise measurements. Besides, at CTs the voltage buffer driving V_{OUT_B} in Figure 5.2, requires a supply voltage of 1.7 V and has a power consumption of 270 µW [99].

In addition to the reference voltages, the charge redistribution DAC requires 1.2 V and 2.5 V supply voltages to power its core and I/O digital circuitry, which consists of memory and logic blocks. Finally, Table 5.2 lists the power consumption values of the charge redistribution DAC, at CTs and $f_R = 3.9\,\text{kHz}$.

5.2 Signal Integrity Issues Faced by the Cryogenic Electronics in this Work

As it is described in section 2.3, the operation of electronic systems at CTs not only involves performance changes of the electrical components, but also the technical challenges associated with the use of cryocooling systems for the electronics cooling. In the case of the GM cryocooling system used in this work, and described in section 2.2, two main aspects hindering the signal integrity of the cryogenic electronics are identified.

The first aspect is the default use of a breakout box for the establishment of electrical connections between the measurement equipment at RT and the cryogenic electronics; Figure 5.3 shows the default setup employed for most of the electrical connections.

The breakout box has 30 Bayonet Neill–Concelman (BNC) connection ports, and each one provides the signal and returns paths. However, after the BNC interface, each port is wired as a twisted pair cable. And, the twisted pairs are gathered in groups of 6 and arranged into a 5 m long cable assembly with Fischer connectors; i.e. 5 cable assemblies come out of the break box. These cable assemblies are connected at the bottom of the

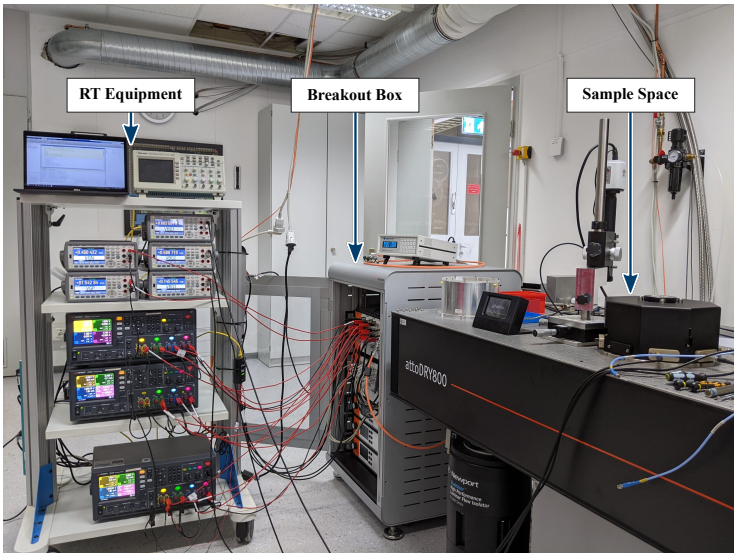


Figure 5.3: Default setup for most of the electrical connections in the attodry800 system.

attodry800 system and after a mechanical interface, the signal and return paths are thermalized with the first and second stages of the cryocooling system before reaching the cryogenic sample space. The cables thermalization is required to avoid condensation on the RT connectors and to prevent that the RT heat reaches the coldest stage of the cryocooling system [37].

Although the breakout box offers to the user an organized interface for electrical connections, the signal integrity of these connections may not only be compromised due to the cables length, but also due to the fact that those cables are physically close to the motor and compressor located at the bottom of the attodry800 cold head. Therefore, the default electrical connections may also be exposed to electromagnetic interference (EMI) [53]. A signal integrity improvement can be obtained by employing shorter connection interfaces going through the cold head shrouds, similarly to the RF connections in Figure 2.6. In this way, the connections length and exposure to EMI, can be reduced.

The second aspect hindering the cryogenic electronics signal integrity is the ground loop noise, an extrinsic noise source as described in section 2.3. In the case of the attodry800, due to its physical construction, the electronics cooled by such a system is exposed to ground loop noise interference.

In order to quantify the impact of the ground loop noise, the voltage noise produced by the linear voltage regulator is measured via an RF connection port, when such a circuit

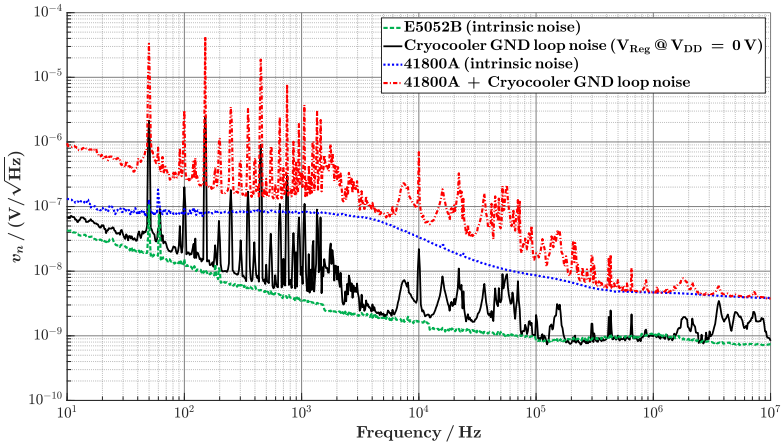


Figure 5.4: Evaluation of ground loop noise impact on the electronics in the attodry800.

Table 5.3: Measured RMS voltage noise values during the ground loop noise evaluation.

BW	10 Hz – 10 kHz	10 Hz – 10 MHz
E5052B (intrinsic noise)	0.35 μV_{rms}	2.57 μV_{rms}
Cryocooler GND loop noise	6.63 μV_{rms}	8.40 μV_{rms}
41800A (intrinsic noise)	6.02 μV_{rms}	15.15 μV_{rms}
41800A + Cryocooler GND loop noise	107.43 μV_{rms}	111.83 μV_{rms}

is not energized (i.e. V_{DD} = 0 V) and is cooled to 6 K by the attodry800. It is relevant to mention that the measurement setup shown in Figure 4.1 is used without the thermally conductive - electrically isolating layer (Gap Pad 5000S3). Thus, in this measurement, the circuit ground is electrically linked to the cryocooler cold head. Figure 5.4 shows the voltage noise amplitude spectral density measured at the output of the voltage regulator, together with the intrinsic voltage noise of the E5052B SSA.

As can be observed, several spurious frequencies contribute to regulator voltage noise spectrum when such a circuit is not powered. Although not reported in Figure 5.4, such an interference occurs not only at CTs, but also at RT. After several trials, it is found that the spurious frequencies only appear on the noise spectrum when the voltage regulator circuit ground is electrically linked with the cryocooler cold head. Hence, these outcomes demonstrate that a ground loop capable of producing electrical interference is present in the experimental setup.

The amount of interference produced by the ground loop noise over a circuit varies according to the circuit characteristics; i.e. each circuit is affected differently. As an

example, Figure 5.4 also shows the intrinsic voltage noise spectrum of the 41800A active probe (a voltage buffer with low input capacitance and high input resistance) [148], and the spectrum measured by such a probe when used as intermediate stage between the voltage regulator circuit and the E5052B SSA.

It can be observed that, in the later case, instead of buffering the noise signal at the output of the voltage regulator circuit the 41800A active probe amplifies the noise; i.e. in the 10 Hz - 10 kHz BW the RMS voltage noise is 17 times higher. The RMS voltage noise values are quantified for each spectra shown in Figure 5.4 by means of Eq. (4.10), and reported in Table 5.3. As it is uncertain how much a ground loop can affect the performance of an electronic circuit, the best approach is to implement EMC techniques that suppress the impact of that extrinsic noise source.

5.3 EMC Techniques for Signal and Power Integrity Improvement

In this work, three methods are investigated to enhance the signal and power integrity of electronics cooled by the attodry800 system. These are:

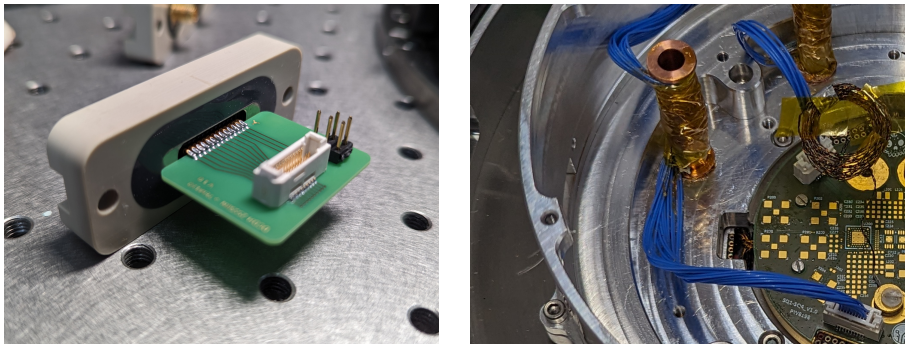
- The implementation of shorter connection interfaces through the cold head shrouds.
- The breaking of the ground loops for its interference suppression.
- RLC low-pass filters for high frequency noise reduction in voltage supply rails.

In the following, these methods are detailed.

5.3.1 Shorter Connections and Thermalization via Copper Bobbins

As to reduce the length and EMI exposure of the electrical connections, a feedthrough with D-Sub-Mikro-D (DCDH-25S4C40.5BN) socket assembly is designed as shown in Figure 5.5 (a). It must be mentioned that the selected socket is rated for high vacuum conditions similar to those inside the attodry800 system during the cryogenic cooling process; e.g. 4×10^{-6} m bar. Also, the socket assembly is inserted into a PEEK frame and glued to it with epoxy adhesive (2216 B/A GRAY).

In order to establish the electrical connections, discrete wire cable assemblies (SESDT-10-32-G-20.0-L1) are used. The assembly consist of 20 tinned copper wires which are isolated and sheathed with FEP. Moreover, the length of the cables is 0.5 m; shorter assemblies are also offered by the manufacturer. As shown in Figure 5.5 (b), the cables are thermalized to the first stage (i.e. 60 K) of the cold head via copper bobbins. The



(a) (b)

Figure 5.5: (a) Feedthrough with D-Sub-Mikro-D socket assembly designed for shorter electrical connections between RT and the cryogenic sample space. The socket is rated for high vacuum environments, and glued to the PEEK frame with epoxy adhesive. (b) Thermalization of the cables via copper bobbins; cables are fastened to the bobbins by mixing GE 7031 varnish and silver paint.

fastening of the cables to the bobbin is achieved via a mix consisting of GE 7031 varnish and silver paint; this mix serves as adhesive and thermal conductor [149].

5.3.2 Ground Loop Break

In order to break the ground loops impacting the electronics cooled by the attodry800 system, three technical approaches are proposed. They are described in the following.

5.3.2.1 USB Isolator

An USB isolator is a device that provides electrical isolation between two elements that are connected through an USB link. These elements are the host (e.g. a computer) and the peripheral device (e.g. a JTAG debugger). The requirements that an USB isolator must satisfy vary according to the application. In medical applications, isolators capable of withstanding a 5 kV surge are required to ensure the patient safety. While in industrial settings, other needs are considered. These could be the susceptibility to electrostatic discharge, lighting strikes, power surges, as well as sensitivity to electrical noise from EMI and ground loops [150].

In this work, two USB isolators are used to break the ground loops between the measurement support computer and the debuggers (JTAG and I^2C) configuring the prototype ICs.

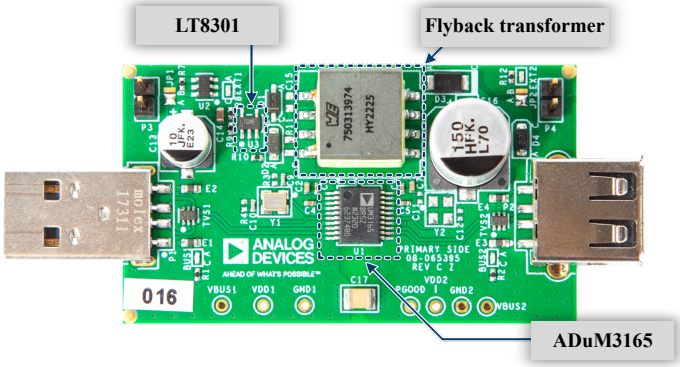


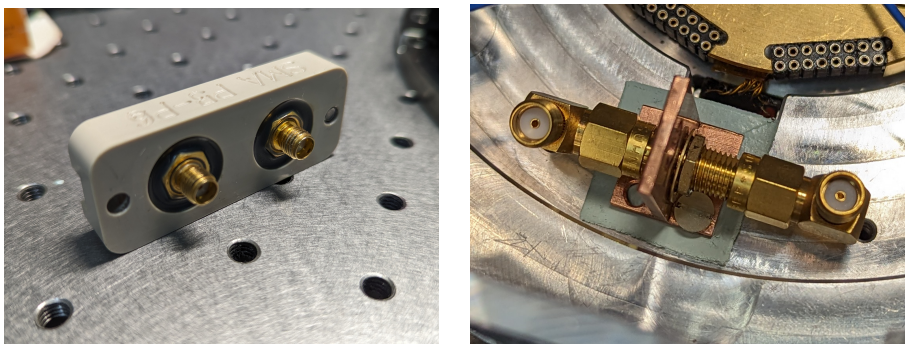
Figure 5.6: CN0550 circuit evaluation board, including an ADuM3165 galvanic digital isolator and an LT8301 galvanically isolated flyback converter [150].

Specifically, the CN0505 evaluation board shown in Figure 5.6 is used for the electrical isolation of the USB links. The board main ICs are the ADuM3165 and LT8301.

The ADuM3165 is a digital isolator IC that provides galvanic isolation to the USB data lines between the host and the peripheral device. It supports up to 480 Mbps of data transfer (USB 2.0), while maintaining an isolation voltage rating of 3.75 kV_{rms}. While the LT8301 IC is a galvanically isolated flyback converter that provides the isolated 5 V bus power on the peripheral side. Depending on the input voltage, this device is capable of delivering up to 6 W of isolated output power, allowing it to support both low-power and high-power USB 2.0 devices. In the CN0550 evaluation board, the LT8301 uses a flyback transformer with a turns ratio of 3:1 and a primary inductance of 40 µH to produce the isolated power. Finally, the CN0550 evaluation board is a an effective and easy to use plug-and-play system. However, only if the USB peripheral has high power consumption, an external PSU must be used to feed the isolated flyback converter for additional power output [150].

5.3.2.2 RF Cables Thermalization with Electrical Isolation

Concerning the RF cabling setup used in the attodry800 system, it is modified to prevent that the RF cables thermalization anchoring forms a ground loop between the electronics and the cryocooler cold head. Figure 5.7 (a) shows the feedthrough designed for SMA cable assemblies. In this case a pair of SMA adapters (32K101-KH0L5), which are elements rated for high vacuum environments, are used to interface the RT systems with the electronics inside the cryogenic sample space. The adapters are inserted in, and glued to a PEEK frame, by means of an epoxy adhesive (2216 B/A GRAY).



(a) (b)

Figure 5.7: (a) Feedthrough with two SMA adapters for RF connections between RT and the cryogenic sample space. The adapters are rated for high vacuum environments, and glued to the PEEK frame with epoxy adhesive. (b) Thermalization copper clamp for RF cables; cables are fastened with SMA adapters. The clamp is anchored to the cold head first stage via plastic screws and a thermal pad (Gap Pad 5000S35) as to avoid ground loops.

As to thermalize the RF cable assemblies (MINIBEND KR-6), thermalization copper clamps are employed as shown in Figure 5.7 (b). The cables are fastened to the clamps with SMA adapters. While each clamp is anchored to the cold head first stage via plastic screws. However, between the clamp and the cold head, a thermal pad (Gap Pad 5000S35) piece is placed to prevent electrical conduction and formation of ground loops.

5.3.2.3 PCB Coating with Cigarette Paper - GE 7031 Varnish

In order to electrically isolate the multiple ICs PCB from the cold head of the attodry800 system, and break the ground loop between them, the use of an electrically isolating - thermally conductive layer is proposed in this work. As such a board uses the same PCB stack depicted in Figure 4.1 (c). In Chapter 4, electrical isolation is achieved by means of the Gap Pad 5000S35. Though effective, the use of such a thermal pad is not an smooth process due to its steadiness, which resembles to the one of modeling clay.

Because of this reason, a layer consisting of a cigarette paper substrate soaked with GE 7031 varnish, is employed to coat the bottom side of the multiple ICs PCB. Figure 5.8 shows the bottom side of the board with the coating layer already applied. This approach is inspired by the thermalization techniques described by J. Ekin [37]. Contrary to the Gap Pad 5000S35, the cigarette paper - GE 7031 varnish layer is a solid coating that

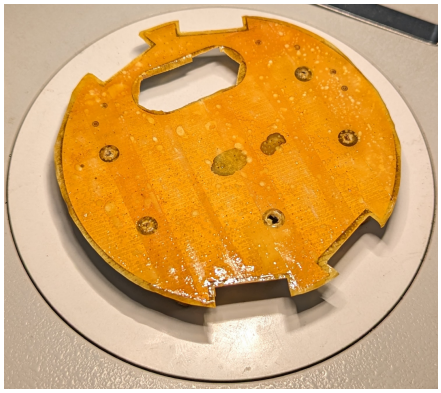


Figure 5.8: Bottom view of the multiple ICs development board. The board bottom side is covered by an electrically isolating - thermally conductive coating layer, consisting of a cigarette paper substrate soaked with GE 7031 varnish.

strongly attaches to the PCB, once it is curated. Regarding the electrical and thermal performance, there was not a noticeable difference between both isolating approaches.

5.3.3 RLC Low-pass Filter

To reduce the impact of the high frequency electrical noise on the voltage supply rails of the prototype ICs potentially induced by the PSUs or the cryogenic test setup, a passive RLC low-pass filter is employed. Figure 5.9 shows a simplified filter schematic. The filter transfer function is defined by Eq. (5.2) and it corresponds to a second-order system.

$$H(j\omega) = \frac{\dfrac{1}{LC}}{(j\omega)^2 + j\omega\dfrac{R}{L} + \dfrac{1}{LC}} \tag{5.2}$$

For an RLC low-pass filter, it is common to define its resonance frequency (ω_0) as in Eq. (5.3). ω_0 indicates the frequency at which the capacitor and the inductor reactances cancel. Another characteristic quantity of this filter is its quality factor (Q). Q establishes the ratio between the capacitive (inductive) reactance and the circuit resistance, as indicated by Eq. (5.4). Also, Q is considered a measure of the filter resonance sharpness; the higher Q, the higher the resonance sharpness and filter selectivity, and vice versa.

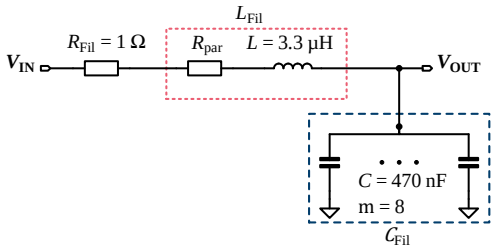


Figure 5.9: Simplified schematic circuit of the passive RLC low-pass filter.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5.3}$$

$$Q = \frac{1}{\omega_0 RC} = \frac{\omega_0 L}{R} \tag{5.4}$$

Consequently, the RLC low-pass filter transfer function can be rewritten in terms of ω_0 and Q, as in Eq. (5.5); considering that $\omega_0^2 = 1/LC$ and $\omega_0/Q = R/L$. Therefore, with Eq. (5.5) it is possible to define equations for the magnitude and phase responses of the filter, as in Eqs. (5.6) and (5.7). These equations become relevant when $\omega = \omega_0$, since they indicate that $|H(j\omega_0)| = Q$ and $Phase(\omega_0) = -90°$, under this condition.

$$H(j\omega) = \frac{\omega_0^2}{(j\omega)^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2} = \frac{1}{1 - \frac{\omega^2}{\omega_0^2} + j\frac{\omega}{\omega_0 Q}} \tag{5.5}$$

$$|H(j\omega)| = \frac{1}{\sqrt{\left(1 - \frac{\omega^2}{\omega_0^2}\right)^2 + \frac{\omega^2}{Q^2\omega_0^2}}} \tag{5.6}$$

$$Phase = -\arctan\left(\frac{\frac{\omega}{\omega_0}}{1 - \frac{\omega^2}{\omega_0}}\right) \tag{5.7}$$

As for the RLC low-pass filter implementation, the selected components are known to have an electrical behavior that is stable and functional at CTs. The resistor (R_{Fil}) con-

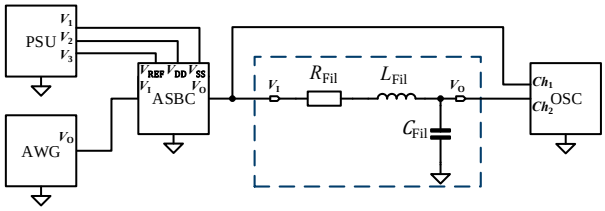


Figure 5.10: Measurement setup used for the characterization of the RLC low-pass filter.

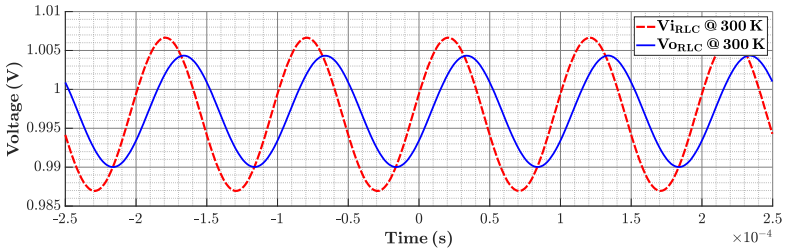


Figure 5.11: Measured time-domain response of the RLC low-pass filter to an AC stimulus signal with $f = 10\,\text{kHz}$, at 300 K.

struction is based on thin-metal film material; the R_{Fil} MPN is CPF0603B1R05E1. Due to the limited availability of component sizes, the capacitor (C_{Fil}) is implemented as a parallel combination of 8 elements, the construction of which is based on the C0G material; the MPN of each of the elements composing C_{Fil} is GRM31C5C1E474GE01. Regarding the inductor (L_{Fil}), a non-magnetic core type is selected for the filter implementation, due to the functional issues that transformers and inductors constructed with magnetic cores have shown at CTs close to 77 K [151]. It is worth mentioning that L_{Fil} uses a copper wire in its construction. Therefore, a resistive parasitic element (R_{par}) must be considered as part of the RLC filter. R_{par} becomes relevant at CTs since the copper electrical resistivity reduces with temperature decline. Moreover, the copper electrical resistivity has a non-linear relation with temperature [37]. This means that the electrical characteristics of the L_{Fil} will differ if obtained at RT or CTs. L_{Fil} MPN is LQW2UAS3R3J00.

The filter is electrically tested with a small AC signal with $V_{p-p} \approx 20\,\text{mV}$ and $V_{DC} \approx 1\,\text{V}$. Then, by measuring the circuit voltage signals (V_{IN} and V_{OUT}) at different frequencies, the input–output amplitude ratio (Gain) and delay (Phase) data are obtained for the construction of the filter Bode plot. As to develop the measurements, an oscilloscope (OSC, DSOX4154A) and an AWG (33600A), were used in combination with the active signal biasing circuit (ASBC) described in the Appendix B. This circuit is employed as a support system in this test since the reactances of C_{Fil} and L_{Fil} change along frequency,

and the AWG cannot handle those changes due to its limited current drive capability. The measurement setup used for the RLC low-pass filter characterization is shown in Figure 5.10. Additionally, Figure 5.11 shows the time-domain response measured from the RLC low-pass filter, when an AC signal with $f = 10\,\text{kHz}$ is used as stimulus at RT.

The described measurement procedure is performed between 1 Hz and 100 kHz, at 8 K and 300 K. The collected data is displayed in the Bode plot shown in Figure 5.12. As can be observed, there are a significant differences between the filter responses measured at both temperatures. First, the frequency at which the filter gain reaches a magnitude of −3 dB increases with temperature reduction. Second, at 300 K the filter has a maximally-flat response. On the other hand, at 8 K the filter exhibits a small amplification peaking. Third, the phase transition towards −180° is faster at 8 K than at 300 K. According to Eqs. (5.3) – (5.7), these changes signal to an increase of Q and a reduction of ω_0. Consequently, this situation can be understood as a resistivity reduction of R_{par} and an inductance increase of L_{Fil} at 8 K; assuming R_{Fil} and C_{Fil} do not change.

In order to verify this hypothesis, the frequency response of the RLC low-pass filter was obtained via circuit simulation with the use of the lumped-element models provided by the components manufacturer. Although these models are rated for RT applications, they can be modified to adjust the values designated to R_{par} and L_{Fil}, allowing the emulation of the inductor electrical behavior at CTs.

The filter frequency responses obtained via simulation, for 8 K and 300 K, are also included in Figure 5.12. At 300 K the measurement data match the simulation, validating in this way the measurement procedure. Regarding the circuit response at 8 K, the measurement and simulation data have similar features along frequency without significant differences. And, since the 8 K simulation data is obtained by reducing R_{par} resistance and increasing L_{Fil} inductance, it can be confirmed that the electrical characteristics of L_{Fil} improve at 8 K. Table 5.4 summarizes the RLC low-pass filter characteristics.

Although the RLC low-pass filter is completely functional at CTs, some aspects must be considered for its application into cryogenic electronic systems.

- Due to the cryogenic increase of L_{Fil}, Q and $f_{-3\,\text{dB}}$ of the RLC low-pass filter will increase, if R_{Fil} and C_{Fil} are held constant. Then, the simplest approach for the reduction of Q and $f_{-3\,\text{dB}}$ is to increase C_{Fil}, since increasing R_{Fil} will produce a higher voltage drop between the input and output ports of the filter. However, area constraints in cryogenic cooling systems may hinder the practicality of this approach.
- The increase of L_{Fil} at CTs will lead to an increment of the filter resonance peaking; e.g. Q increases at CTs. Thus, care must be taken to control or exploit this phenomenon.
- Due to R_{Fil} and R_{par}, the voltage drop between the filter input and output ports cannot be neglected; e.g. if $I_{\text{Load}} \approx 10\,\text{mA}$, at 8 K the voltage drop will be close to 13 mV.

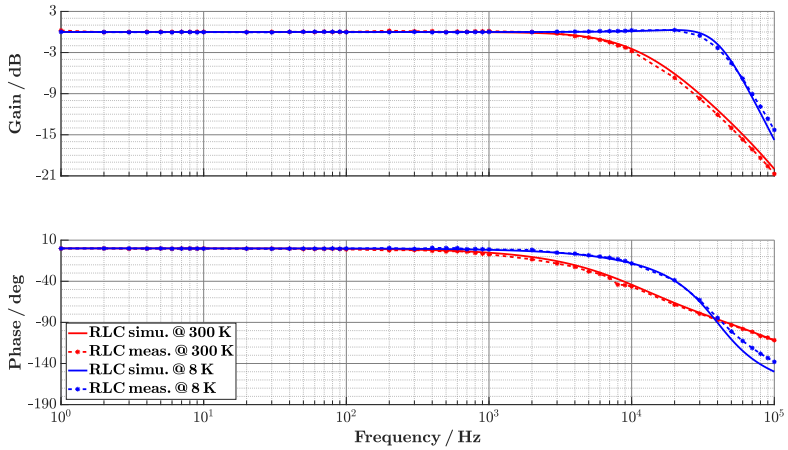


Figure 5.12: Frequency-domain responses of the RLC low-pass filter obtained via measurement and simulation, at 8 K and 300 K.

Table 5.4: RLC low-pass filter electrical characteristics.

Temp.	L_{Fil}	R_{par}	Q	ω_0	f_0	$f_{-3\,\text{dB}}$
300 K	3.3 µH	3 Ω	0.234	0.284 M rad/s	45.18 kHz	10 kHz
8 K	4.25 µH	0.3 Ω	0.818	0.250 M rad/s	39.81 kHz	45 kHz

- The approach used in this work to model the cryogenic behavior of L_{Fil} is just an initial approximation. Better results could be obtained by developing a simulation model based on the cryogenic characterization of the passive elements scattering parameters.
- In this work an RLC low-pass filter is preferred over the RC or RC-RC filter variants, due to the higher selectivity and lower area requirements of the RLC filter.

5.4 Evaluation of Noise Suppression EMC Techniques

In order to evaluate the efficiency of the EMC techniques described in section 5.3, these techniques are used for the preparation of the experimental setup shown in Figure 5.13. Thereafter, several technical assessments are performed.

In the experimental setup the multiple ICs development board is installed on the sample holder, which is the coldest point in the attodry800 sample space. Besides, a detailed view of the development board inside the attodry800 system, is shown in Figure 5.14.

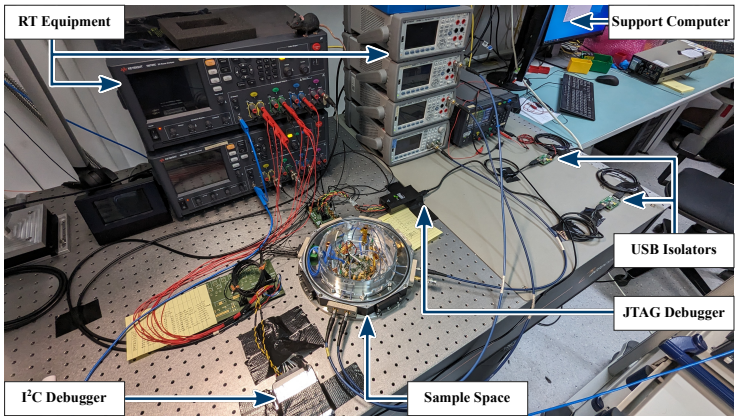


Figure 5.13: Experimental setup for testing of multiple ICs development board. The EMC techniques described in section 5.3 are used for the board deployment.

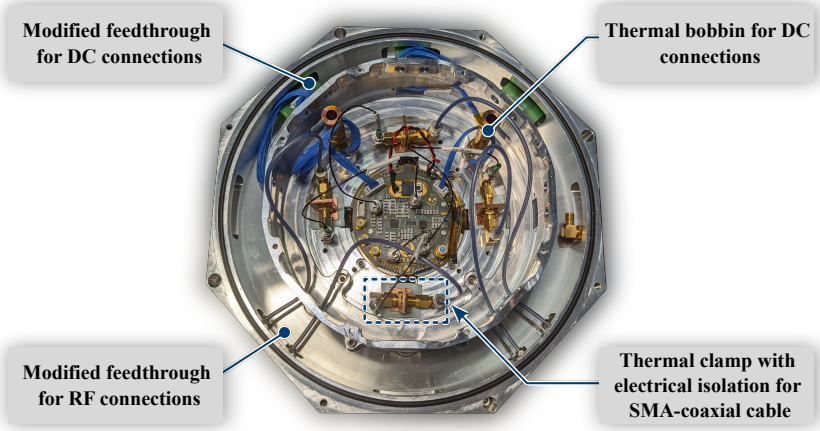


Figure 5.14: Multiple ICs development board installed in cryogenic sample space of the attoDRY800 system. The EMC techniques described in section 5.3 are used for the board deployment.

Moreover, Figure 5.15 provides a schematic representation of the testing setup used for the evaluation of the multiple ICs system. Here, the debuggers (JTAG and I^2C) controlling the prototype ICs are electrically decoupled from the support computer via USB isolators (CN0550). Also, instruments as PSUs (N6705C), DMMs (34470A), and an AWG (33600A), are also included in the setup and controlled via IP addressing by the sup-

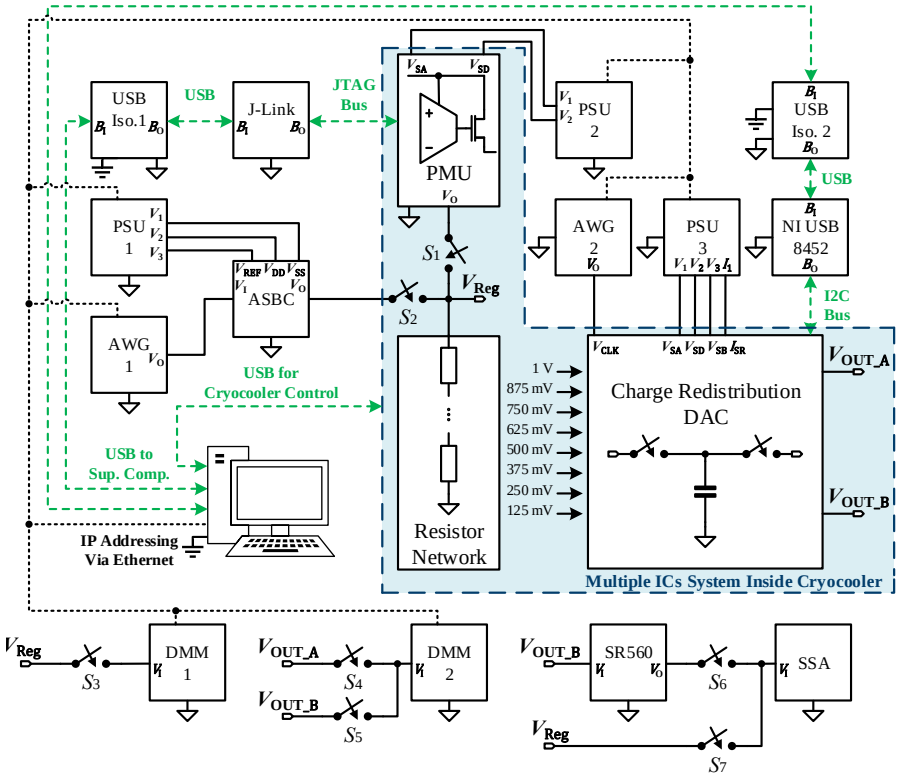


Figure 5.15: Simplified schematic representation of the setup used in this work for testing the multiple ICs system.

port computer. In contrast, the LNA (SR560) and the SSA (E5052B) are controlled by the testing operator. As to represent the different testing scenarios addressed in section 5.5, Figure 5.15 employs switches ($S_1 - S_7$) to indicate the connections requiring manual attachment.

An initial evaluation of the setup ground isolation is performed by testing the electrical conductivity between the development board ground and the attodry800 chassis, with a DMM. Due to the EMC techniques, both of the setup points are electrically isolated.

A subsequent test consisted on the measurement of the voltage noise amplitude spectral density generated by a passive circuit, via a SSA (E5052B); Figure 5.16 provides an schematic representation of the measurement setup. In this case the DUT is a passive circuit, which is composed by an RLC low-pass filter (described in subsection 5.3.3) and a 50 Ω resistor. And, such a DUT is embedded in the multiple ICs development board.

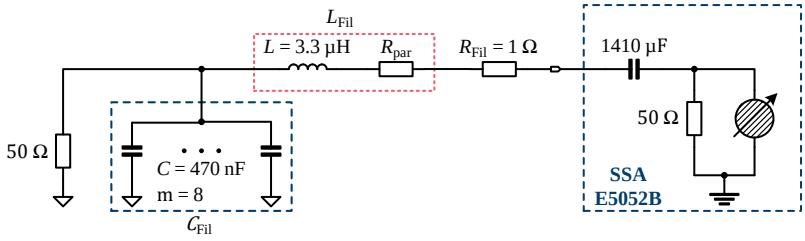


Figure 5.16: Setup used in evaluation of noise suppression EMC techniques for the electronics inside attodry800 system. The SSA (E5052B) is used to measure the voltage noise amplitude spectral density of the RLC||50 Ω circuit (DUT).

In order to compere the impact of the EMC techniques, the DUT voltage noise spectrum is measured under three conditions:

- Development board in total isolation, i.e. the board is physically detached from the experimental setup; RLC || 50 Ω (intrinsic noise).
- Development board installed inside the attodry800, with EMC techniques; RLC || 50 Ω (isolated, in sample space).
- Development board installed inside the attodry800, with EMC techniques, but with a ground loop added on purpose; RLC || 50 Ω (non isolated JTAG, in sample space).

The measured voltage noise spectra, at RT, are shown in Figure 5.17. In addition, the intrinsic noise generated by the SSA (E5052B) is added as a reference for comparison. Also, for all the spectra the RMS voltage noise values are quantified by means of Eq. (4.10), and reported in Table 5.5.

It can be observed that there is little difference between the measured intrinsic noise spectra of the SSA (E5052B) and the DUT (RLC||50 Ω circuit). And only a small difference, attributed to the connection parasitic elements, appears at the 1 MHz - 10 MHz BW. However, once the DUT (RLC||50 Ω circuit) is installed in the experimental setup, the presence of noise spurs is evident at the 10 kHz - 10 MHz BW.

After several trials, it is defined that these spurs are related to the instruments held at RT used in the experimental setup; i.e. the PSUs, DMMs, and AWG. Even though the suppression of these spurs was not possible in this work, the use of ferrite beads may mitigate them.

The efficiency of the EMC techniques used in this work, for noise suppression, is noticed when a ground loop is added to the experimental setup on purpose; i.e RLC || 50 Ω (non isolated JTAG, in sample space) plot in Figure 5.17. In this case the USB isolator placed

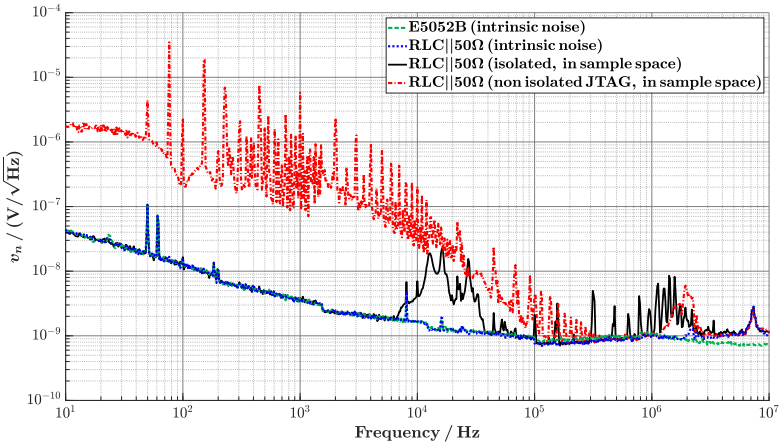


Figure 5.17: Efficiency evaluation of the EMC techniques for suppression of noise sources impacting the electronics inside the attodry800 system.

Table 5.5: Measured RMS voltage noise values in the evaluation of EMC techniques.

BW	10 Hz – 10 kHz	10 Hz – 10 MHz
E5052B (intrinsic noise)	0.36 μV_{rms}	2.23 μV_{rms}
RLC|| 50 Ω (intrinsic noise)	0.36 μV_{rms}	2.81 μV_{rms}
RLC|| 50 Ω (isolated, in sample space)	0.40 μV_{rms}	4.96 μV_{rms}
RLC|| 50 Ω (non isolated JTAG, in sample space)	81.84 μV_{rms}	82.14 μV_{rms}

between the JTAG debugger and the support computer, is removed. In this way a direct ground connection between the development board and the computer is established. As a consequence, the low frequency V_{rms} noise measured at the DUT by the SSA (E5052B) is 205 times higher than the isolated case. Moreover, when the 10 kHz - 10 MHz BW is considered, the low frequency V_{rms} noise is 17 times higher.

As third test, the voltage noise generated by the linear voltage regulator is measured at CTs, with and without the application of the EMC techniques. Such a circuit is used as DUT since its functionality at CTs has been verified and it is embedded in the development board. Figure 5.18 shows the voltage noise spectra measured in this test. And, as can be observed, the EMC techniques are able to suppress the low frequency noise spurs impacting the linear regulator voltage output. Hence, the regulator low frequency (10 Hz - 10 kHz) RMS noise is 2.7 times lower when the EMC techniques are employed in the assembly of the experimental setup.

Based on the evaluation tests results summarized in the Tables 5.5 and 5.6, it can be

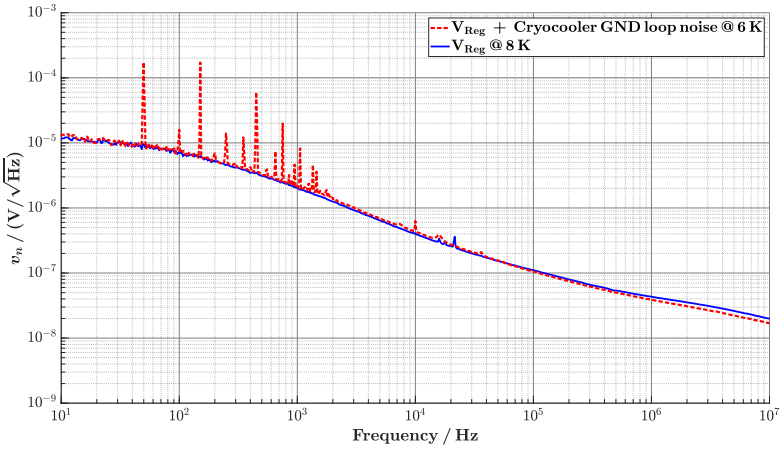


Figure 5.18: EMC techniques impact on the voltage regulator output noise. Measurement at 6 K is performed without using the EMC techniques described in section 5.3, while those techniques are applied for the measurement at 8 K. Test conditions: $V_{IN\ Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V, $I_{Load} = 5$ mA and $V_{Sup} = 2$ V.

Table 5.6: Measured RMS voltage noise values of the linear voltage regulator at CTs, as part of the EMC techniques evaluation.

BW	10 Hz – 10 kHz	10 Hz – 10 MHz
$V_{Reg,n}$ @ 6 K (without EMC techniques)	427.61 μV_{rms}	440.42 μV_{rms}
$V_{Reg,n}$ @ 8 K (with EMC techniques)	157.88 μV_{rms}	194.88 μV_{rms}

concluded that the EMC techniques used to assemble the experimental setup, effectively suppress the influence of the extrinsic noise sources affecting the electronics cooled by the attodry800 cryocooling system.

5.5 Testing of Multiple ICs Heterogeneously Integrated with the GM Cryocooler

As previously stated, the purpose of this work is to achieve a cryogenic heterogeneous integration between the multiple ICs system (shown in Figure 5.1) and the GM cryocooler (attodry800), by applying the noise suppression EMC techniques presented in section 5.3. In this way, an accurate, repeatable, and extrinsic noise-free performance test of a cryogenic electronic system is intended to be achieved.

Therefore, this section describes the testing of the multiple ICs system heterogeneously integrated with the GM cryocooler (attodry800). The technical results are discussed at the end of this section.

5.5.1 System Test

The multiple ICs system (Figure 5.2) is subjected to several electrical evaluation tests performed at 8 K, with the application of the EMC previously addressed. As mentioned in section 5.3, the setup shown in Figure 5.15 is used in this work to perform different tests over the multiple ICs system. The tests and their results are discussed in the following.

5.5.1.1 Test 1: Direct DC Output Voltage Measurement

The main purpose of this test is to verify that the multiple ICs system components can operate at CTs, once integrated with the GM cryocooler via the EMC techniques. The PMU is operated with a supply voltage of 2 V, and it is configured via a JTAG debugger as to provide an output voltage close to 1 V. Then, the PMU output voltage energizes the resistor network. The charge redistribution DAC receives the eight voltages produced by the energized resistor network, and use them as reference quantities for the production of the its output voltage. In this test the DAC uses 1.2 V and 2.5 V to energize its core and I/O digital circuitry. Moreover, $f_R = 3.9$ kHz.

In this particular instance, DC measurements of the DAC output voltage are done via a demultiplexed sample and hold structure. Thus, the measured quantities correspond to the V_{OUT_A} node of Figure 5.2. Due to the low current drive capability of the sample and hold structure storing the DAC output voltage, the DMM (34470A) used to perform the DC voltage measurements is set for an input load of 10 GΩ.

Figure 5.19 shows the DC voltages measured in this test. It must be mentioned that the DAC output voltage is controlled by 13 bits digital words (DWs), via an I^2C debugger and without interpolation algorithm. Due to the constant configuration of the DAC registers needed to change its input DW, and the time required by the DMMs to perform the DC measurements, this test requires two hours to be completed. In fact, even though the output voltage of the PMU is set for a value close to 0.985 mV, it suffers a slight drift along the test. Perhaps, due to thermal variations even along time; this topic requires further investigation and it is not addressed in this work. Regarding the DAC, it generates its output voltages according to the voltage references generated by the resistor network. From the measurement results, the DAC less significant bit equivalent voltage (V_{LSB}) and differential nonlinearity (DNL) are defined according to Eqs. (5.8) and (5.9), respectively [152].

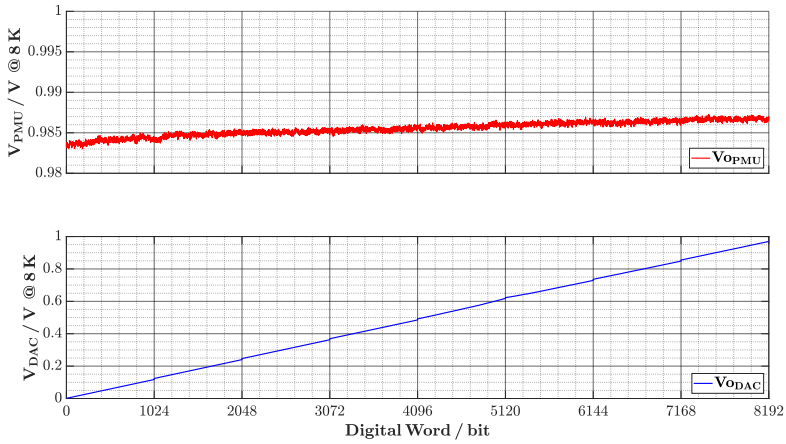


Figure 5.19: Cryogenic test (8 K) of the multiple ICs system (Test 1). The DC output voltages of the PMU and DAC are measured regarding the input digital word.

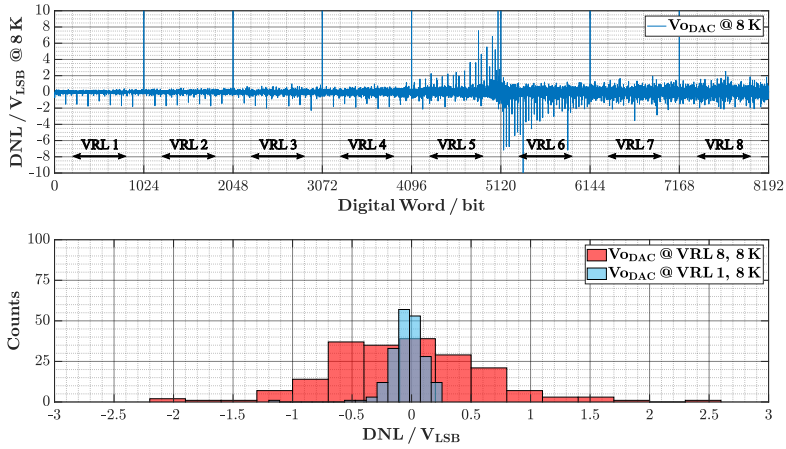


Figure 5.20: DNL of the DC voltages generated by the DAC; results from Figure 5.19 are used (Test 1). The DNL statistical variation, with respect to the voltage reference level (VRL) used by the DAC, is presented as histograms; 200 samples, taken at the center of each VRL, are used to build each histogram.

$$V_{LSB} = \frac{V_{o_{DAC}}(0) - V_{o_{DAC}}(2^N - 1)}{2^N} \tag{5.8}$$

Table 5.7: DNL statistics of the DAC at 8 K, with respect to the VRL (Test 1).

VRL	$V_{o_{DAC}}$ range	σ	mean	max.	min.
1	0 V - 125 mV	0.1494 V_{LSB}	−0.0362 V_{LSB}	0.2423 V_{LSB}	−1.1360 V_{LSB}
2	125 mV - 250 mV	0.1980 V_{LSB}	−0.0345 V_{LSB}	0.4779 V_{LSB}	−1.2792 V_{LSB}
3	250 mV - 375 mV	0.2324 V_{LSB}	−0.0341 V_{LSB}	0.6366 V_{LSB}	−0.8820 V_{LSB}
4	375 mV - 500 mV	0.3269 V_{LSB}	−0.0397 V_{LSB}	0.9785 V_{LSB}	−1.4467 V_{LSB}
5	500 mV - 625 mV	0.4981 V_{LSB}	0.0271 V_{LSB}	2.5857 V_{LSB}	−1.1612 V_{LSB}
6	625 mV - 750 mV	0.6831 V_{LSB}	−0.0861 V_{LSB}	1.2112 V_{LSB}	−3.62 V_{LSB}
7	750 mV - 875 mV	0.5948 V_{LSB}	−0.0819 V_{LSB}	1.3394 V_{LSB}	−3.5425 V_{LSB}
8	875 mV - 1 V	0.6558 V_{LSB}	−0.0511 V_{LSB}	2.5122 V_{LSB}	−2.1348 V_{LSB}

$$\mathrm{DNL}\,(\mathrm{DW}) = \frac{V_{o_{DAC}}(\mathrm{DW}) - V_{o_{DAC}}(\mathrm{DW}-1) - V_{LSB}}{V_{LSB}} \tag{5.9}$$

Figure 5.20 provides a graphical representation of the DNL, with respect to the input DW of the DAC. It can be observed that the DNL variation increases each time the input DW reaches a multiple of 1024 bits. This situation corresponds to a change of the reference voltages assigned to $V_{Ref,U}$ and $V_{Ref,L}$. In this work, each reference voltage pair is referred as voltage reference level (VRL).

Besides, the DNL variation of the DAC output could be related to the low frequency noise generated by the PMU. A comparison of the DNL variation between the lowest and highest VRLs (1 and 8, respectively) is provided by the histograms shown in Figure 5.20. Additional statistical information, regarding the DAC DNL variation with respect to the VRL at use, is provided in the Table 5.7.

5.5.1.2 Test 2: DAC Output Voltage Measurement via Analog Buffer

This test seeks to fulfil two objectives. The first one is to verify that the DAC output can be characterized via the on-chip analog voltage buffer. The second objective is to measure the voltage noise spectrum of the buffered DAC output, as to verify the efficiency of the EMC techniques used for the cryogenic heterogeneous integration of the electronic and cryocooling systems.

In this test the operation of the multiple ICs system is similar to the one performed in Test 1, but with some differences. In particular, the on-chip analog voltage buffer is energized with 1.7 V and the measurements are done on the V_{OUT_B} node of Figure 5.2. Figure 5.21 shows the DC voltages measured in this test.

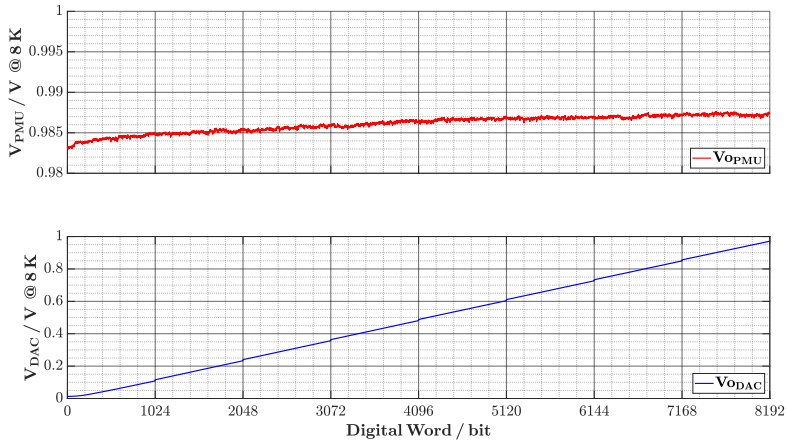


Figure 5.21: Cryogenic test of the multiple ICs system (Test 2). The DC output voltages of the PMU and DAC are measured regarding the input digital word. The DAC output is measured via the on-chip voltage buffer, at 8 K.

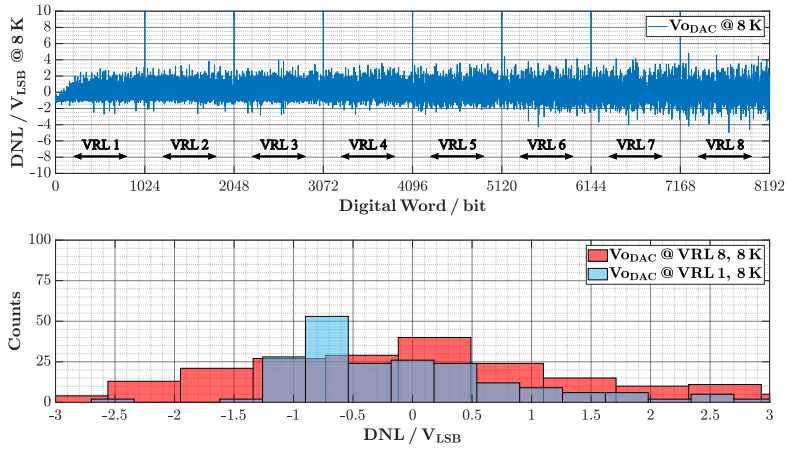


Figure 5.22: DNL of the DC voltages generated by the DAC; results from Figure 5.21 are used (Test 2). The DNL statistical variation, with respect to the voltage reference level (VRL) used by the DAC, is presented as histograms; 200 samples, taken at the center of each VRL, are used to build each histogram.

Hence, the measurement seems to be similar to the one obtained in Test 1. However, it can be noticed that the analog buffer is not able to set the V_{OUT_B} node to values close to 0 V; this situation occurs in the VRL 1. Furthermore, the use of the on-chip analog

Table 5.8: DNL statistics of DAC at 8 K via on-chip buffer, regarding VRL (Test 2).

VRL	$V_{o_{DAC}}$ range	σ	mean	max.	min.
1	0 V - 125 mV	0.9681 V_{LSB}	−0.0818 V_{LSB}	2.9108 V_{LSB}	−2.6968 V_{LSB}
2	125 mV - 250 mV	1.0212 V_{LSB}	−0.0100 V_{LSB}	3.3824 V_{LSB}	−2.6667 V_{LSB}
3	250 mV - 375 mV	1.0951 V_{LSB}	−0.0106 V_{LSB}	3.9053 V_{LSB}	−2.7764 V_{LSB}
4	375 mV - 500 mV	1.0628 V_{LSB}	−0.0062 V_{LSB}	3.3656 V_{LSB}	−2.2120 V_{LSB}
5	500 mV - 625 mV	1.1289 V_{LSB}	−0.0185 V_{LSB}	3.6372 V_{LSB}	−2.3633 V_{LSB}
6	625 mV - 750 mV	1.2394 V_{LSB}	−0.0209 V_{LSB}	3.5875 V_{LSB}	−4.2539 V_{LSB}
7	750 mV - 875 mV	1.3264 V_{LSB}	−0.0072 V_{LSB}	4.1494 V_{LSB}	−4.0101 V_{LSB}
8	875 mV - 1 V	1.4668 V_{LSB}	−0.0169 V_{LSB}	4.6012 V_{LSB}	−4.9635 V_{LSB}

voltage buffer also increases the DAC DNL variation, as can be seen in Figure 5.22. Nevertheless, the progressive increase of the DNL variation, with respect to the VRL used by the DAC still remains; Table 5.8 provides additional statistical information.

In order to characterize the voltage noise spectrum generated by the DAC, a LNA (SR560) is used as intermediate stage between the V_{OUT_B} node and the input port of the SSA (E5052B). This is because the on-chip analog buffer is not able to drive the input port of the SSA; Appendix C provides a description of the voltage noise measurement setup calibration procedure.

The voltage noise amplitude spectral densities measured in this test are shown in Figure 5.23. It can be observed that in the 10 Hz - 100 Hz BW, the voltage noise generated by the buffered DAC output scales with the VRL at use. Moreover, in this BW the DAC seems to completely sample the voltage noise generated by the PMU, when the VRL 8 is used.

This behavior is related to the voltage division performed by the resistor network used in the multiple ICs system. However, for frequencies higher than 200 Hz, the influence of the PMU voltage noise reduces, while the noise generated by the on-chip analog voltage buffer and the charge redistribution DAC dominate the spectra. Table 5.9 lists the RMS voltage noise values measured in this test, as to quantify the the noise spectra behavior previously described; the RMS values are calculated with Eq. (4.10).

Finally, as the spurs appearing in the noise spectra are due to the DAC operation, it can be concluded that the EMC techniques applied for the cryogenic heterogeneous integration of the electronics and the GM cryocooling systems effectively suppress the influence of extrinsic noise sources.

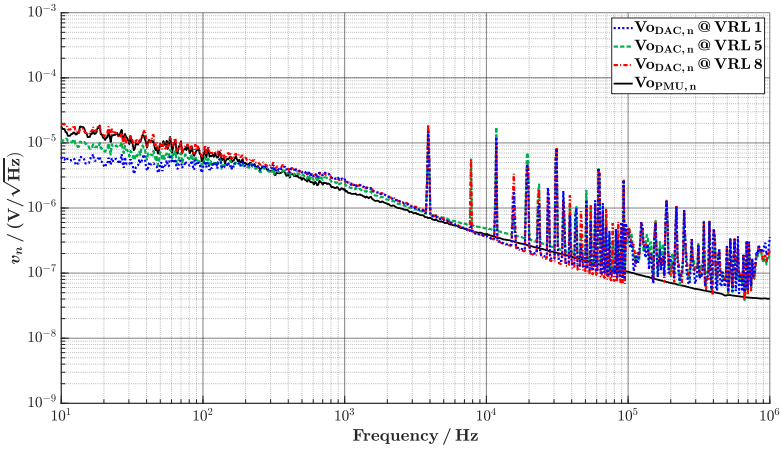


Figure 5.23: Voltage noise amplitude spectral densities measured from the DAC output (V_{OUT_B}) of the multiple ICs system at 8 K (Test 2); the on-chip analog voltage buffer and LNA (SR560) are used as support circuits to drive the SSA (E5052B) input port. The noise spectrum generated by the PMU at 8 K is added for comparison.

Table 5.9: Measured RMS voltage noise values in Test 2.

BW	10 Hz – 100 Hz	10 Hz – 10 kHz	10 Hz – 1 MHz
$V_{o_{DAC,n}}$ **@ VRL 1**	46.40 μV_{rms}	200.11 μV_{rms}	507.67 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 2**	45.50 μV_{rms}	217.91 μV_{rms}	565.75 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 3**	49.09 μV_{rms}	212.76 μV_{rms}	558 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 4**	57.40 μV_{rms}	198.71 μV_{rms}	535.69 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 5**	65.63 μV_{rms}	213.26 μV_{rms}	550.07 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 6**	77.75 μV_{rms}	208.88 μV_{rms}	526.89 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 7**	88.86 μV_{rms}	217.03 μV_{rms}	526.67 μV_{rms}
$V_{o_{DAC,n}}$ **@ VRL 8**	102.93 μV_{rms}	258.35 μV_{rms}	523.50 μV_{rms}
$V_{o_{PMU,n}}$	96.49 μV_{rms}	157.21 μV_{rms}	173.98 μV_{rms}

5.5.1.3 Test 3: DAC Output Voltage Measurement, with Active Signal Biasing Circuit, via Analog Buffer

Taking advantage of the extrinsic noise suppression provided by the applied EMC techniques, this test seeks to analyze the charge redistribution DAC sensitivity to voltage noise signals appearing on its reference voltages, $V_{Ref,U}$ and $V_{Ref,L}$. For that purpose, the

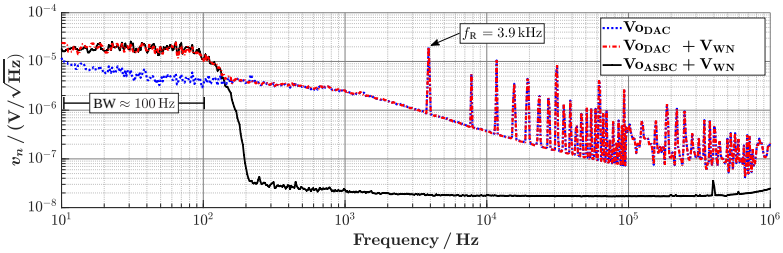


Figure 5.24: Voltage noise amplitude spectral densities measured from DAC output at 8 K (Test 3). The active signal biasing circuit biases the resistor network with a DC potential of 1 V and a white noise signal set for BW ≈ 100 Hz.

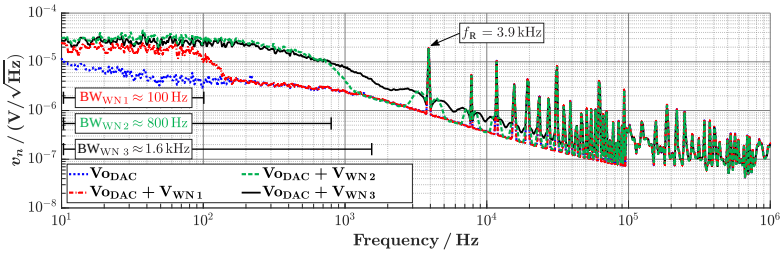


Figure 5.25: Voltage noise amplitude spectral densities measured from DAC output at 8 K (Test 3). The active signal biasing circuit biases the resistor network with a DC potential of 1 V and a white noise signal; the BW is set for 100 Hz, 800 Hz and 1.6 kHz.

PMU is disconnected from the resistor network and it is substituted by the active signal biasing circuit, which is operated at RT. With the active signal biasing circuit, the resistor network is biased with a DC potential of 1 V, together with an AC test signal; Appendix B provides a description of this support system. Moreover, the DAC is set to operate with the VRL 8. As this configuration provides the highest voltage values for $V_{\text{Ref, U}}$ and $V_{\text{Ref, L}}$. Consequently, the DAC is also set for the highest noise inclusion in its voltage references, as demonstrated by the measurement shown in Figure 5.23. Apart from these modifications, Test 3 uses the same measurement setup as Test 2.

Figure 5.24 compares the noise spectra generated by the DAC output, with and without the addition of a white noise signal via the active signal biasing circuit. In this case the noise signal is set for BW ≈ 100 Hz. As can be observed, the DAC samples the low frequency white noise signal. Besides, for frequencies above 3.9 kHz, the DAC output noise spectra are dominated by harmonics associated with the sample and hold refresh process since f_R = 3.9 kHz.

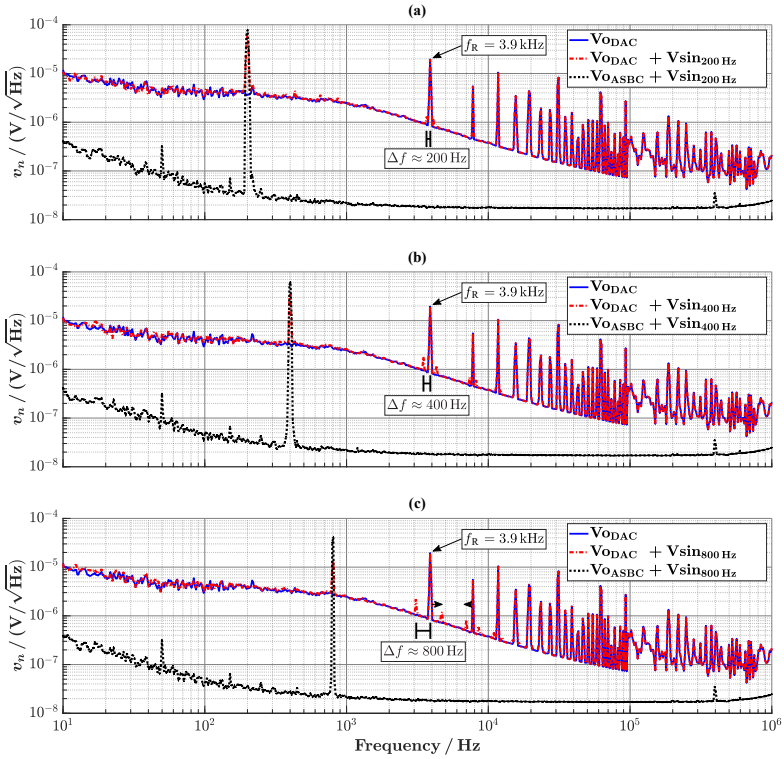


Figure 5.26: Voltage noise spectra measured from DAC output at 8 K (Test 3). The active signal biasing circuit biases the resistor network with a DC potential of 1 V and an AC sine signal of 0.2 mV_{rms}. (a) $f_{\text{sin}} = 200\,\text{Hz}$, (b) $f_{\text{sin}} = 400\,\text{Hz}$, and (c) $f_{\text{sin}} = 800\,\text{Hz}$.

This analysis is extended to white noise signals of wider BW, as is shown in Figure 5.25. With BW $\approx$ 800 Hz the DAC still performs the noise signal sampling. However, side bands appear around its harmonics. Furthermore, when the noise signal BW is set for 1.6 kHz, the DAC sampling process is cluttered, as the side bands around the harmonics interfere with the sampled white noise signal.

In order to get a better understanding of the DAC behavior, the stimulus white noise signal is replaced by a sine signal, as is shown by the measurements in Figures 5.26 and 5.27. When $f_{\text{sin}} = 200\,\text{Hz}$, the added sine signal appears to be perfectly sampled by the DAC. Also, side bands appear around the first harmonic (3.9 kHz) and they are spaced by 200 Hz around the harmonic. A similar situation occurs for $f_{\text{sin}} = 400\,\text{Hz}$ and $f_{\text{sin}} = 800\,\text{Hz}$. Though, the amplitude of the sample sine signal is reduced as its frequency

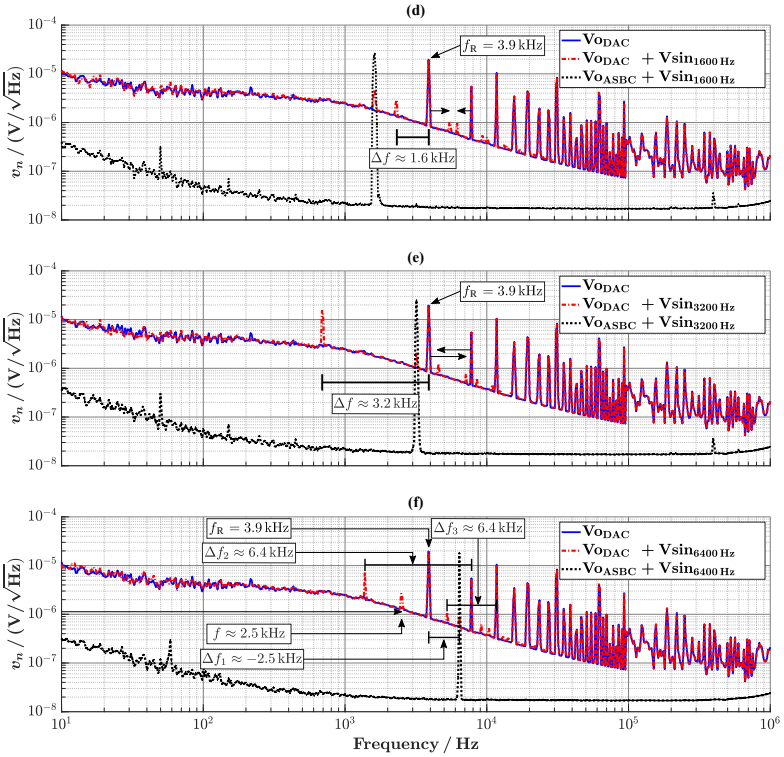


Figure 5.27: Voltage noise spectra measured from DAC output at 8 K (Test 3). The active signal biasing circuit biases the resistor network with a DC potential of 1 V and an AC sine signal of 0.2 $\mathrm{mV_{rms}}$. (d) $f_{\mathbf{sin}} = 1.6\,\mathrm{kHz}$, (e) $f_{\mathbf{sin}} = 3.2\,\mathrm{kHz}$, and (f) $f_{\mathbf{sin}} = 6.4\,\mathrm{kHz}$.

increases; similarly to a low-pass filter. Moreover, at higher frequencies the side bands around higher harmonics become noticeable. Under this conditions, the DAC appears to behave as a discrete low-pass filter that generates modulation side band signals around the harmonics of the sampling frequency (f_R).

At $f_{\mathbf{sin}} = 1.6\,\mathrm{kHz}$, the first harmonic side band signal gets closer to the sampled sine signal. But, since $f_R > 2f_{\mathbf{sin}}$, these signals are not clashing and aliasing phenomenon is not occurring. In contrast, when $f_{\mathbf{sin}} = 3.2\,\mathrm{kHz}$, the first harmonic side band signal extends to 700 Hz, producing in this way aliasing. The situation gets worse when $f_{\mathbf{sin}} = 6.4\,\mathrm{kHz}$, as the spectrum becomes populated by a higher amount of side band signals, including side band signals related to the negative frequency sampling harmonics.

Several conclusions can be drawn from the results obtained by this test. First, due to the intrinsic sampling process performed by the charge redistribution DAC, any noise signal appearing on $V_{\text{Ref, U}}$ and $V_{\text{Ref, L}}$ will be transferred to the converter output voltage. And, if the noise signal frequency extends beyond f_{R}, the converter output voltage will be cluttered with aliasing signals.

A solution to this situation could be the implementation of anti-aliasing filters between the reference voltages and the DAC. However, if extrinsic noise sources affect an electronic system cooled by a cryocooler, the efficiency of the anti-aliasing filters is uncertain. Finally, this test showcases the importance of the signals integrity in the cryogenic heterogeneous integration of the electronic and cryocooling systems.

5.5.2 Discussion

The results obtained from the evaluation tests demonstrate that the components of the multiple ICs system can operate together at CTs, as to perform an specific function. In addition, the results also indicate that the EMC techniques applied for the integration of the multiple ICs system and the GM cryocooler (attodry800), effectively suppress the influence of extrinsic noise sources that could distort the signal and power integrity of the electronics and measurement setup. In this way it is possible to perform a study of the charge redistribution DAC sensibility to voltage noise signals appearing on its reference voltages, $V_{\text{Ref, U}}$ and $V_{\text{Ref, L}}$.

The test results significance lays on the fact that they allow to establish a certainty over the amount of voltage noise that can be tolerated by the DAC in its reference voltages, beyond the ideal quantity of $0\,\text{V}_{\text{rms}}$. Considering that in Test 1 the lowest DNL variation is obtained with VRL 1 ($\sigma = 0.1494\,\text{V}_{\text{LSB}}$), and confirming in Test 2 that the DAC samples the voltage noise of its references in proportion with the VRL at use, it can be estimated that a voltage noise spectral density eight times smaller that the one from the PMU could by tolerated by the DAC; i.e. close to $12\,\mu\text{V}_{\text{rms}}$, between 10 Hz and 100 Hz.

Finally the results obtained by the cryogenic test of the multiple ICs system serve as validation of the technical approaches used to perform the cryogenic heterogeneous integration between the electronics and GM cryocooler (attodry800). Accordingly, the applied techniques could be used in the development of measurement protocols for the cryogenic test of prototype ICs, which require an environment free of extrinsic noise sources for its electrical validation.

Chapter 6

Conclusions and Outlook

6.1 Conclusions

There is no doubt that the cryogenic CMOS IC technology will be a key enabler for the scalability of QC systems. Given the importance of the CMOS IC technology, this work presented the development, integration and test of a cryogenic PMU composed by a CMOS IC and additional passive components. The ultimate goal is to provide a regulated and low noise voltage supply to other circuit blocks located at cryogenic environments close to 4 K with a cryogenic PMU. In this way, the power integrity of the cryogenic electronics is improved, and the amount of DC connections between the RT equipment and the cryogenic electronics is reduced. Consequently, the QC systems scalability efforts are thereby supported.

In this work, the analog MOS circuits employed to produce the cryogenic PMU are a voltage reference and a linear voltage regulator. These circuits are developed with a 22 nm FDSOI technology, as it supplies MOS transistors that can operate at CTs without significant performance degradation. Moreover, these circuits are used for the cryogenic performance evaluation of such a technology.

In addition, the measurement data obtained by a DC characterization of the 22 nm FDSOI technology demonstrate that the cryogenic V_{th} increase, and the subsequent increment in voltage supply requirements of the cryogenic analog MOS circuits can be countered with V_{th} tuning via the back-gate of the FDSOI MOS transistors. Also, this work showcased the use of the cryogenic V_{th} saturation exhibited by the I/O NMOS transistor, settled to 578 mV in the 6 K – 50 K range, as a working principle for the production of cryogenic voltage references.

Besides, the effect that the cryogenic g_{m} increase has on a voltage regulator performance is also observed in this work, and it directly improves the circuit load regulation and PSRR. This is because the regulator loop gain (A_{LG}) is proportional to g_{m}, while its load regulation and PSRR are inversely proportional to A_{LG}; i.e., as g_{m} increases at CTs, the regulator load regulation and PSRR improve, as indicated by Equations 4.6, 4.8 and 4.9.

Table 6.1: Comparison between the design specifications and the measured characteristics of the cryogenic PMU implemented in this work.

Parameter	**Specification**	**Implementation**
Supply voltage (V_{Sup})	2 V	2 V
Regulated output voltage (V_{Reg}) range	0.7 V-1 V	0.8 V-1.15 V @ 6 K
Load current (I_{Load}) range	1 µA-10 mA	1 µA-10 mA @ 6 K
Load regulation (LR) @ ΔA = 10 mA	50 mV/A	22 mV/A @ 6 K
Power supply rejection ratio (PSRR)	−50 dB	−56.83 dB @ 6 K, 1 kHz
Integrated output noise @ BW= 10 Hz-10 kHz	200 μV_{rms}	157.21 μV_{rms} @ 8 K

Furthermore, the occurrence of the LF excess noise is observed at CTs in the voltage reference and voltage regulator circuits. This occurs because the LF excess noise at CTs is correlated with the MOS transistor SiO_2 interface traps density; i.e. the capture and release of charge carriers induced by interface traps substantially contribute to the MOS transistor cryogenic LF noise. As indicated by Table 4.2, in both circuits the LF RMS voltage noise increased by 90 % at 8 K, with respect to 300 K. All of these facts highlight the need for the adoption of low noise circuit design techniques in cryogenic applications that are sensible to LF noise.

Essentially, the 22 nm FDSOI technology possesses MOS transistors whose electrical characteristics are suitable for the development of cryogenic analog MOS circuits that are intended for QC applications. Nevertheless, the development of cryogenic simulation models representing the FDSOI MOS transistors characteristics, including their intrinsic electrical noise, is required for the optimal design of cryogenic analog circuits.

As an initial endeavour, the cryogenic PMU in this work possesses electrical characteristics that matches the design specifications proposed in section 2.4; Table 6.1 provides a comparison between the cryogenic PMU design specifications and its measured characteristics. Hence, an improvement of the cryogenic PMU electrical performance could be obtained by applying low noise and low power circuit design techniques during its development. In combination with the use of cryogenic simulation models of the FDSOI MOS transistor. Besides, in this work the PMU functionality is showcased at CTs.

Additionally, the cryogenic heterogeneous integration between a multiple ICs system and the GM cryocooler is developed in order to achieve an accurate, repeatable, and extrinsic noise-free performance test of the cryogenic electronic system. In this way the combined operation at CTs of a charge redistribution DAC and the PMU is demonstrated. Moreover, the cryogenic heterogeneous integration is achieved by applying EMC techniques that improve the signal and power integrity of the cooled electronics.

Allowing the study of the DAC sensitivity to extrinsic noise signals. Besides, the relevance of the EMC techniques application for the performance evaluation of cryogenic ICs is also demonstrated.

Finally, it is expected that the information and outcomes provided by this work support the advancement of the cryogenic analog MOS circuit design and test discipline.

6.2 Outlook

In the framework of upcoming projects, the integration of cryogenic electronics with the dilution unit of the CF-CS110-1500M-2PT system via a sample insert, is under development; Figure 6.1 shows the current progress of this integration project. The electronics to be integrated are the PMU, resistor network, charge redistribution DAC and a die containing quantum dot devices [23, 139].

Beyond just testing the electronics cryogenic operation inside the dilution refrigerator, the ICs physical distribution across the different temperature stages will also be at test. Thus, by placing the PMU on the Still[2] stage, the operation of such an electronic system at 700 m K will be evaluated. In this way, information related to the operation of analog and digital circuit blocks designed with the 22 nm FDSOI technology will be obtained for that temperature.

In addition, since a dilution refrigerator usually dissipates around 20 mW as heat on the Still stage in order to control the ^{3}He flow and dilution cooling process, this integration project also seeks to evaluate the potential placement of electronic systems on the Still stage. Thus, the heat dissipated by the electronics may be used as part of the heating process performed on the Still stage of the dilution refrigerator, increasing in this way the available power dissipation budget of the cryogenic electronics. Therefore reducing the distance between the cryogenic electronics and the mixing chamber, the coldest stage in a dilution refrigerator holding the qubit devices. All of these possibilities are meant to be explored by the integration project.

It is also expected that the development of this project serves as training ground for the QC researchers at the Forschungszentrum Jülich - Central Institute of Engineering, Electronics and Analytics, Electronic Systems (ZEA-2); since 2025, Forschungszentrum Jülich - Integrated Computing Architectures (PGI-4). Because this project will provide first hand experience on the handling of a dilution cooling system such as the CF-CS110-1500M-2PT, in addition to the measurement and operation of quantum dot qubit devices.

[2] The Still of a dilution refrigerator is the element where the ^{3}He-^{4}He mixture is separated in order to allow the ^{3}He circulation. See section 2.1.3.

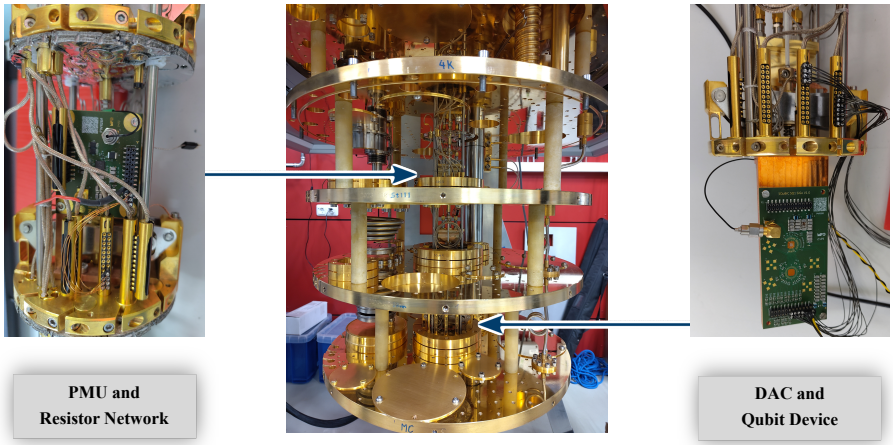


Figure 6.1: Integration of the multiple ICs system with the dilution unit of the CF-CS110-1500M-2PT system, via a sample insert; Leiden Cryogenics.

The development of cryogenic analog and mixed-signal CMOS ICs, in conjunction with cryogenic simulation models, will need to be continued in future endeavours in order to develop scalable QC systems. For example, the development of a cryogenic switched mode voltage regulation systems, such as a digital LDO voltage regulator, could benefit the development of high-performance digital systems operating at CTs [153]. While the application of low noise design techniques for the development of cryogenic analog circuits, such as voltage, current, transconductance and transimpedance amplifiers, will improve the performance of classical QC computing systems operating at CTs.

Equally significant for the development of scalable QC systems is the signal integrity analysis of the electronics located inside a dilution refrigeration system. Therefore, representing a relevant research topic in the filed of applied dilution refrigeration systems. Consequently, hardware developers must consider it when building a QC system.

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Curriculum Vitae

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Publications and Conferences

Journal Publications

Alfonso R. Cabrera-Galicia, Arun Ashok, Patrick Vliex, Andre Kruth, André Zambanini, and Stefan Van Waasen. "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology". In: *IEEE Open Journal of Circuits and Systems* 5 (2024), pp. 377–386. DOI: 10.1109/OJCAS.2024.3466395

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Posters and Presentations (Without Journal Publication)

Santosh Mutum, Christian Grewing, **Alfonso Rafael Cabrera Galicia**, Mario Schlösser, Patrick Vliex, Phanish Chava, and Stefan van Waasen. "Performance and signal quality analysis of a photonic link from room temperature to 6K using laser-photodiodes (poster)". In: Applied Superconductivity Conference 2024, Salt Lake City (USA), 1 Sep 2024 - 6 Sep 2024. Sept. 1, 2024. DOI: 10.34734/FZJ-2024-05996. URL: https://juser.fz-juelich.de/record/1032097

Patrick Vliex, Jonas Bühler, **Alfonso Rafael Cabrera Galicia**, Lea Schreckenberg, Rene Otten, and Stefan van Waasen. "Cryogenic CMOS for Local Qubit Control and Readout – A Path to Scaling (poster)". In: Silicon Quantum Electronics Workshop 2023, Kyoto (Japan). Oct. 31, 2023. DOI: 10.34734/FZJ-2023-04442. URL: https://juser.fz-juelich.de/record/1017935

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Master Thesis Supervision

Swasthik Baje Shankarakrishna Bhat. "Design of Digitally Enhanced Power Management Circuits for Future Quantum Computers". MA thesis. Technische Universität Hamburg, Apr. 13, 2023

Appendix A

Functional Test and Post-layout Simulation of Prototype IC

As part of the development process of the the prototype IC designed in this work, the functionality of its analog circuit blocks is experimentally evaluated at 300 K, 273.15 K and 233.15 K. In addition, the experimental measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT (typical - typical), FF (fast - fast), FS (fast - slow), SF (slow - fast) and SS (slow - slow). In this way, the efficiency of the IC design flow used in the development of the prototype IC is assessed.

Figures A.1, A.2, A.3 shows the results corresponding to the evaluation of the V_{th} saturation voltage reference. For all the evaluated temperatures, the experimental data is close to the results provided by the post-layout simulations performed with the process corners. Similarly, the evaluation results of the V_{th} difference based voltage reference are shown in Figures A.4, A.5 and A.6. Here, the experimental data is also close to the post-layout simulation results.

Regarding the voltage regulator developed in this work, Figures A.7, A.8 and A.9 show its load regulation at 300 K, 273.15 K and 233.15 K. It can be observed that in all cases there is a difference between the measured regulator output voltage (V_{Reg}) and the post-layout simulation results. This discrepancy may be attributed to the input offset voltage of the differential amplifier used for the implementation of the voltage regulator. Besides, due to the random nature of the differential amplifier input offset voltage, its effect is not considered by the corner models; a post-layout simulation based on Monte Carlo process variations centered in each process corner is required to observe the effect of the input offset voltage. In the case of the evaluated prototype IC, the input offset voltage is estimated to be around 6 mV to 8 mV. Nevertheless, it can be observed that under the evaluated temperatures, the measurement results and the simulation data follow a similar trend with respect to load regulation.

Finally, since the experimental measurements presented in this appendix correlate with the post-layout simulation results, the effectiveness of the IC design flow employed in this work has been demonstrated.

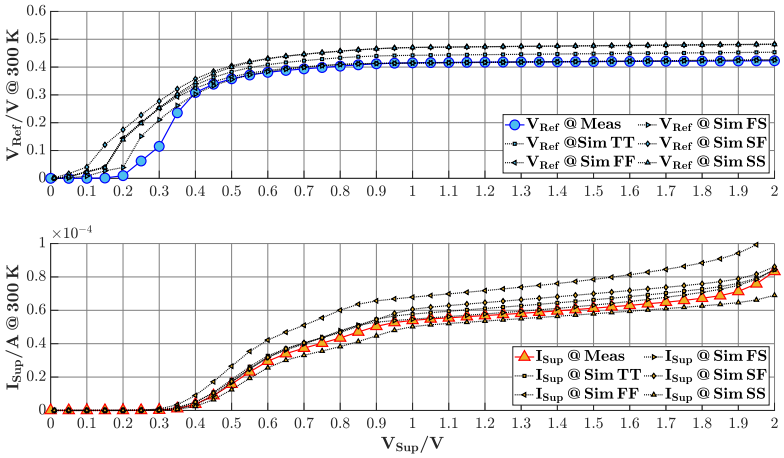

Figure A.1: Measured output voltage and current consumption of V_{th} saturation based voltage reference circuit with respect to supply voltage (V_{Sup}), at 300 K. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

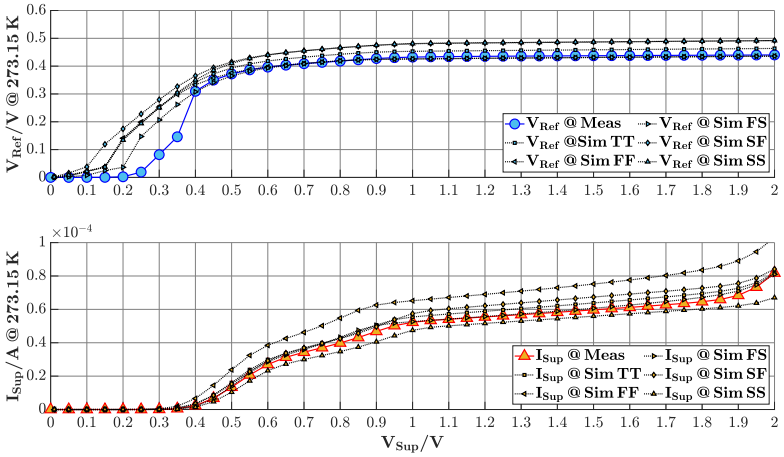

Figure A.2: Measured output voltage and current consumption of V_{th} saturation based voltage reference circuit with respect to supply voltage (V_{Sup}), at 273.15 K. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

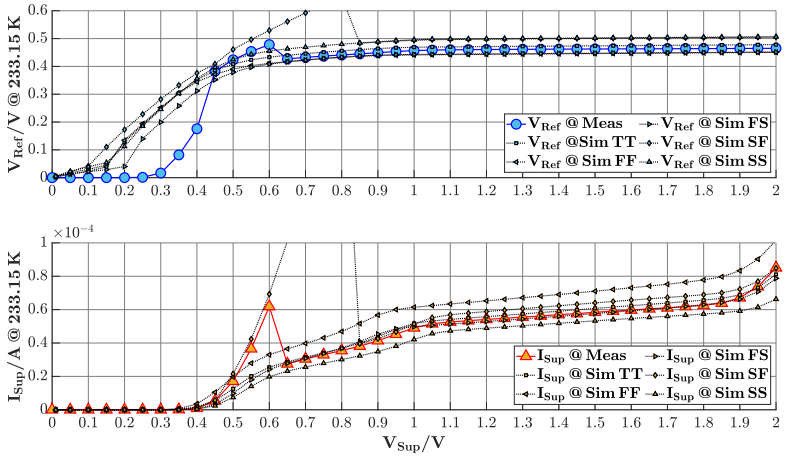

Figure A.3: Measured output voltage and current consumption of V_{th} saturation based voltage reference circuit with respect to supply voltage (V_{Sup}), at 233.15 K. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

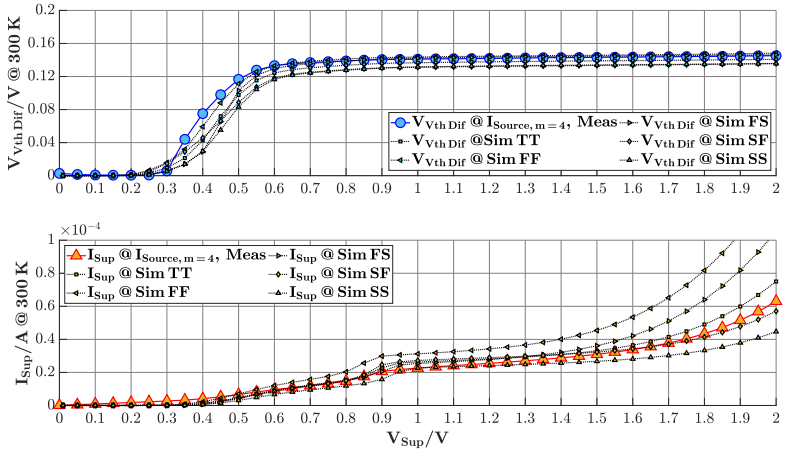

Figure A.4: Measured output voltage and current consumption of V_{th} difference based voltage reference circuit with respect to supply voltage (V_{Sup}), at 300 K. The current bias is set to $I_{Source,\,m=4}$. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

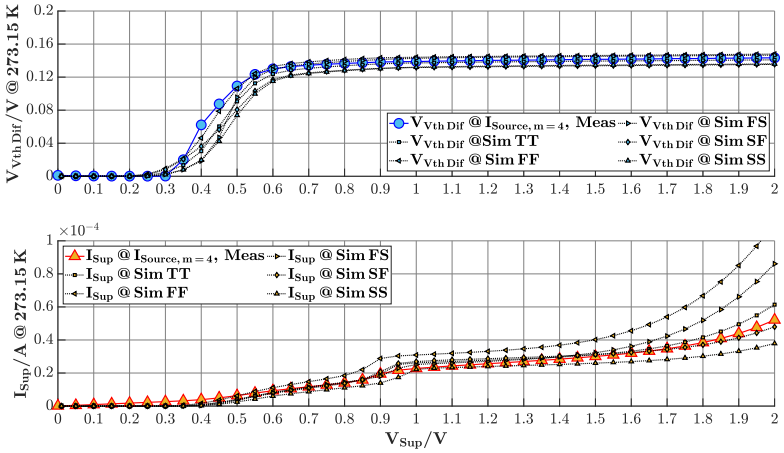

Figure A.5: Measured output voltage and current consumption of V_{th} difference based voltage reference circuit with respect to supply voltage (V_{Sup}), at 273.15 K. The current bias is set to $I_{Source,\,m=4}$. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

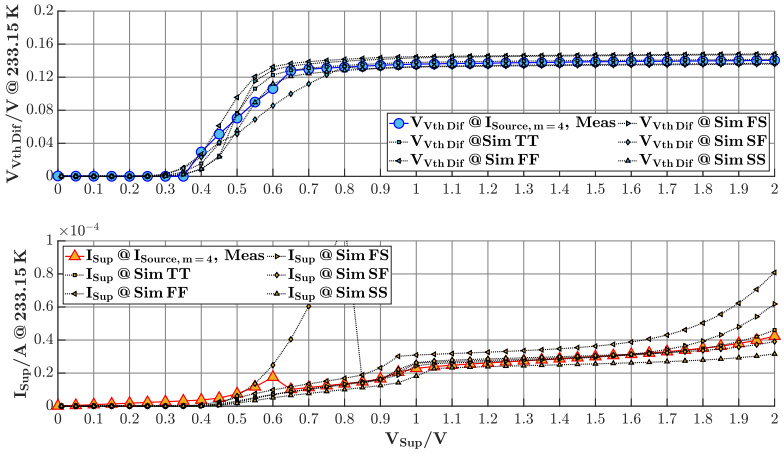

Figure A.6: Measured output voltage and current consumption of V_{th} difference based voltage reference circuit with respect to supply voltage (V_{Sup}), at 233.15 K. The current bias is set to $I_{Source,\,m=4}$. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

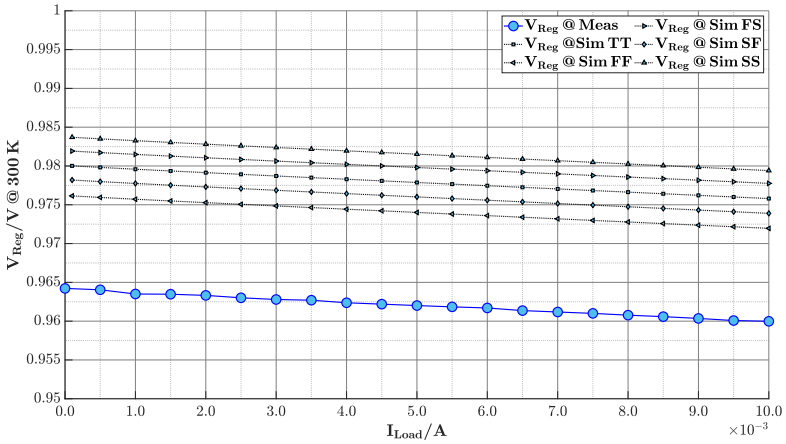

Figure A.7: Measured regulator output voltage (V_{Reg}) in relation to current load (I_{Load}) at 300 K; $V_{\mathrm{IN\,Ref}} = 0.5$ V, $R_{\mathrm{F1}} = R_{\mathrm{F2}}$, $V_{\mathrm{BG}} = 0$ V and $V_{\mathrm{Sup}} = 2$ V. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

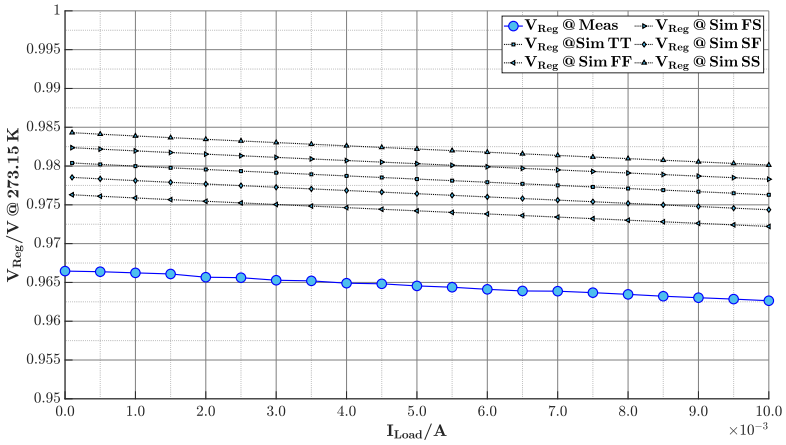

Figure A.8: Measured regulator output voltage (V_{Reg}) in relation to current load (I_{Load}) at 273.15 K; $V_{\mathrm{IN\,Ref}} = 0.5$ V, $R_{\mathrm{F1}} = R_{\mathrm{F2}}$, $V_{\mathrm{BG}} = 0$ V and $V_{\mathrm{Sup}} = 2$ V. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

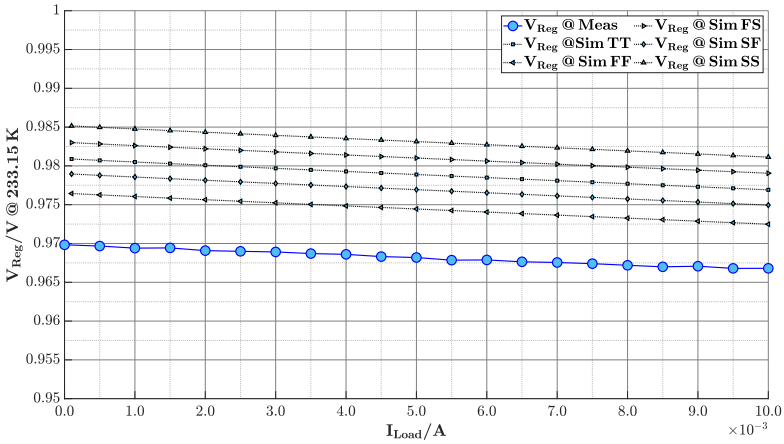

Figure A.9: Measured regulator output voltage (V_{Reg}) in relation to current load (I_{Load}) at 233.15 K; $V_{\text{IN Ref}} = 0.5$ V, $R_{\text{F1}} = R_{\text{F2}}$, $V_{\text{BG}} = 0$ V and $V_{\text{Sup}} = 2$ V. The measurement data is compared with post-layout simulation results obtained by using the process corners; i.e. TT, FF, FS, SF and SS.

Appendix B

Active Signal Biasing Circuit

The active signal biasing circuit shown in Figure B.1 is employed in this work as a support system for the development of some of the experimental measurements presented in this work. It establishes a DC voltage bias condition (V_{DC}) over which an small AC voltage signal (V_{AC}) is set, with higher output current drive capability than a common AWG. This functionality is used for the characterization of the voltage regulator PSRR (section 4.3), the RLC low-pass filter frequency response (section 5.3.3) and the charge redistribution DAC sensitivity to voltage reference noise (section 5.5.1.3).

The output voltage of the active signal biasing circuit can be approximated as in Equation B.1, under the consideration that $R_2 = R_3$ and $R_4 = R_5$.

$$\begin{aligned} V_{OUT} &\approx -\left(\frac{R_5}{R_4}\right) V_{DC} + \left(1 + \frac{R_5}{R_4}\right)\left(\frac{R_3}{R_2 + R_3}\right) V_{AC} \\ &\approx -V_{DC} + V_{AC} \end{aligned} \tag{B.1}$$

The circuit operation can be comprehended by dividing it into three stages. The first one (R_1, C_1 and IC_1) filters the DC reference voltage (V_{DC}) and decouple the RC filter from the next stage. The second stage (R_2, R_3, R_4, R_5 and IC_2) adds V_{AC} to $-V_{DC}$, as in Equation B.1; V_{DC} takes the negative sign due to the inverter configuration set by R_4, R_5 and IC_2. The last stage (R_6, R_7, C_2, IC_3 and IC_4) is a voltage follower which has a higher output current capability than an operation amplifier

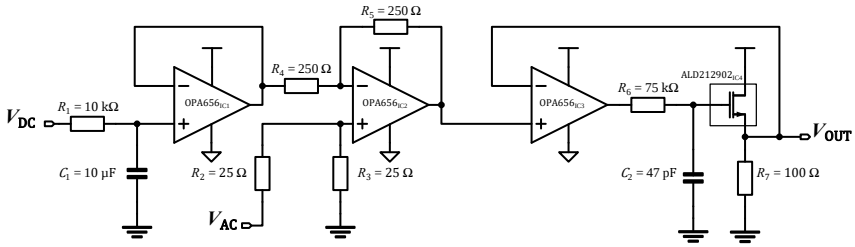

Figure B.1: Schematic view of the active signal biasing circuit employed in this work.

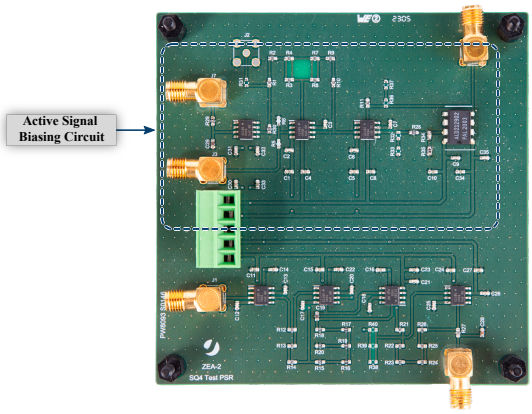

Figure B.2: Active signal biasing circuit PCB implementation.

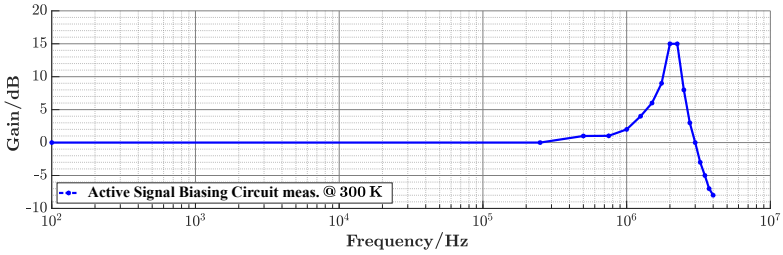

Figure B.3: Measured gain response of the active signal bias circuit with respect to frequency.

(OPA656). In this stage, R_6 and C_2 are used to set a low-frequency pole for loop compensation, while the NMOS pass device (ALD212902, with $V_{th} = 0.2\,V$) allows a wide range of positive output voltages. It must be mentioned that the third stage can only provide positive output DC voltage levels. Thus, V_{DC} must be set to a negative value in order to render a functional circuit.

A PCB implementation of the active signal biasing circuit is shown in Figure B.2. Moreover, Figure B.3 displays the gain response of the circuit measured along frequency when $V_{DC} = -1.8\,V$ and $V_{AC,P\text{-}P} = 2\,mV$. In this test a high-input impedance active probe (41800A), an AWG (33600A) and an spectrum analyzer (R&S FSU) are used; the setup is shown in Figure B.4. As can be seen in Figure B.3, the circuit has a peaking response close to 2 MHz which is associated to the amplifiers (OPA656) characteristics around this frequency. This situation limits the use of the circuit up to 1 MHz.

Alternatively, the circuit performance may be improved in a subsequent implementation by identifying the frequency components that produce the gain peak, in order to cancel them. Nevertheless, the circuit implementation presented in this work has shown an stable response, as

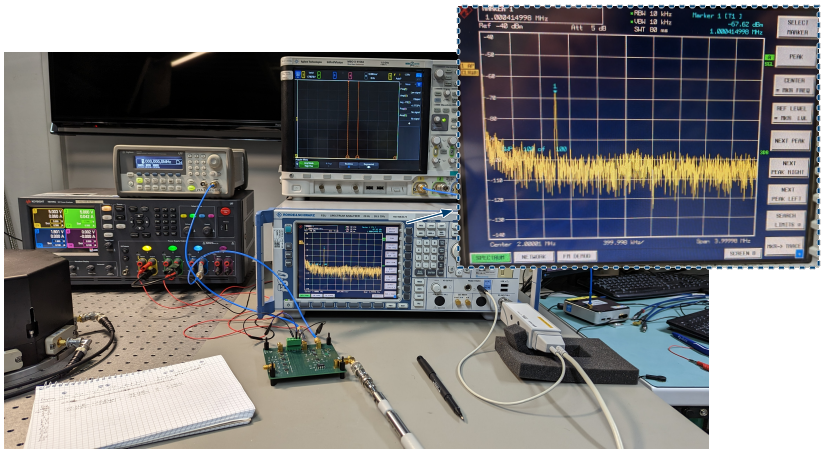

Figure B.4: Active signal biasing circuit PCB implementation.

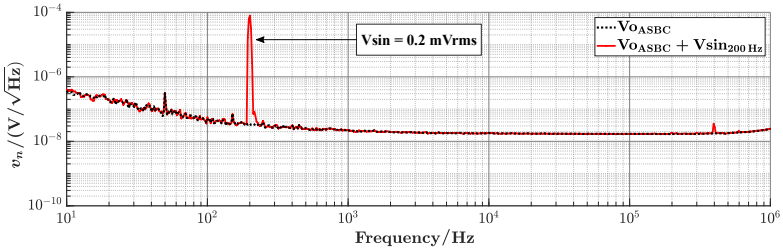

Figure B.5: Voltage noise amplitude spectral density measured at the output of the active signal biasing circuit, with and without a sine component ($V_{AC} = 0.2\,\mathrm{mV_{rms}}$ and $f = 200\,\mathrm{Hz}$).

Table B.1: Measured electrical characteristics of the active signal biasing circuit.

Temp.	V_{DD}	V_{SS}	P_{Dis}	$V_{OUT,n}$	f_{max}	$f_{-3\,dB}$
300 K	+5 V	−5 V	500 mW	19.09 μV_{rms}	1 MHz	3 MHz

demonstrated by its spectral characteristic shown in Figure B.4; only the added sine component ($f = 1\,\mathrm{MHz}$) appears in the spectrum.

As to showcase the circuit functionality with respect to electrical noise, Figure B.5 shows the voltage noise amplitude spectral density measured at its output, with and without a sine component; in this case $V_{AC} = 0.2\,\mathrm{mV_{rms}}$ and $f = 200\,\mathrm{Hz}$. In this measurement, AWG (33600A), LNA (SR560) and SSA (E5052B), are used. Moreover, a calibration methodology for voltage noise measurement with LNA (SR560) and SSA (E5052B), is described in the Appendix C. Thus, for a 10 Hz–1 MHz

bandwidth and $V_{AC} = 0\,V_{rms}$, $V_{OUT,n} = 19.09\,\mu V_{rms}$. In contrast, when $V_{AC} = 0.2\,mV_{rms}$, a sine component is added to the voltage noise spectrum at $f = 200\,Hz$ and $V_{OUT,n} = 203.43\,\mu V_{rms}$. The circuit electrical characteristics are summarized in Table B.1.

Appendix C

LNA (SR560) Calibration for Noise Measurement with SSA (E5052B)

One of the most important quantities that characterize the performance of an electronic system is the amount of intrinsic electrical noise that it produces. In other words, the amount of undesired random or systematic fluctuations that are produced by the system over its signals; e.g. voltage or current output noise.

In order to quantify this characteristic, the amount of power carried by an electrical signal must be measured along a defined frequency bandwidth. Thus, it is common to use an spectrum analyzer for that purpose, as it can measure the power contained by a voltage signal in a certain bandwidth. However, spectrum analyzers are intended to be used for the characterization of voltage signals that are produced by electrical systems capable of driving 50 Ω termination loads. This is a challenging situation for the electrical noise characterization of low power systems, since by design these systems are not able to drive such loads. Consequently, in this situation the use of an intermediate stage between a low power system and an spectrum analyzer is needed.

Such an intermediate stage must present an input port to the low power system that has high input resistance and low input capacitance, while it is also able to drive the input port of the spectrum analyzer. Thus, the intermediate stage must deliver a voltage signal to the spectrum analyzer that is proportional to the voltage signal generated by the low power system. This task can be performed by a Low Noise Amplifier (LNA) such as the SR560 [162]. Yet, some technical aspects must be considered to properly use an LNA in voltage noise measurements.

First, it is necessary to define the LNA gain as a function of frequency ($A_{\mathrm{v_{SR560}}}(f)$), since it is not constant due to the amplifier physical characteristics. For that purpose, the setups shown in Figure C.1 (a) – (b) are used. In this case, AWG (33600A), LNA (SR560) and SSA (E5052B), are employed. It is worth mentioning that the SSA (E5052B) contains a voltage noise measurement system similar to an spectrum analyzer [163]. Thus, the objective of the Figure C.1 (a) setup is to measure an amplified reference voltage noise signal ($v_{\mathrm{n,o}}$). On the other hand, the Figure C.1 (b) setup intends to measure the reference voltage noise signal ($v_{\mathrm{n,i}}$) without amplification. Then, by means of Equation C.1, a value for $A_{\mathrm{v_{SR560}}}(f)$ can be identified with the measured spectra.

$$A_{\mathrm{v_{SR560}}}(f) = \frac{v_{\mathrm{n,i}}}{v_{\mathrm{n,o}}} \tag{C.1}$$

When performing the voltage noise spectra measurements above described, it must be considered that:

- For proper signal transfer, the AWG (33600A) load option (Z_{Load}) must be set according to each setup; Z_{Load} = High-Z in Figure C.1 (a) and $Z_{\text{Load}} = 50\,\Omega$ in Figure C.1 (b).
- Power overloading of the SSA (E5052B) input port is prevented by setting the LNA (SR560) for $A_{\text{v}} = 1000$ and the AWG (33600A) for an small noise signal generation.
- The LNA (SR560) incorporates a matching resistor (R_{o} in Figure C.1) of 50 Ω at its output port. Therefore, when this amplifier drives a 50 Ω load, its output signal is reduced by a factor of 2. As a consequence, when measuring signals produced by the LNA (SR560) with the SSA (E5052B) this power reduction must be corrected by multiplying the measured data by 2. This does not apply for the AWG (33600A), since this device performs the power correction according to the value set for its Z_{Load} option.

Figure C.2 shows the measured voltage noise spectra and the equivalent $A_{\text{v}_{\text{SR560}}}(f)$. As can be seen, $A_{\text{v}_{\text{SR560}}}(f)$ maintains a constant value up to 1 MHz, frequency at which the LNA loses its gain. The next step is to measure the LNA intrinsic output noise ($v_{\text{n, o}_{\text{SR560}}}$) as indicated by the setup shown in Figure C.1 (c). Then, once $v_{\text{n, o}_{\text{SR560}}}$ and $A_{\text{v}_{\text{SR560}}}(f)$ are known, it is possible to define the LNA intrinsic input referenced noise ($v_{\text{n, i}_{\text{SR560}}}$) as in Equation C.2; the use of 2 as correcting factor is considered.

$$v_{\text{n, i}_{\text{SR560}}} = 2\frac{v_{\text{n, o}_{\text{SR560}}}}{A_{\text{v}_{\text{SR560}}}(f)} \tag{C.2}$$

Figure C.3 shows the measured LNA (SR560) input and output voltage noise spectral densities ($v_{\text{n, i}_{\text{SR560}}}$ and $v_{\text{n, o}_{\text{SR560}}}$), when $A_{\text{v}_{\text{SR560}}}(f) \approx 1000$. For these spectra and a 10 Hz–1 MHz bandwidth, $V_{\text{i}_{\text{SR560, n}}} = 5.39\,\mu\text{V}_{\text{rms}}$ and $V_{\text{o}_{\text{SR560, n}}} = 4.6\,\text{mV}_{\text{rms}}$. This confirms that $A_{\text{v}_{\text{SR560}}}(f) \neq 1000$; in fact, for $f > 400\,\text{kHz}$, $A_{\text{v}_{\text{SR560}}}(f)$ begins to decay as shown in Figure C.2. Hence, knowing $v_{\text{n, i}_{\text{SR560}}}$, and consequently $V_{\text{i}_{\text{SR560, n}}}$, allows to establish a noise floor level for voltage signal measurements with Figure C.1 (d) setup.

Finally, with Equation C.3 and Figure C.1 (d) setup, a calibrated voltage noise amplitude spectral density ($v_{\text{n, Cal}}$) of a DUT can be obtained from a raw noise measurement ($v_{\text{n, SSA meas}}$).

$$v_{\text{n, Cal}} = 2\frac{v_{\text{n, SSA meas}}}{A_{\text{v}_{\text{SR560}}}(f)} \tag{C.3}$$

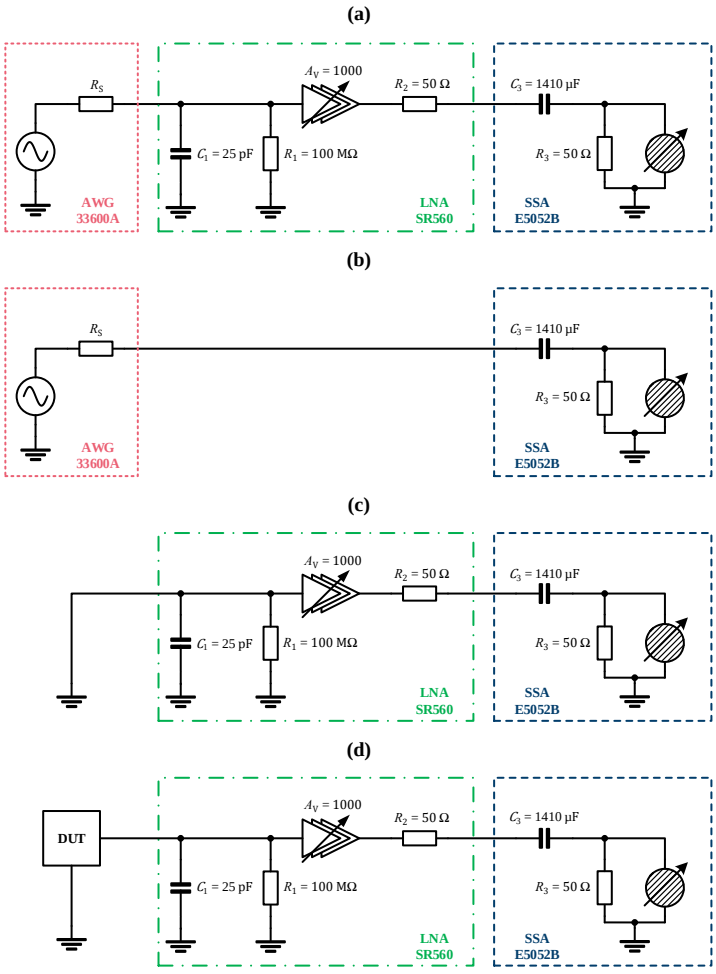

Figure C.1: LNA (SR560) calibration setups for voltage noise measurement with SSA (E5052B). **(a)** Measurement of amplified reference voltage noise signal. **(b)** Measurement of non-amplified reference voltage noise signal. **(c)** Measurement of SR560 LNA intrinsic output voltage noise. **(d)** Measurement of output voltage noise generated by a DUT after LNA (SR560) calibration.

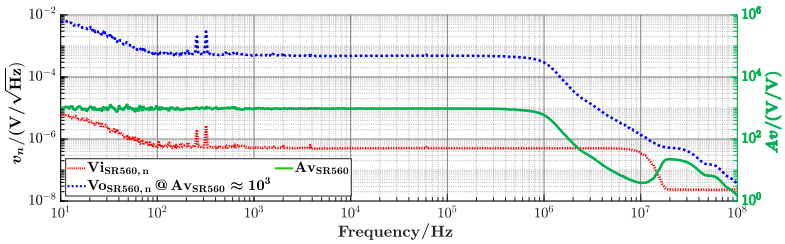

Figure C.2: Voltage noise amplitude spectral densities measured from a reference noise signal, with and without amplification ($v_{\mathrm{n,\,o}}$ and $v_{\mathrm{n,\,i}}$). These spectral densities are used for the definition of the LNA (SR560) voltage gain ($A_{\mathrm{V_{SR560}}}(f)$).

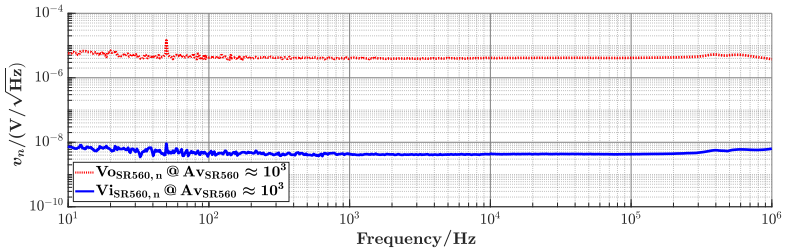

Figure C.3: Measured LNA (SR560) input and output voltage noise spectral densities ($v_{\mathrm{n,\,i_{SR560}}}$ and $v_{\mathrm{n,\,o_{SR560}}}$), when $A_{\mathrm{V_{SR560}}}(f) \approx 1000$.

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