AUTOMATED CO-DESIGN OF QUBITS AND CRYOGENIC ELECTRONICS

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MOTIVATION

- Need for common understanding between quantum physicists and electrical engineers to enable **scalable qubit-electronics interfaces**
- Interdisciplinary IC Verification via **Co-Simulation**
- Interdisciplinary IC Optimization via **Co-Design**

METHODS

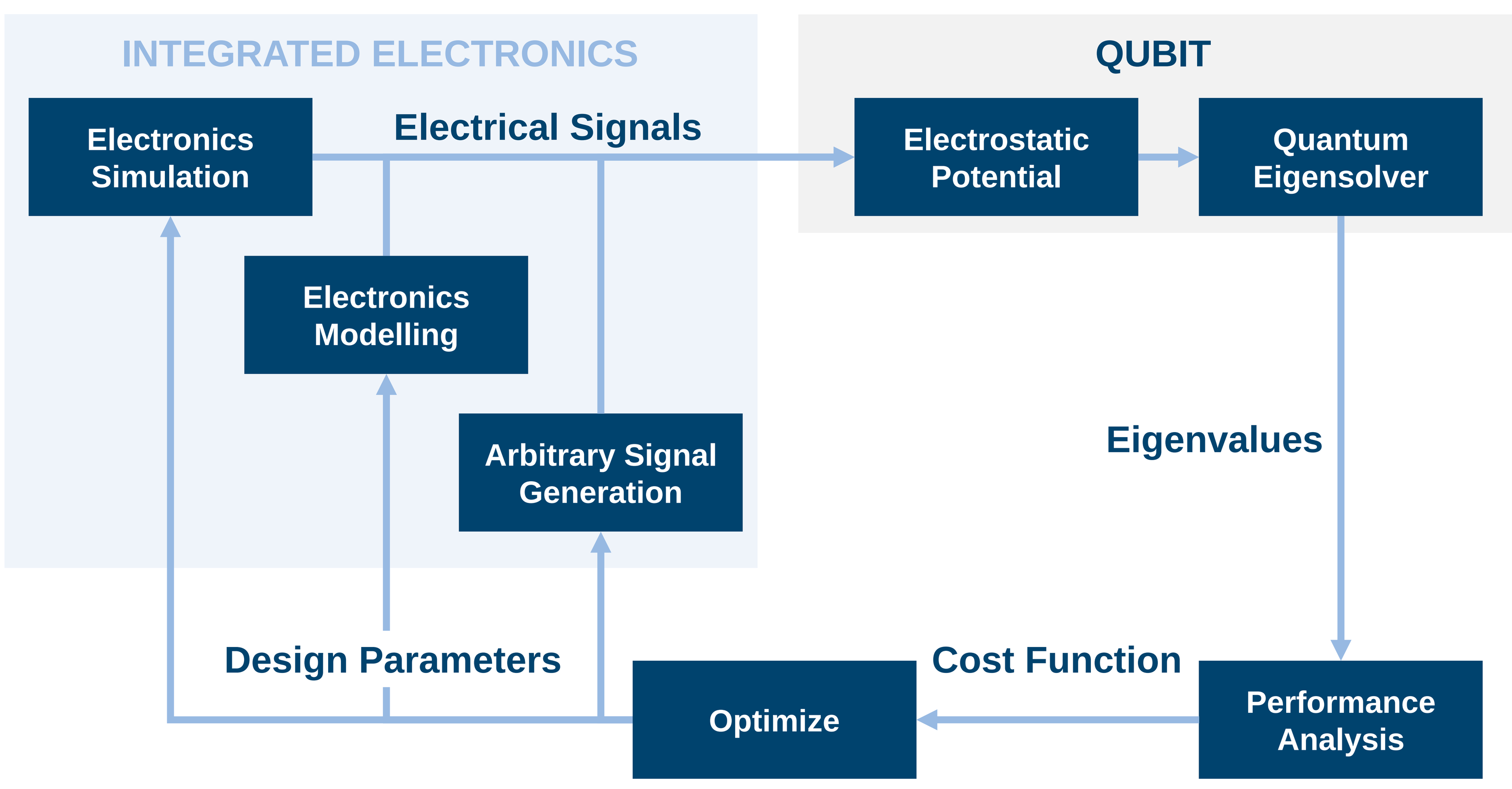
Systems Engineering:

Electronic design is constrained by system and qubit requirements.

System Requirements	$A_{1\ million\ qubits} = 0.25\ cm^2$ $P_{cooling\ 1\ million\ qubits} = 3\ W$
Control Electronics	Low Clock Frequency → Digital Power Low Signal Amplitude → Analog Power Tight Electronic Specifications → Footprint Optimized Signal Waveform → Analog Power
Qubit Requirements	$d_{shuttle} = 10\ \mu m$ $E_{orb} = 1\ meV$ $v_{shuttle} = 5\ \frac{m}{s}$

Co-Design Workflow:

- First, the ideal shuttling signal is determined.
- Second, a behavioral circuit model approximates the ideal signal.
- Finally, the simulated IC design is fine-tuned.



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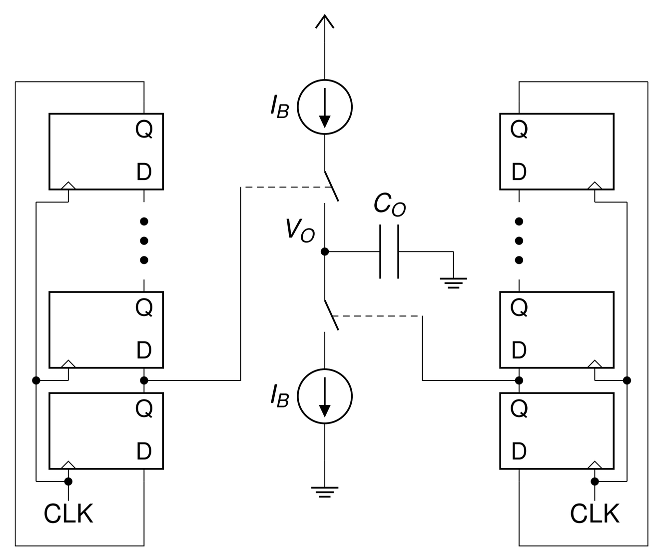
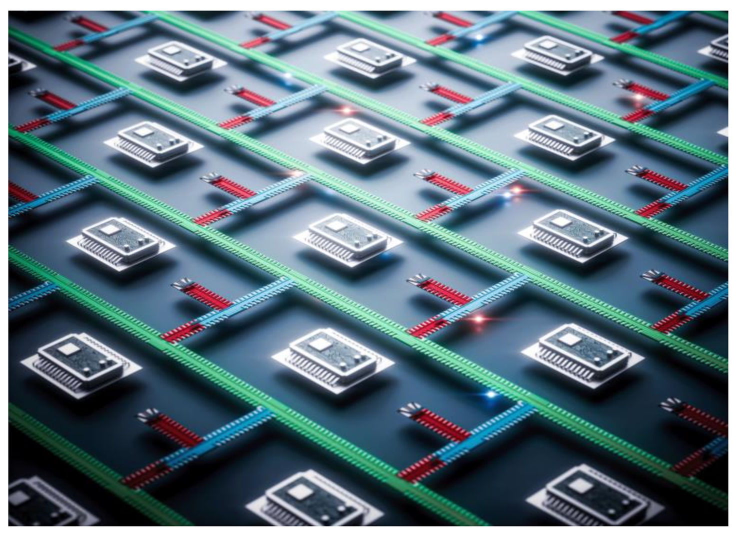
RESULTS

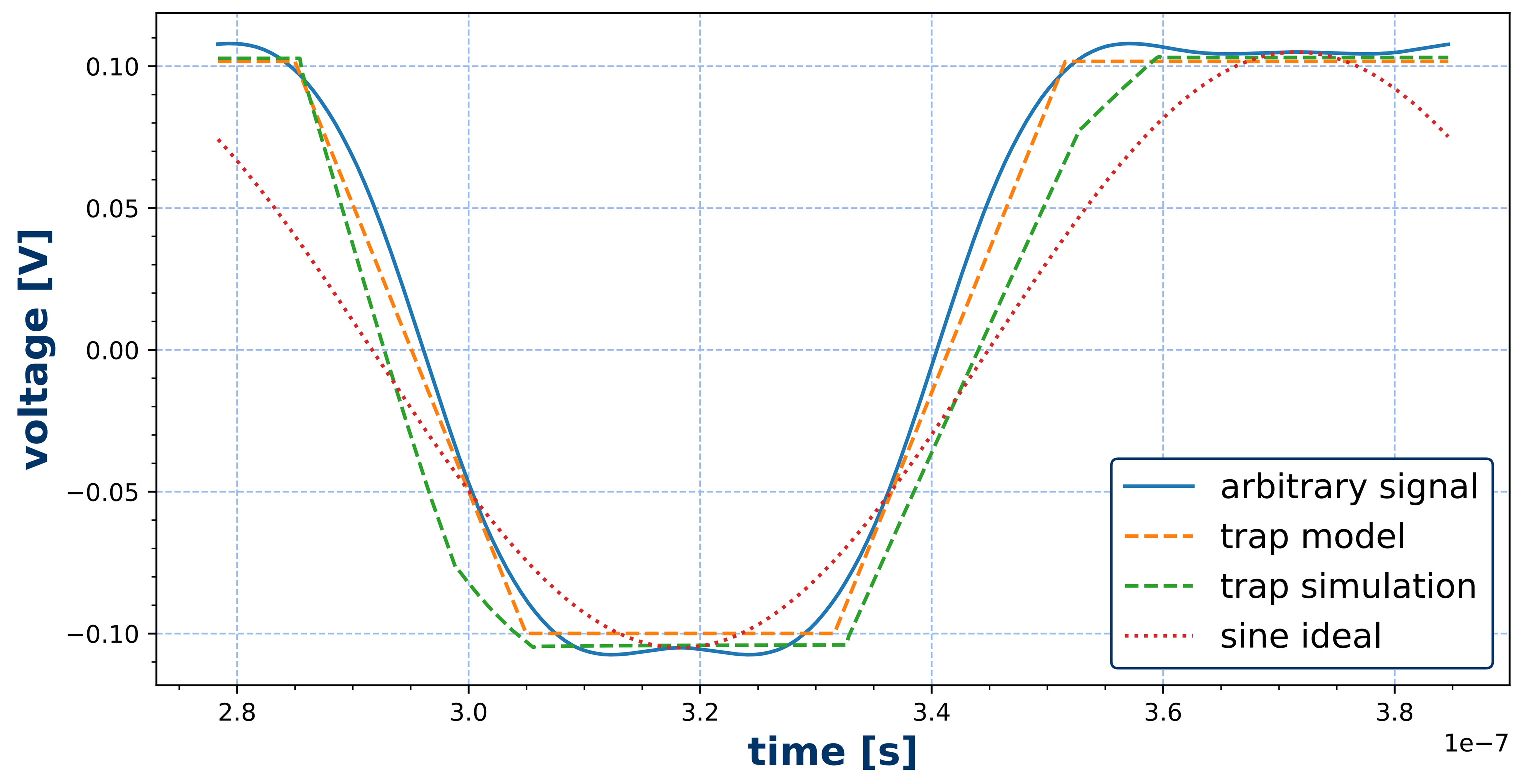
The circuit parameters and shuttle signals have been optimized in an automated three-step process.



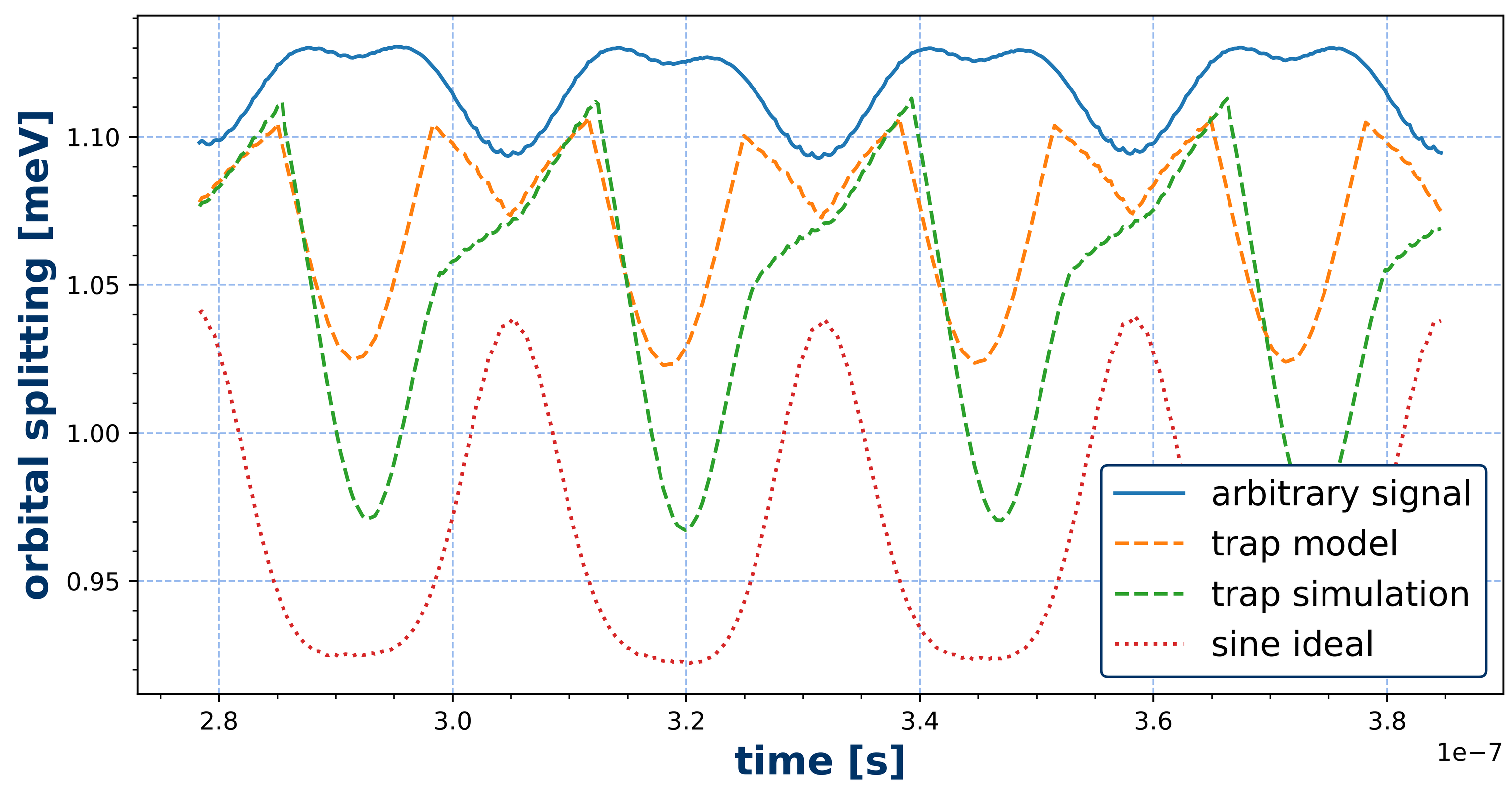
Circuit Topology of Trapezoidal Signal Generator [1] © 2025 IEEE



SpinBus Architecture representing a sparse qubit grid for Spin Qubits [2]



Shuttling Waveform in the different abstraction levels of the co-design process starting from an ideal signal to a transistor-level-simulation.



Resulting confinement of the electron qubit expressed by the orbital splitting which influences robustnes against disturbances. A minimal orbital splitting energy of 1 meV with minium power consumption of 3.6µW was determined.

CONCLUSION & OUTLOOK

- The co-design framework [1] has been demonstrated on the use case of spin qubit shuttling.
- Two circuits were optimized to achieve the qubit orbital splitting requirements while minimizing power dissipation.
- Next, the co-design will be extended to increase shuttling fidelity in a valley aware valley splitting shuttling path.

COOPERATION

PGI-8, Forschungszentrum Jülich GmbH
Shuttling Strategies using optimized velocity Modulation

PGI-11, Forschungszentrum Jülich GmbH
Experimental Physics and Qubit Development

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Planned Spin-Off and associated Partner

[1] Dietz Romero, P., Toprak, C., Duipmans, L., van Waasen, S., & Geck, L. (2025). Co-simulation for automated optimization of integrated cryogenic qubit electronics. SMACD Conference. Figures reprinted with permission from IEEE © 2025 IEEE
[2] Künne, M., Willmes, A., Oberländer, M., Gorjaew, C., Teske, J., Bhardwaj, H., Beer, M., Kammerloher, E., Otten, R., Seidel, I., Xue, R., Schreiber, L., & Bluhm, H. (2024). The SpinBus architecture: Scaling spin qubits with electron shuttling. Nature Communications.