Towards Scalable Cryogenic Charge Transition Detection for Automated Quantum Dot Tuning

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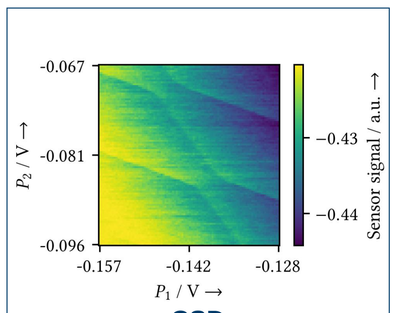
Motivation

Quantum dot qubits are controlled via electrostatic gate voltages

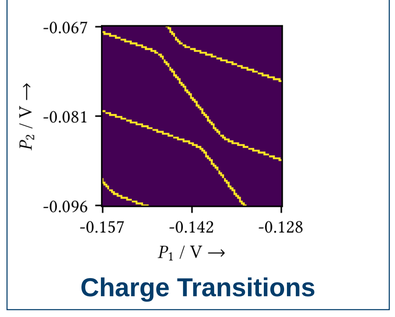
Scaling to a million-qubit processor requires automated tuning

Bottlenecks:
- Reliable detection of charge transitions in charge stability diagrams (CSDs)
- Limited bandwidth for transferring raw measurement data to room temperature

→ **Solution:** automation must be lightweight, generalizable, and implemented directly at the cryogenic stage



CSD

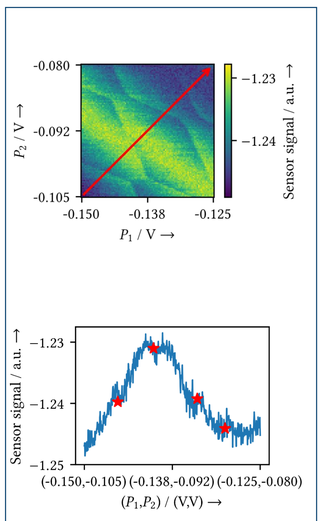


Charge Transitions

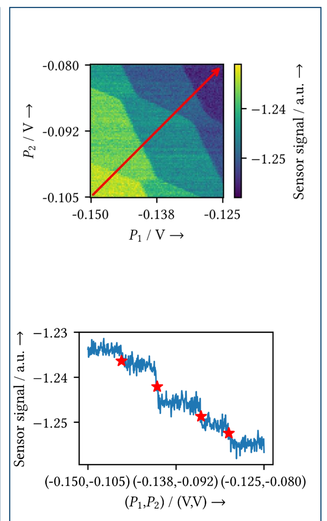
Refinement with Sensor Compensation

Sensor dot (SD) is disturbed by the voltages applied to the double quantum dot (DQD) gate electrodes

Effect can be mitigated by using virtual gates:
- Combination of several physical gates
- Effect of DQD gates on the SD is compensated
- SD signal shows stepwise characteristic
  - Reduces interpretation complexity



Uncompensated

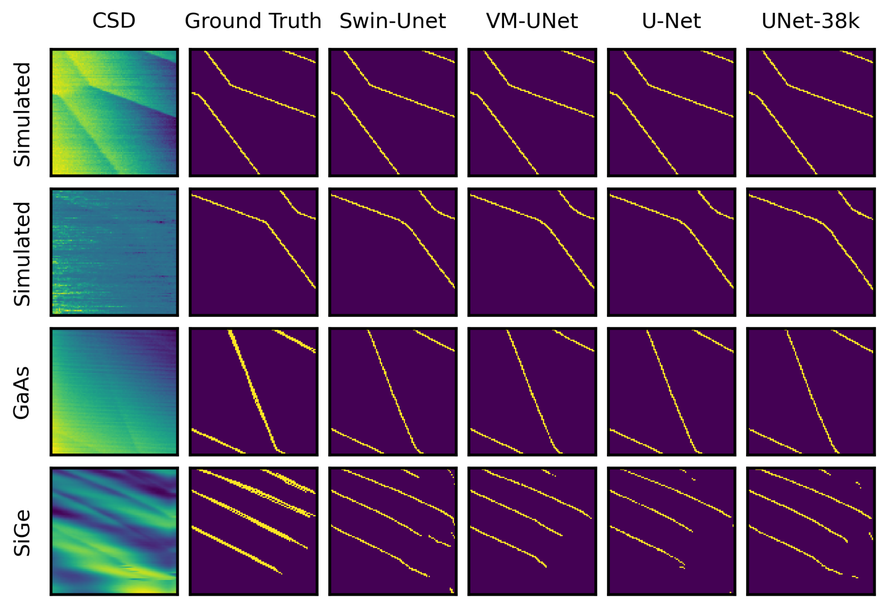


Compensated

Automated Charge Transition Detection

Investigated Approaches:
- Classical (gradient, phase-congruency, and mixed)
- Machine learning (convolution-, transformer-, state-space-model-, and diffusion-based)

CSD Data:
- Training: 10^6 simulated CSDs (SimCATS model [1])
- Validation: simulated + experimental CSDs [2]



Observations:
- Algorithms trained on simulated data can generalize to experimental data
- U-Net like architectures performed best
- Diffusion-based approaches too complex for hardware implementation
- Convolution based architectures are sufficient
- Tiny versions (e.g. UNet-38k) show competitive results

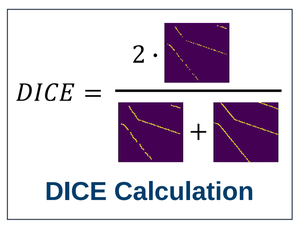
→Hardware integration requires further reduction

Results with Sensor Compensation

Dice Similarity Coefficient for evaluation: $\boldsymbol{DICE} = \frac{2|X \cap Y|}{|X|+|Y|}$

Surface Dice (S-DICE) allows deviation from exact segmentation

Target benchmark: S-DICE ≥ 0.95 on simulated data



DICE Calculation

Detector			S-DICE (threshold=2)	
Category	Name	Type	Contemporary* Data Quality	Superior* Data Quality
2D	Unet-38k	ML (CNN)	0.9944	0.9998
	Unet-4k	ML (CNN)	0.9884	0.9979
	Unet-447	ML (CNN)	0.9474	0.9884
	PhCon+GCanny	Classical	0.8673	0.9160
Ray-Based	Unet-1k-RB	ML (CNN)	0.8903	0.9926
	Unet-179-RB	ML (CNN)	0.8229	0.8971

* “Contemporary quality” denotes the distributions of distortions and sensor sensitivities extracted from the GaAs sample and applied in the simulations of [3]. “Superior quality” indicates that these distributions were restricted to the top 10% of the observed values

Energy Efficiency of Scaled ML Models

Required power for tuning procedure:

$$P_{tune} = \frac{N_{ops/csd} \cdot n_{csd}}{E_{unet} \cdot t_{tune}}$$

$E_{unet} = 50.62 \left[\frac{TOPS}{W}\right]$: U-Net accelerator efficiency [4]

$N_{ops/csd}$: number of operations per CSD inference

$n_{csd} = 10^7$ CSDs (or $6 \cdot 10^7$ ray-based measurements)

$t_{tune} = 6h$: time requirement of the tuning procedure

Detector	$N_{ops/csd}$	P_{tune} [W]
Unet-38k	$7.701 \cdot 10^7$	$7.043 \cdot 10^{-4}$
Unet-4k	$2.404 \cdot 10^7$	$2.199 \cdot 10^{-4}$
Unet-447	$4.471 \cdot 10^6$	$4.089 \cdot 10^{-5}$
Unet-1k-RB	$1.374 \cdot 10^7$	$7.855 \cdot 10^{-6}$
Unet-179-RB	$2.207 \cdot 10^6$	$1.262 \cdot 10^{-6}$

Outlook

Full charge state tuning

Precise assessment of **cryogenic limits**: heat, wiring, data transfer

→ Define the partition between cryo and room-temperature processing

→ Pursue **multi-purpose ML architectures** optimized via NAS/HPO

→ Build **hardware demonstrator** to evaluate performance

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[1] F. Hader et al., “Simulation of Charge Stability Diagrams for Automated Tuning Solutions (SimCATS),” in IEEE Transactions on Quantum Engineering, doi: 10.1109/TQE.2024.3445967
[2] Provided by the Quantum Technology Group of RWTH Aachen (www.quantuminfo.physik.rwth-aachen.de/cms/quantuminfo/forschung/~xwpl/quantum-technology-group)
[3] F. Hader et al., "Automated Charge Transition Detection in Quantum Dot Charge Stability Diagrams," in IEEE Transactions on Quantum Engineering, doi: 10.1109/TQE.2025.3596392
[4] T. Hui Teo et al., “U-Net Hardware Accelerator”. In: 2024 IEEE 17th International Symposium on Embedded Multicore/Manycore Systems-on-Chip (MCSoC), doi: 10.1109/MCSoC64144.2024.00063