Evaluation of cryogenic model libraries for FDSOI CMOS transistors

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***Abstract*— Scalable quantum computers demand innovative solutions to tackle the wiring bottleneck and control an increasing number of qubits. Cryogenic electronics based on CMOS technologies are promising candidates which can operate down to deep-cryogenic temperatures and act as a communication and control interface to the quantum layer. However, the performance of transistors used in these circuits is altered significantly when cooling from room temperature to cryogenic temperatures, which motivates accurate cryogenic modeling of transistors. In this paper, we report on a cryogenic simulation library tailored specifically to fully depleted silicon-on-insulator (FDSOI) transistors. We validated the accuracy of our preliminary model library by comparing simulations at both the device and circuit levels with experimental measurements from single transistors, ring oscillators, and a transimpedance amplifier. Our models effectively capture the DC behavior across the temperature range from $8\,\mathrm{K}$ to room temperature.**

***Index Terms*— Cryogenics, complementary metal-oxide-semiconductor (CMOS), fully-depleted silicon-on-insulator (FDSOI), integrated circuits, ring oscillators, semiconductor device modeling, and quantum computing.**

I. Introduction

REALIZING the full potential of quantum computers requires overcoming significant engineering challenges, particularly in the realm of qubit control and readout. One of the major hurdles is the wiring bottleneck, which arises as the number of qubits increases [1], [2].

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Cryogenic integrated circuits, which operate at extremely low temperatures, offer a promising solution to this wiring challenge by integrating control and readout electronics close to the quantum processor and operating them at cryogenic temperatures [3]–[8]. CMOS (Complementary Metal-Oxide-Semiconductor) technology, which is the backbone of modern electronic devices, shows great potential for adaptation to cryogenic environments [9]–[12].

Among various CMOS technologies, Fully Depleted Silicon-on-Insulator (FDSOI) stands out for its excellent electrostatic control and reduced short-channel effects, making it particularly suitable for cryogenic applications [13]–[18]. The main advantage of FDSOI transistors is their ability to adjust the threshold voltage using the back gate, which becomes especially critical at cryogenic temperatures. This tunability enables compensation for the threshold voltage increase caused by cryogenic temperature. Additionally, FDSOI transistors, which are built on an ultra-thin silicon layer atop a buried oxide layer, exhibit lower variability and enhanced performance at reduced voltages. This enables lowering the power consumption, which is a crucial factor to cope with the limited cooling power of a dilution refrigerator.

The transition from room temperature to cryogenic temperatures significantly alters the electrical characteristics of a transistor. Critical device parameters such as carrier mobility, threshold voltage, and subthreshold slope are significantly affected due to reduced thermal energy and changes in carrier scattering mechanisms [19], [20]. Consequently, existing foundry-based simulation libraries, which are typically characterized only down to $-40\,^{\circ}\mathrm{C}$, fail to accurately predict device performance at deep cryogenic temperatures. This discrepancy motivates the need for specialized cryogenic libraries that can accurately capture the physical phenomena occurring in the cryogenic regime.

Among the widely used modeling approaches, the Enz-Krummenacher-Vittoz (EKV) model [21], [22] requires the fewest parameters. It is a charge-based compact framework that is particularly suited for low-power and analog applications, offering strong performance in weak inversion regions. On the other hand, the BSIM family of models from UC Berkeley feature extensive parameterization to handle the complexities of advanced transistor technologies. These models accurately capture short-channel effects and performance in various operating conditions and require significant adaptation and retuning to account for cryogenic effects, such as

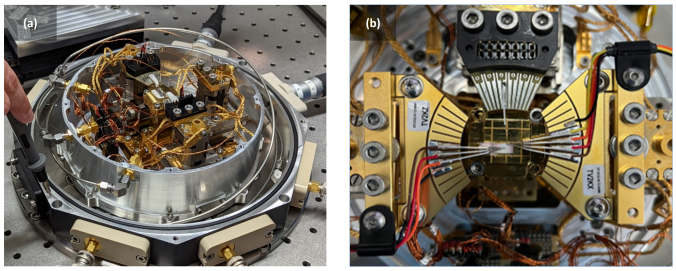

Fig. 1. (a) Cryogenic chamber and (b) a close-up of test chip with DC needle probes.

carrier freeze-out, mobility degradation, and threshold voltage shifts. Lastly, the L-UTSOI model developed by CEA-LETI [23], [24] is specifically designed for FDSOI technology and provides an optimal balance between computational efficiency and physical accuracy. It captures the unique characteristics of ultra-thin body and body-biasing effects, which are critical at low temperatures. The BSIM family and L-UTSOI are both recognized as the industry standard compact SPICE models by the Compact Model Coalition.

In this work, using the BSIM-IMG library, we develop a cryogenic simulation library for transistors based on a FDSOI process of GlobalFoundries. We rely on the BSIM-IMG library due to its compatibility with the foundry library as well as industry-standard EDA and simulation software, like Cadence Spectre. As a starting point, we performed DC characterization of several transistors from room temperature down to $8\,\mathrm{K}$, which is used as a calibration reference for the generation of the simulation library over the entire temperature range.

The developed library is used to simulate single-transistor devices and circuit blocks like ring oscillators and a transimpedance amplifier. The results of these simulations are compared against the measurement data at different temperatures to verify the accuracy of our transistor models. This work aims to provide a robust modeling framework that supports the design and accurate simulation of cryogenic electronic circuits. Such a framework is essential for the development of scalable quantum computing systems, where reliable and scalable control and readout electronics play a critical role.

II. Device Characterization

A. Experimental Setup

We used an attoDRY800 closed-cycle cryostat to cool down the test chips. The cryostat can achieve a minimum temperature of $5\,\mathrm{K}$. However, the base temperature can vary depending on the measurement configuration. Figure 1(a) and (b) show the system configuration for the measurement of single transistor devices using DC multi-contact needle probes. The probes are mounted onto piezo-positioners to access different areas of the test chip. In this particular configuration, a base temperature of $8\,\mathrm{K}$ is achieved. The test chips described in section V were wire bonded to a custom printed circuit board (PCB), and the measurements were also performed in the same cryogenic chamber.

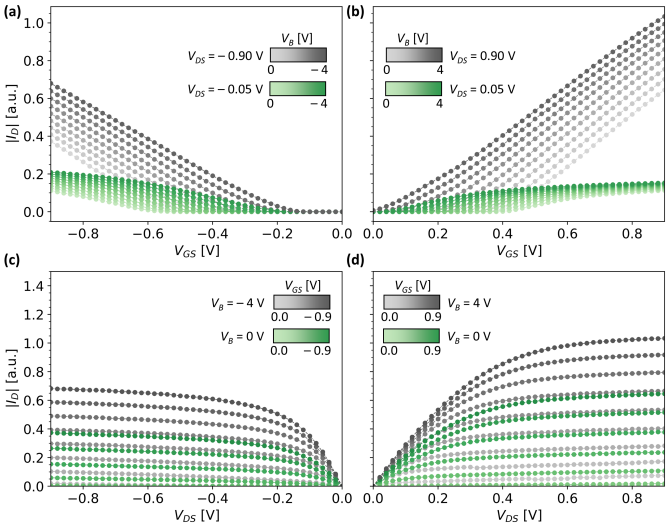

Fig. 2. Normalized transfer curves of (a) PMOS and (b) NMOS transistors at $|\boldsymbol{V_{DS}}| = 0.05\,\mathrm{V}$ (green curves) and $|\boldsymbol{V_{DS}}| = 0.90\,\mathrm{V}$ (gray curves), varying across different back-bias values ($\boldsymbol{V_B}$) in steps of $|0.5\,\mathrm{V}|$; normalized output curves of (c) PMOS and (d) NMOS transistors at $\boldsymbol{V_B} = 0\,\mathrm{V}$ (green curves) and $|\boldsymbol{V_B}| = 4\,\mathrm{V}$ (gray curves), varying across different front-gate biases ($\boldsymbol{V_{GS}}$) in steps of $|0.1\,\mathrm{V}|$ Measurements are recorded at $8\,\mathrm{K}$ for all the sub-plots.

B. I-V Measurements

The test chip, which is comprised of transistor arrays, was produced by GlobalFoundries. Initially, our investigations concentrated on the SLVT (Super-low threshold voltage) variant of the transistors. We carried out comprehensive DC characterization on transistors of various sizes, spanning from room temperature down to $8\,\mathrm{K}$.

We measured the current-voltage (IV) characteristics of each device under a range of bias conditions at different temperature stages, using the Keysight B1500 Parameter Analyzer. For illustration, Figure 2 presents examples of these measurements at $8\,\mathrm{K}$ for both NMOS and PMOS transistors of identical dimensions.

The impact of the applied back-bias (V_B) on these transistors is clearly visible in the transfer curves shown in Figure 2(a) and (b). These curves reveal a shift in the threshold voltage towards lower values, which is observed for both linear ($|V_{DS}| = 0.05\,\mathrm{V}$) and saturation modes ($|V_{DS}| = 0.90\,\mathrm{V}$) of the transistors shown by the green and gray sets of curves. These measurements were repeated for multiple devices of different device dimensions across temperatures ranging from $8\,\mathrm{K}$ to $300\,\mathrm{K}$.

III. Modeling Approach

We developed a simulation library based on DC measurements to cover the temperature range from room temperature down to a few Kelvin. For the modeling process, we utilized the BSIM-IMG 102-9.6 model [25], which includes a built-in cryogenic extension. This model was selected for its ability to accurately capture the physical phenomena in FDSOI transistors at low temperatures. We calibrated the model parameters using the measured data to ensure that the

simulated behavior aligned with the observed characteristics across the temperature range.

A. SPICE models for cryogenic applications

Simulation models for bulk or SOI devices have traditionally supported temperatures down to $-55\,^{\circ}\mathrm{C}$ (218 K). For applications such as cooled amplifiers or infrared detectors, specialized models were developed to accommodate even lower temperatures, 4 K for helium-cooled and 77 K for nitrogen-cooled circuits. Since these circuits are only operated at a fixed temperature, it is sufficient to create the models without temperature effects and also to set the extraction and simulation temperature to $25\,^{\circ}\mathrm{C}$ although the measurements were carried out at a low temperature. This approach avoids numerical problems in the models if the correct temperature would be set.

Two standard models certified by the Compact Model Coalition have already been available for transistors manufactured in the 22nm FDSOI process: BSIM-IMG 102.9.4 [25] from UC Berkeley and L-UTSOI 102.5 [23], [24] from CEA-LETI. However, both models failed to converge at temperatures below approximately 40 K. More recently, the updated versions BSIM-IMG 102.9.6 and L-UTSOI 102.7 [26] have been released with cryogenic extensions that enable reliable simulation across the targeted temperature range.

The cryogenic extension in the case of the BSIM-IMG model avoids numerically unstable states when the transistor temperature approaches absolute zero. This can be seen particularly well in the calculation of the temperature voltage (Vtm), which approaches 0 as the temperature falls. This can lead to floating-point exceptions in those parts of the model code that use the fundamental expression:

$$\lim_{T\to 0}\left(\frac{k_B T}{q}\right) = 0 \tag{1}$$

To avoid this situation, BSIM-IMG 102.9.6 introduces an effective temperature ($Tempeff$) for the cryogenic extension, which specifies a lower limit for the device temperature, and this avoids the aforementioned numerical problems.

The two subplots shown in Figure 3 have been generated using the Verilog-A code of the BSIM-IMG 102.9.6 model. They show the effective temperature for BSIM-IMG 102.9.6 with CRYOMOD model selector set to 0 (standard operation with classical temperature model) and CRYOMOD = 2 with the special extension for cryogenic applications. Below is the derived temperature voltage Vtm for both cases. Both variables go into a saturated state at a temperature of approximately 50 K.

In this paper, the parameter extractions have been performed for the BSIM-IMG model, which serves as the foundation for the existing foundry library.

B. Model parameter extraction and simulation library

Figure 4 shows an overview of the general development flow of the simulation library, organized into four main steps. The first step involves expanding the existing foundry library (based on BSIM-IMG 102.9.4) to include the additional

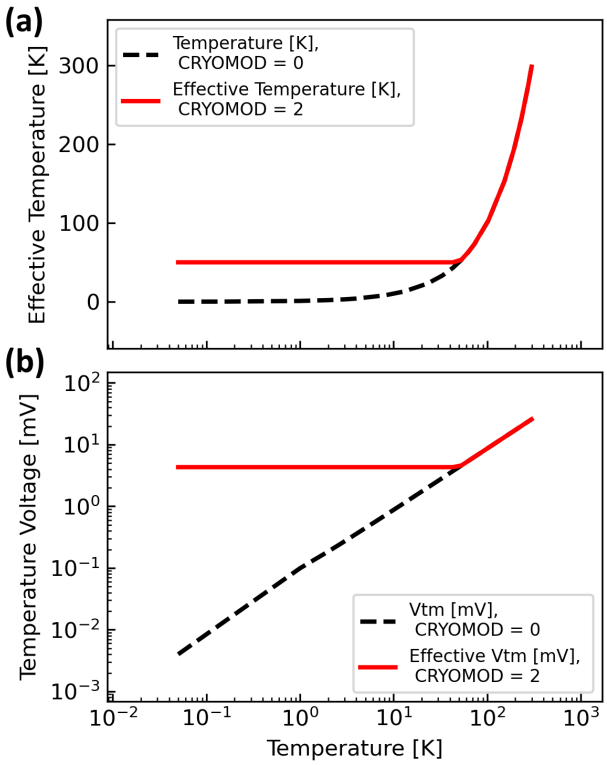

Fig. 3. Calculation of (a) effective temperature and (b) resulting temperature voltage for CRYOMOD=0 and 2

cryogenic extension parameters from the BSIM-IMG 102.9.6 model. Following this, a modifiable adjustment parameter is introduced for each of the model parameters, as shown in the following example:

$$\mathrm{UA1} = 0.00 + \mathrm{UA1}_{\mathrm{adjust}} \tag{2a}$$
$$\mathrm{UC} = -0.027 + \mathrm{UC}_{\mathrm{adjust}} \tag{2b}$$

$$\mathrm{TLOW} = 50.0 + \mathrm{TLOW}_{\mathrm{adjust}} \tag{3a}$$
$$\mathrm{KT11} = 0.01 + \mathrm{KT11}_{\mathrm{adjust}} \tag{3b}$$

where Equations 2 correspond to the parameters in the existing foundry library, while Equations 3 account for the cryogenic extension parameters. In this fashion, all the remaining model parameters are also redefined with the adjustment parameters, resulting in an updated version of the existing foundry library, hereby defined as our *cryogenic library*.

In the second step, simulations are performed for various device geometries using the existing foundry library. An initial parameter extraction is carried out to capture the effective model parameters across all measured temperature points. These parameters are compiled into a new file, referred to as the *slim library* file, including a compact model to adapt the simulation to the measured curves. This file contains both geometry-independent parameters as well as the parameters that vary with the width (W) and/or gate length (L), along with the adjustment parameters to be tuned in the next step.

The *slim library* file is then loaded into the simulator along with the measured data corresponding to each temperature point. At this stage, the adjustment parameters are iteratively

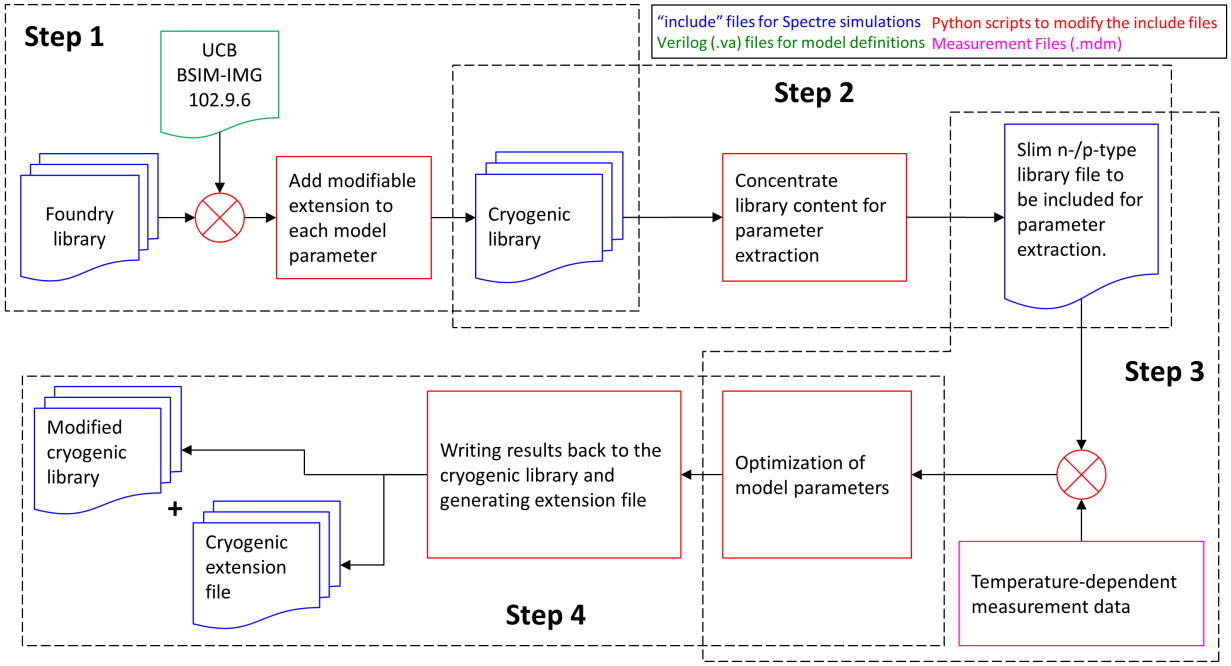

Fig. 4. Flowchart depicting the development of cryogenic simulation libraries. The blocks are color-coded according to the type of files indicated in the legend.

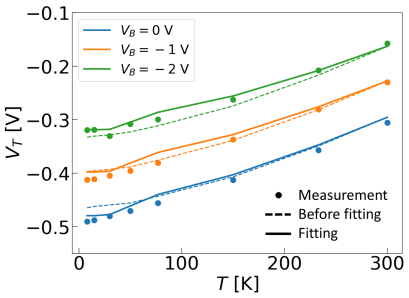

Fig. 5. Calibration of V_T values using measurement data of a short-channel PMOS transistor.

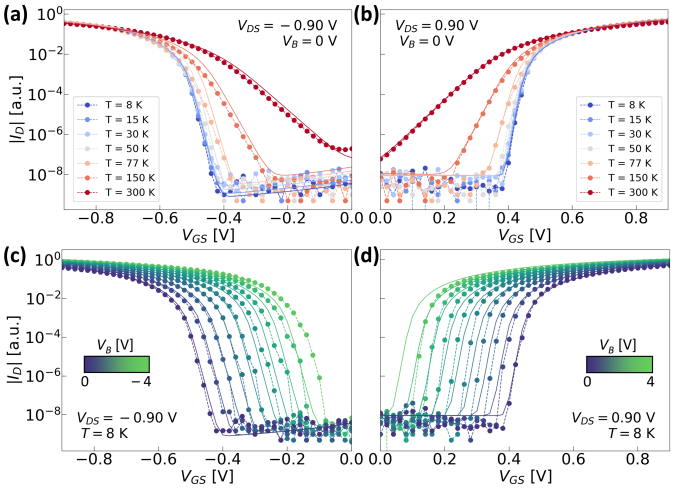

Fig. 6. Measured (symbols) and simulated (lines) transfer curves at different temperatures for short-channel (a) PMOS and (b) NMOS transistor; measured and simulated transfer curves at $8\,\mathrm{K}$ for different back-bias voltages in steps of $|0.5\,\mathrm{V}|$ (c) PMOS and (d) NMOS transistor. The curves in all the sub-figures are normalized to the corresponding maximum values.

optimized to minimize the relative error between simulated and measured data across all temperatures. In the first step of the optimization procedure, the existing temperature parameters like UTE for the basic mobility behavior are re-adjusted to the extended temperature range down to a few Kelvin. Subsequently, only a few specific model parameters for the cryogenic extension, like the threshold voltage parameters KT11, the mobility coefficient UA2, or the velocity saturation parameter AT2, and in the case of the p-type transistor, the transition parameter TLOW and the coefficient for smoothening function TMEXP2 were taken to adjust the simulations to the experimental data. Table I lists the parameters that were chosen for the optimization. As an example, we show the adjustment of the threshold voltage (V_T) versus temperature at different back bias values in Figure 5, which includes both the measurement points as well as the fitting curves. The curves before fitting (simulated with the existing foundry library), the parameters to the measurement data are shown as dashed lines, and the curves after optimization (simulated with *cryogenic library*) are shown as solid lines.

As a final step, after the whole extraction process, the results are written back to the cryogenic library and a separate cryogenic extension file. These files with optimized parameters can be directly loaded into an EDA software for simulations across a broad temperature range of a few K to $298\,\mathrm{K}$. The cryogenic library was also verified against the original library, and it shows identical behavior at room temperature.

IV. Device-level Validation

TABLE I
MODEL PARAMETERS GROUPED BY TEMPERATURE DEPENDENCE

A. Non-cryogenic temperature parameters					
Name	**Description**	**P0**	**W**	**L**	**W×L**
KT1L	Vth temperature coefficient	x			
KT2	Vth temperature coefficient	x			
UTE	Mobility temperature coefficient	x	x	x	x
UTL	Mobility temperature coefficient	x			
UA1	Mobility temperature coefficient for UA	x	x		
UC1	Mobility temperature coefficient for UC	x			
PRT	Series resistance temperature coefficient	x			
AT	Saturation velocity temperature coefficient 1	x			x
ATL	Length scaling parameter for AT	x			
PTWGT	PTWG temperature coefficient	x		x	
B. Model parameters for cryogenic extension (CRYOMOD = 2)					
Name	**Description**	**P0**	**W**	**L**	**W×L**
CRYOMOD	Cryogenic model selector; 2 = turn on cryogenic model and merge smoothly to CRYOMOD = 0 for T more than 210 K				
KT11	Vth temperature coefficient	x			
UA2	Mobility temperature coefficient for UA	x			
TLOW	Transition temperature of SS at low temperatures	x			
TMEXP2	Temperature coefficient for Vdseff smoothing	x			
AT2	Saturation velocity temperature coefficient	x			

A. I-V Curves

Using the *cryogenic library*, we simulated the transfer curves of short-channel PMOS and NMOS transistors with identical dimensions at the measured temperature points. The temperature dependence of the measured (symbols) and simulated (lines) transfer curves is shown in Figure 6(a) and (b) for the PMOS and NMOS transistors, respectively, at $V_B = 0\,\mathrm{V}$ and $|V_{DS}| = 0.90\,\mathrm{V}$.

The results indicate that the *cryogenic library* has a good match to the measurements at room temperature for both PMOS and NMOS transistors. However, at cryogenic temperatures, the model has a larger deviation from the measurement points as compared to room temperature. This is also observed in the back-bias dependent transfer curves at $8\,\mathrm{K}$ as shown in Figure 6(c) and (d), where the model deviates further from the measurement at much higher $|V_B|$ values, especially in the weak inversion or the sub-threshold regime.

B. Threshold Voltage

From the measured transfer curves, we use the threshold voltage as an initial parameter to quantitatively estimate the accuracy of our model. For all the measured and simulated curves shown in Figure 6, the threshold voltage values were extracted using the constant current method [27]. Critical current values of $100\,\mathrm{nA}$ and $300\,\mathrm{nA}$ were used for the PMOS and NMOS transistors, respectively. Figure 7(a) shows the extracted threshold voltage values of the curves in Figure 6(a) and (b) plotted together against temperature.

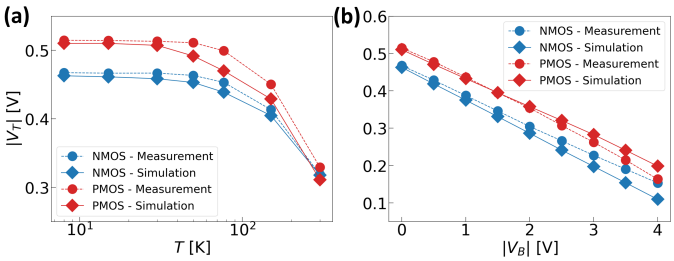

Fig. 7. Measured and simulated values of threshold voltage plotted against (a) temperature at $\boldsymbol{V_B} = 0\,\mathrm{V}$ and (b) back-bias at $\boldsymbol{T} = 8\,\mathrm{K}$.

For both PMOS and NMOS transistors, the values increase with decreasing temperature and start to saturate towards lower temperatures around $30\,\mathrm{K}$, which is also in agreement with previous reports on bulk [20], [28] and FDSOI [29] transistors. Using the extracted V_T values from the measurement and simulations, we calculated the mean average percentage error (MAPE) between measured and simulated V_T values for the PMOS and NMOS transistors to be around 3% and 2%, respectively, over the entire temperature range. However, on considering the V_T values for different back-bias conditions at $8\,\mathrm{K}$ as plotted in Figure 7(b), the MAPE in V_T for PMOS and NMOS devices was extracted to be around 15% and 5% respectively, indicating that the model deviation is much higher for PMOS devices at $8\,\mathrm{K}$. Nevertheless, for $|V_B| < 1.5\,\mathrm{V}$ the model fits well with the measured data for both PMOS and NMOS transistors.

V. CIRCUIT-LEVEL VALIDATION

We further expanded our investigation on the accuracy of our cryogenic models using two distinct test chips. The first test chip, featuring a series of ring oscillators, was designed by Racyics GmbH, while the second, developed at ICA (PGI-4), includes a transimpedance amplifier. Both test chips were produced by GlobalFoundries and the specific circuit blocks we focused on within these chips were designed using the SLVT variants of the transistors as discussed previously.

A. ABB Ring Oscillators

In cryogenic temperatures, a major target is to significantly reduce the power consumption of digital standard cell logic. But, high performance is still required. Biasing the back-gate of the transistors is a promising technique to speed up digital circuits powered with ultra-low supply voltage (ULV). An investigation of digital standard cell logic performance in cryogenic conditions with an Advanced Body-Biasing (ABB) regulation scheme [30] can be evaluated with the test chip. The resulting measurements are compared to the simulation with the developed cryogenic transistor library.

The test chip contains PVT performance monitors of the SLVT transistor flavor with a gate-length of $28\,\mathrm{nm}$. A single PVT monitor instance consists of ring oscillators with NAND3 and NOR3 standard cell logic gates. Multiple instances of

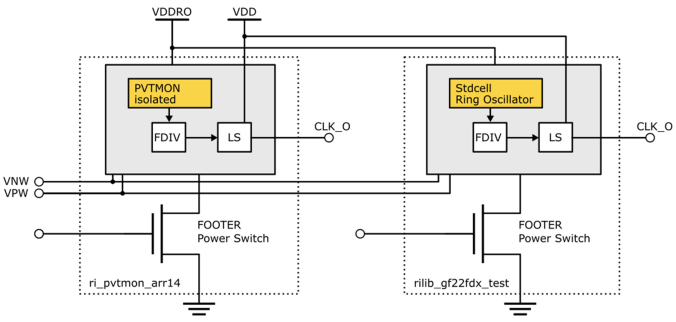

Fig. 8. ABB PVT monitor and standard cell ring oscillator test structure.

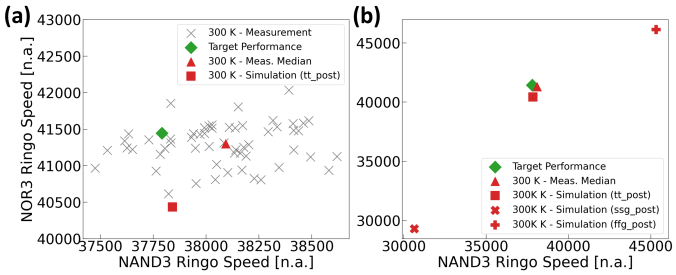

Fig. 9. PVT monitor (a) measurement and (b) simulation values at ZBB $0.80\,\mathrm{V}$ at $300\,\mathrm{K}$.

them are instantiated to measure the local performance deviation on silicon. Based on the room temperature target performance of the PVT monitor ring oscillators at Zero-Body-Bias (ZBB) and $0.80\,\mathrm{V}$ supply voltage, in room and cryogenic temperatures, and lower supply voltages, the PVT monitors are moved to their target performance. Hence, in each PVT operation condition the back-bias voltages V_{NW} and V_{PW} are adapted in forward body-bias direction (FBB) from ZBB to $V_{NW} = -V_{PW} = 4.0\,\mathrm{V}$ based on the ABB scheme [30]. The adapted back-bias voltages are applied to a test ring oscillator consisting of standard cell logic gates of a specific cell type (e.g. INV), VT-flavor, and gate-length (e.g. SLVT $28\,\mathrm{nm}$). Measurement results of the ring oscillator speed, leakage, and dynamic current consumption are compared to simulation values. The schematic of the ABB ring oscillator measurement is visualized in Figure 8.

The ABB target performances of PVT monitor ring oscillators NAND3 and NOR3 are depicted in Figure 9. At room temperature, the median of the NMOS-sensitive ring oscillator built up of NAND3 standard cell logic gates is 1% slower than the TT (typical-typical) process model. The median of the PMOS-sensitive NOR3 ring oscillator measurement is around 2.5% faster than the TT process model. At cryogenic temperature, the PVT monitor NAND3 ring oscillator is faster by 15% and the NOR3 ring oscillator has a speed-up by 20% compared to the room temperature measurements. In Figure 10, the developed cryogenic model also shows a speed-up of the ring oscillator performance from room temperature to cryogenic temperature. This speed-up has been simulated for schematic and extracted netlists, and is about 8% greater than the measurements show.

The standard cell ring oscillator performance, leakage, and dynamic current consumption in the ABB corners are depicted

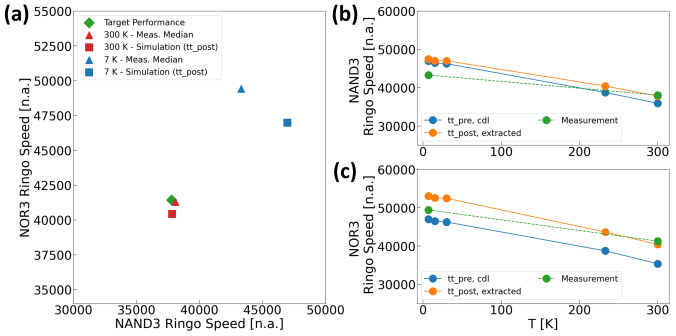

Fig. 10. (a) PVT monitor measurement and simulation values at ZBB $0.80\,\mathrm{V}$ at $7\,\mathrm{K}$; Comparison of schematic and extracted netlist simulation of (b) NAND3 and (c) NOR3 ring oscillators with the cryogenic transistor models.

in Figure 11(a)-(c), respectively. The ABB calibration has been executed on silicon and virtually, with the transistor models extended to the cryogenic temperature range. Due to ABB, the process mismatch between the model and silicon seen in the ZBB PVT monitor measurement is canceled out. Therefore, the performance measurements in Figure 11(a) show only a deviation of less than 0.5% down to a supply voltage of $0.40\,\mathrm{V}$ between model and silicon. For lower supply voltages ($V_{DD} < 0.50\,\mathrm{V}$), the back-bias voltages are close to their limits of $V_{NW} = -V_{PW} = 4.0\,\mathrm{V}$. Since the ABB simulations with the cryogenic model show a higher back-bias sensitivity than on silicon measured, for $V_{DD} < 0.50\,\mathrm{V}$ the back-bias voltages are at their limits and slow down the ring oscillator in the simulation. On silicon, an over-compensation of the ring oscillator performance can be observed since the back-bias voltages are in between their limits, especially for lower supply voltages of V_{DD}. In Figure 11(b), the leakage current rises exponentially with lower V_{DD} because the ring oscillator is more biased into the forward direction. The cryogenic model shows a very low leakage independent of the back-gate voltage and supply voltage for $V_{DD} > 0.45\,\mathrm{V}$. Then, the leakage rises rapidly due to the back-bias voltages close to their voltage range limits. The dynamic current consumption of the test ring oscillator in Figure 11(c) shows a minimum around $0.55\,\mathrm{V}$ at room temperature. In cryogenic temperatures, the dynamic current consumption decreases with lower V_{DD} for the developed model as well as the measurements.

At ZBB $0.80\,\mathrm{V}$, the developed cryogenic model shows a speed-up of NAND3 and NOR3 ring oscillator performances from room temperature to cryogenic temperature, which is also observed in the measurements. With the removed process offset between silicon and model by ABB in between the back-bias voltage range limits, the cryogenic model can fairly represent the ABB ring oscillator measurements.

B. Transimpedance Amplifier

We tested the performance of the developed models further by simulating a transimpedance amplifier (TIA). The TIA comprises of a two-stage operational amplifier with adjustable gain as shown in Figure 12(a). In order to implement gain control, the feedback loop comprises of 15 resistors ($200\,\mathrm{k\Omega}$), which can be shorted with a standard transmission gate.

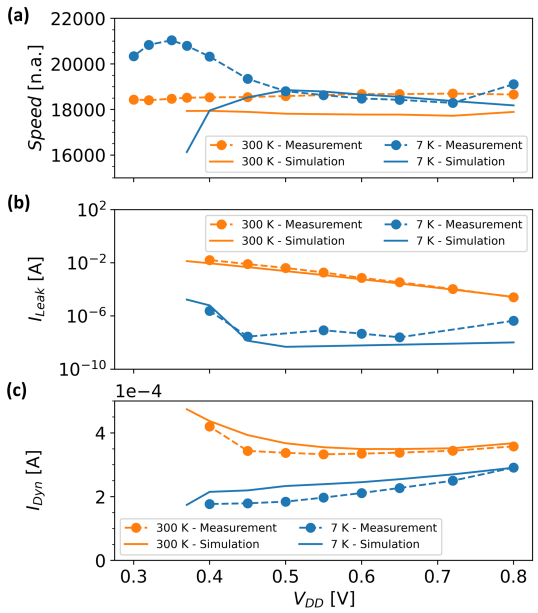

Fig. 11. Exemplary standard cell ring oscillator measurement of SLVT28 INVX040 and comparison to simulation results for ring oscillator (a) speed, (b) leakage current, and (c) dynamic current consumption.

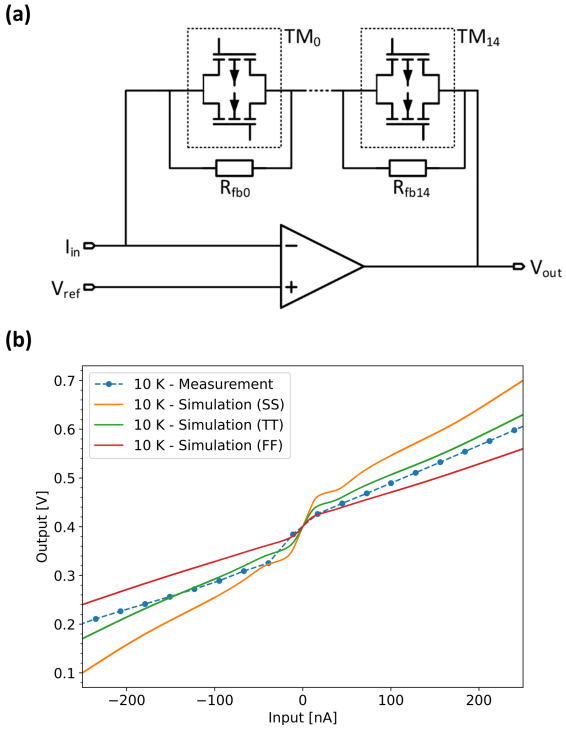

Fig. 12. (a) Schematic and (b) output characteristic of the transimpedance amplifier.

Simulation at the minimum valid temperature using the standard library at $-40\,^{\circ}\mathrm{C}$ demonstrates an expected highly linear output characteristic. Initial measurements at $10\,\mathrm{K}$ reveal a kink in the output characteristic of the TIA for currents approaching $0\,\mathrm{A}$ as seen in Figure 12(b).

We simulated the amplifier using our cryogenic library, which yielded results that align closely with the observed measurement at $10\,\mathrm{K}$. The simulation setup comprises the foundry's standard library, with the substitution of the standard p- and n-channel transistors with our cryogenic models. Cadence Spectre AMS Designer was employed as a simulator, with the ambient temperature set to $-40\,^{\circ}\mathrm{C}$, to circumvent potential invalid behavior of feedback resistors, since cryogenic models are unavailable for them. The temperature of the transistors is set to $-266\,^{\circ}\mathrm{C}$ within a configuration cell-view. The simulation is performed with two worst-case corners, i.e slow-slow (SS) and fast-fast (FF).

The measured output characteristic is found to be within the simulated worst-case corners, which demonstrates the correctness of the cryogenic simulation. Moreover, the kink inside the output characteristic can be investigated by setting the temperature of individual sets of transistors to room temperature. In this case, the kink is caused by an increase in the threshold of the transistors inside the transmission gates. For values around $V_{DD}/2$, neither the n-channel nor the p-channel transistor is fully conducting, increasing the resistance of the feedback network around this value. A more detailed analysis of the amplifier with further measurements and simulations is yet to be done and is not available at the moment, and is beyond the scope of this work.

VI. Conclusion

In summary, we have addressed the critical need for accurate transistor modeling in cryogenic environments, which is essential for the advancement of scalable quantum computing systems. We developed a cryogenic simulation library specifically for a FDSOI technology, compatible with industry-standard EDA tools such as Cadence Spectre. This library was calibrated using DC characterization data collected from room temperature down to $8\,\mathrm{K}$, ensuring its reliability across a broad temperature range.

Our simulations of single transistor devices and circuit blocks, including ring oscillators and a transimpedance amplifier, demonstrated a reasonable agreement with experimental measurements from room temperature down to $8\,\mathrm{K}$. While the model is not production-ready, it successfully captures key trends and provides a reliable basis for the design and simulation of cryogenic integrated circuits. These results show a significant step towards the development of cryogenic electronics for scalable quantum computers.

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