Fault-Tolerant Stabilizer Measurements in Surface Codes with Three-Qubit Gates

Josias Old,[1,2,*] Stephan Tasler,[3,†] Michael J. Hartmann,[3] and Markus Müller[1,2]
[1]Institute for Theoretical Nanoelectronics (PGI-2), Forschungszentrum Jülich, Jülich, Germany
[2]Institute for Quantum Information, RWTH Aachen University, Aachen, Germany
[3]Physics Department, Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany

(Received 9 July 2025; revised 16 October 2025; accepted 13 November 2025; published 9 December 2025)

Stabilizer quantum error correction (QEC) codes, in particular topological surface codes, are prime candidates to enable practical quantum computing. While it is widely believed that strictly fault-tolerant protocols can only be implemented using single- and two-qubit gates, several quantum computing platforms, including trapped ions, neutral atoms, and superconducting qubits, support native multi-qubit operations. In this Letter, we show that stabilizer measurement circuits for unrotated surface codes can be fault tolerant using single auxiliary qubits and *three-qubit* gates. These gates enable lower-depth circuits with fewer fault locations and potentially shorter QEC cycle times. We find that in an optimistic parameter regime where fidelities of three-qubit gates are the same as those of two-qubit gates, the logical error rate can be up to one order of magnitude lower and the threshold significantly higher, increasing from $\approx 0.63\%$ to $\approx 0.83\%$. Our results, applicable to a wide range of platforms, motivate further investigation into multi-qubit gates for fault-tolerant QEC as they can offer substantial time and physical qubit resource advantages to reach a given target logical error rate.

DOI: 10.1103/sblg-fbq4

Introduction—Quantum error correction (QEC) is crucial to enable fault-tolerant quantum computation [1,2]. For the widely used *stabilizer codes* repeatedly measuring a generating set of commuting *stabilizer operators* reveals information on errors that occurred, forming the error syndrome. While a stabilizer code with *distance* d can in principle correct for arbitrary weight-$t = \lfloor (d-1)/2 \rfloor$ errors, implementing the stabilizer measurements with a noisy quantum circuit can reduce the number of correctable errors. Quantum gates or measurements that underlie the error syndrome measurement circuits can be faulty, leading to a wrong diagnosis of the error. Additionally, errors on auxiliary qubits can propagate into higher-weight data qubit errors (also called *hook* errors), effectively reducing the distance.

Circuits where the distance of the underlying code is preserved are deemed fault tolerant (FT). Traditionally, see, e.g., Ref. [3], an error correction subroutine (or gadget) is called fault tolerant if the *weight* of the output error is bounded by the sum of the weight of the incoming error and the number of faults occurring during the protocol. This turns (almost) any stabilizer readout with single, physical auxiliary qubits non fault-tolerant. There are numerous approaches to tackle these challenges, including *Shor*, *Steane,* and *Knill error correction* [1,4,5]. These methods rely on (fault-tolerantly) encoded auxiliary qubits to transversally read out the syndrome information using only single- and two-qubit gates. These approaches, as well as more recent flag-qubit-based constructions [6–8] use carefully crafted quantum circuits to prevent malicious error propagation. There exist relaxed definitions of fault tolerance that include errors of weight $w > t$ that can still be corrected [9]. Using these, it is known that *any* stabilizer measurement circuit using two-qubit gates in the unrotated surface code is fault tolerant [10]. The more qubit-efficient rotated surface codes, however, require a specific ordering of two-qubit gates to retain fault tolerance [11].

To date, QEC cycles on rotated surface codes have been realized in trapped ions [12] and superconducting architectures [13–15]. Recently, distance-5 and 7 codes have been operated below the threshold, where the error rate of the logical qubit decreases with increasing code distance [16]. Logical operations have been realized in error-detecting surface codes in superconducting architectures [17,18], with trapped ions [19], and error-corrected entangling gates with neutral atoms [20].

These experimental QEC demonstrations use elementary gate sets consisting of single- and two-qubit gates. Most architectures, however, also allow for native implementation of multi-qubit gates, e.g., using Rydberg blockade in neutral atoms [21,22], multi-qubit Mølmer-Sørensen gates

*Contact author: j.old@fz-juelich.de
†Contact author: stephan.tasler@fau.de

in trapped ions [23], or optimized gate sequences for the control Hamiltonians of solid-state-based platforms [24,25]—according to common belief that these would result in non-FT circuits. Recently, multi-qubit gates have been proposed for surface code QEC in semiconductor spin qubits [26], superconducting qubits [27–29], and neutral atoms [30]. While these references all use different noise models, they find that higher thresholds can be achieved in certain parameter regimes, but at the expense of losing strict fault tolerance.

In this Letter, we report on and explore the unexpected finding that stabilizer measurement circuits for unrotated surface codes using three-qubit gates can be fault tolerant, even when considering three-qubit depolarizing noise channels on these gates. We use single physical auxiliary qubits, repeatedly measuring stabilizers to gain confidence in measurement outcomes, and carefully design readout circuits to prevent malicious error propagation. We first recover standard results for surface-code syndrome readout circuits and then show how circuits using three-qubit CZZ gates are fault tolerant, based on distinguishability of all circuit faults up to order t in the unrotated surface code. We finally show comparative numerical studies that support the theoretical findings—the logical error rates of memory experiments scale $\propto p^{t+1}$ in the regime of low physical error rates. We also find that, with optimistic assumptions on the noise strength, the parallel three-qubit CZZ-gate-based scheme outperforms sequential application of two-qubit CZ gates in terms of logical error rate. In particular, the threshold increases from $\approx 0.63\%$ to $\approx 0.83\%$. These results can have practical significant impact for surface-code-based QEC with ions, neutral atoms, and solid-state platforms, lowering time and space resource requirements.

Quantum error correction and surface codes—In stabilizer error correction, the $+1$ eigenstates of $n-k$ commuting Pauli operators span the 2^k-dimensional logical subspace of an n-(physical) qubit Hilbert space [31]. These operators generate the stabilizer group $\mathcal{S} = \{\langle S_i \rangle_{i=1}^{n-k}, [S_i, S_j] = 0 \ \forall \ i \neq j, \mathbf{1} \notin \mathcal{S}\}$. Nontrivial Pauli operators on the codespace are all Pauli operators that commute with the stabilizers, but are not stabilizers themselves, i.e., elements of the normalizer $\mathcal{N}_{\mathcal{P}}(\mathcal{S})$. The minimum weight of any such element is the code *distance* d and measures the performance of the code: a distance-d QEC code can correct for arbitrary weight-t with $t = \lfloor (d-1)/2 \rfloor$ errors. The *parameters* of a QEC codes are then the triple $[[n, k, d]]$.

If a Pauli error $E \in \mathcal{P}^{\otimes n}$ occurs on the qubits, the outcomes of a projective measurement of a generating set of the stabilizer using auxiliary qubits yields its *syndrome* $\mathbf{s}(E) = (\langle S_i, E \rangle)_{i=1}^{n-k}$, which is decoded to correct for the error. Here, we denote by $\langle P, P' \rangle$ whether Pauli operators P and P' commute (0) or anticommute (1).

One prominent family of stabilizer codes are topological surface codes [32]. For a distance-d surface code, data qubits are placed on the edges of a $d \times d$ square lattice. Stabilizer generators are defined on plaquettes fixing the Z parity of qubits on adjacent edges and on vertices fixing the X parity of qubits on emanating edges. The resulting surface code has parameters $[[d^2 + (d-1)^2, 1, d]]$. Additionally, one can cut the $(d-1)^2$ corner qubits to get the rotated surface code with parameters $[[d^2, 1, d]]$ [33,34], without reduction of the code distance.

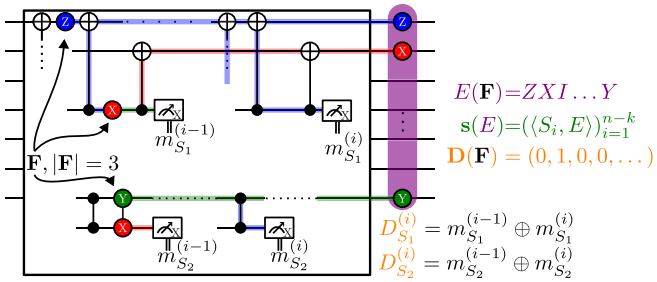

FIG. 1. Objects used to determine distinguishability of a fault set. The box represents some (Clifford) circuit with measurements. It is encoded in an error-correcting code with stabilizer generators $\{S_i\}_{i=1}^{n-k}$. During the circuit, sets of deterministic measurements specify the detectors $\{D\}$. For an error correction gadget, these are typically the parities of consecutive stabilizer measurements. The exemplarily shown fault path $\mathbf{F}$ of weight $w = 3$ can be efficiently propagated using Clifford simulation. This results in a vector of flipped detectors D and a final error E. The ideal syndrome of E is $s(E) = (\langle S_i, E \rangle)_{i=1}^{n-k}$.

Fault tolerance of surface code syndrome measurement circuits—Loosely speaking, a circuit implementing an error correction gadget using a QEC code with distance d is fault tolerant if it takes at least d distinct elementary [i.e., $\mathcal{O}(p)$] faults to cause an undetected logical error. If the smallest fault leading to an undetectable logical error has order $2w+1$, then every order $2w$ fault is detectable and every order w fault has a distinct syndrome and is therefore correctable. The latter property is called *distinguishability* in Ref. [9] and is a key property to extending the fault tolerance definition of Ref. [35] to incorporate surface code syndrome readout circuits. In Fig. 1, we summarize the objects that we use to determine distinguishability of fault sets: if any pair of fault paths $\mathbf{F}_i, \mathbf{F}_j$ in a fault set $\mathcal{F}^{(w)}$ either results in errors with different syndromes, stabilizer equivalent errors, or different detector flips during the protocol, then the fault set $\mathcal{F}^{(w)}$ is distinguishable. A more technical exposition of this approach is outlined in the End Matter.

First, we recall stabilizer measurement circuit constructions for rotated and unrotated surface codes using single- and two-qubit gates and explain how they fit the fault tolerance definitions. In the rotated surface codes, the order of CZs determines whether the fault set $\mathcal{F}^{(t)}$ is distinguishable or not. If X faults, e.g., on the auxiliary qubit (*hook error*) of a Z-stabilizer measurement propagate to weight 2 Z errors parallel to the Z-logical operator, the circuit is not fault tolerant because it only requires $\lceil d/2 \rceil$ of such faults

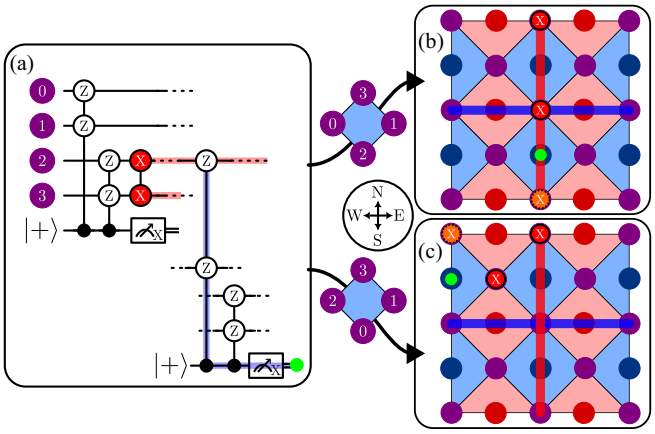

FIG. 2. Detail of stabilizer measurement circuits for the distance-3 unrotated surface code, implemented with three-qubit CZZ gates as described in the main text. (a) For a uniform depolarizing noise model, there exist elementary two-qubit X faults on the support of Z-stabilizer generators—contrary to the two-qubit gate situation. These faults are captured by a subsequent Z-stabilizer measurement. (b),(c) Show the effect for two different orderings of the gates. In the unrotated surface codes, we draw the X-(Z-)logical operators as thick red (blue) lines and draw flipped detectors with a light green dot. (b) If the last three-qubit gates act on the horizontal (WE) and vertical (NS) qubits, the final X error is parallel to the X-logical operator. We draw another first-order fault (orange, dotted) with the same syndrome, which is logically inequivalent, implying a nondistinguishable fault set $\mathcal{F}^{(1)}$. (c) For a diagonal ordering toward the south-east (SE) and north-west (NW) qubits, however, faults of the same order with the same flipped detectors are stabilizer equivalent. The fault set $\mathcal{F}^{(1)}$ is distinguishable.

to completely cover the logical operator. Therefore, fault paths of weight $\lceil d/2 \rceil - 1$ are detectable, and the largest distinguishable fault set is $\mathcal{F}^{(\lfloor (d-1)/4 \rfloor)}$. If, however, hook errors propagate to qubits orthogonal to the logical operator (cf. Ref. [11]), the static distance is preserved in the sense that fault paths in $\mathcal{F}^{(t)}$ are distinguishable—see Fig. 5 in the End Matter for exemplary faults.

For the unrotated surface code, as noted in Ref. [32] hook errors are less damaging than naively expected. This is because unrotated surface codes can be constructed as hypergraph product codes of two (classical) repetition codes [36]. For any hypergraph product code, any order of two-qubit entangling gates gives a distance preserving stabilizer measurement circuit [10]. This is equivalent to $\mathcal{F}^{(t)}$ being distinguishable. The fundamental reason for that is that every stabilizer generator (of Pauli P) overlaps with any minimum-weight logical operator (of Pauli P) on at most a single qubit, as can be seen in Fig. 2(b).

Since during the measurement of a Pauli P-type stabilizer generator only Pauli-P errors are propagated on the data qubits and any propagated error has at most one overlap with a (minimum weight) logical operator, d faults are required to make a direct logical error. By linearity, $t = \lfloor (d-1)/2 \rfloor$ faults are distinguishable.

Now, we extend these arguments for circuits using three-qubit CZZ gates, as shown in Fig. 2(a) for a Z-stabilizer measurement. To manage hook errors, two data qubits on the support of the three-qubit gate have to reflect the ordering in the two-qubit case, i.e., rotated surface codes require propagation orthogonal to the logical operators and unrotated surface codes are robust against hook errors.

In addition to hook errors, there are now also weight-3 elementary faults with arbitrary two-qubit Pauli operators on data qubits involved in the CZZ gate. These potentially turn $\mathcal{F}^{(t)}$ indistinguishable. In rotated surface codes for a uniform depolarizing noise model, there is no way to retain distinguishability: if the direction of the CZZ gates is chosen such that, e.g., Pauli-Z hook errors propagate orthogonally to the Z-logical operator, the elementary XX-fault on the data qubits of the CZZ gate is parallel to the X-logical operator, and vice versa. Only if the correlated faults IXX, IXY, IYX, IYY and XXX, XXY, XYX, XYY (Ancilla-Data-Data) are suppressed to $\mathcal{O}(p^2)$, e.g., by dedicated gate engineering [29], distinguishability up to $\mathcal{O}(p^t)$ is guaranteed.

In the unrotated surface code, we differentiate between horizontal-vertical (West-East, WE, or North-South, NS) and diagonal (North-East, NE, or North-West, NW) qubits of a stabilizer that are supported on the CZZ gate; see Figs. 2(b) and 2(c). The horizontal and vertical qubits overlap with Z- and X-logical operators on two positions. Therefore only $\lceil d/2 \rceil$ faults are needed to make a direct undetected logical error. Equivalently, there exist two indistinguishable fault paths in order $\mathcal{F}^{(t)}$, also shown in Fig. 2(b).

For CZZ gates involving the diagonal data qubits, we observe that these contain one of the "outer" $d \times d$ and one from the "inner" $d-1 \times d-1$ square lattice. Realizing that all minimum-weight logical operators of the unrotated surface codes have support only on the outer lattice, we can conclude that faults on these qubits again overlap with minimum-weight logical generators on only a single position. Contrary to rotated surface codes, this also holds for X faults on the support of Z stabilizers, and vice versa [see an example in Fig. 2(c)]. Once more, d faults are required for an undetected logical error, and the fault set $\mathcal{F}^{(t)}$ is distinguishable.

We numerically verify the distinguishability of fault sets for circuits implemented with CZZ gates (cf. Algorithm 1 of Supplemental Material [37]): we first simulate the effect of each elementary fault and then construct all up-to-order-t combinations of faults until we find indistinguishable fault paths. We summarize the results of our exhaustive checks in Table S1 of Supplemental Material [37]. These numerical results complement the above arguments and confirm that, while rotated surface codes have their distance reduced to $d_{\text{eff}} = [(d-1)/2]$, the NE and NW three-qubit gate stabilizer measurement circuits for unrotated surface codes are fault tolerant with the full effective distance $d_{\text{eff}} = d$.

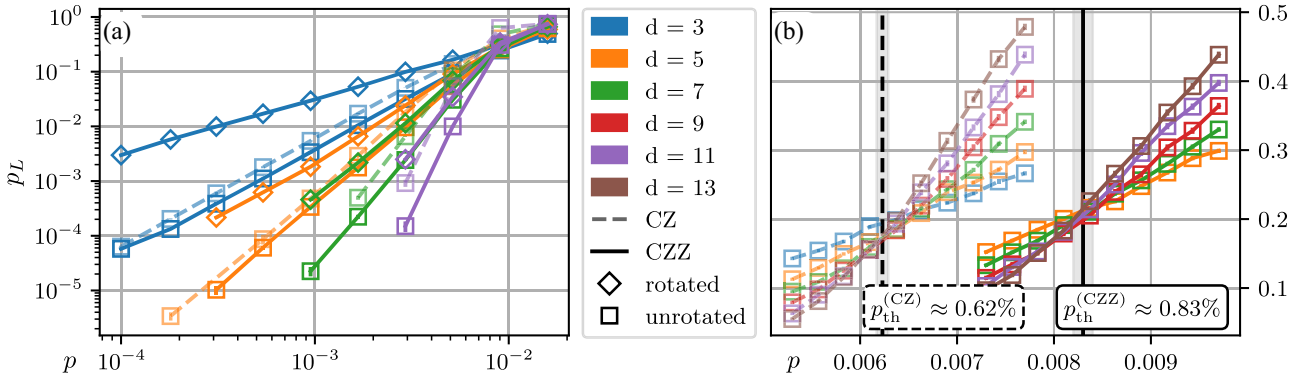

FIG. 3. Logical error rates for implementations using CZ (dashed line) and CZZ gates (solid line). We assume a three-qubit gate noise strength of $\frac{3}{2}p$ and an idling noise strength of $(p/2)$. The color coding represents codes with increasing distance. (a) CZZ circuits for the rotated surface code (◇) are not fault tolerant and show a scaling $\propto \lceil (d+1)/4 \rceil$, consistent with a halved distance. For the unrotated surface code (□), CZZ circuit show the same FT scaling of the logical error rate $p_L \propto p^{(d+1)/2}$ as CZ circuits. Distance-3 and 5 codes correct for all faults up to order $t = \lfloor (d-1)/2 \rfloor$, whereas for larger distances, deviations due to the decoder can be seen; see also Supplemental Material [37]. Because of fewer idling locations using three-qubit gates, the logical error rate is up to 50% lower for physical error rates in the range of 10^{-2} to 10^{-3} when using three-qubit CZZ gates, with more pronounced advantages with increasing distance. (b) The threshold is increased from $p_{\text{th}}^{(\text{CZ})} \approx 0.63\%$ to $p_{\text{th}}^{(\text{CZZ})} \approx 0.83\%$. Decoded using beliefmatching with d iterations of belief propagation (BP) before matching. Error bars are standard Monte Carlo errors and can be smaller than the symbol used. Thresholds are obtained using finite-size scaling (see Supplemental Material [37]).

Memory experiments—To investigate the QEC performance of the three-qubit gate protocol, we perform full circuit level noise memory experiments using stim [46]. We construct circuits for rotated and unrotated surface codes similar to the circuits in the experimental Ref. [13], i.e., we implement X- and Z-stabilizer readout circuits one after another, with measurement of X-(Z-)ancillary qubits during the Z-(X-)entangling gate cycle. In the CZ protocol, we order the gates orthogonal to the logical operators, i.e., South–East–West–North (SEWN) for X- and South–West–East–North (SWEN) for Z-type stabilizers. When using the three-qubit CZZ gate, we order both X and Z stabilizers NW-SE (see Supplemental Material for details [37]). We consider a noise model similar to the SI1000 model of Ref. [47] based on a single noise parameter p, the base noise strength for CZ gates. Single-qubit gates have noise strength $p/10$, initializations $2p$, and measurements $5p$. We assume a noise strength of $\frac{3}{2}p$ for CZZ gates and an idling noise strength of $p/2$. This rests on the assumption that noise is ultimately decoherence limited and a parallelized CZZ gate takes about the same time as a single CZ gate. This can be regarded as an optimistic, though not unrealistic, parameter regime, and the associated QEC performance represents loosely speaking an upper limit of the potential offered by the three-qubit-based approach. For a more in-depth discussion as well as complementary parameter regimes, refer to Supplemental Material [37]. In Ref. [29], we show how a three-qubit CZZ gate with equal gate times as a two-qubit CZ gate can be realized with transmon-based qubits in superconducting circuits. For further details on the circuits, multi-qubit gates and error channels and beliefmatching as the decoder choice, see Supplemental Material [37,48].

We show results on the scaling of the logical error rate for different settings in Fig. 3(a). We compare implementations with CZZ gates for rotated (◇) and unrotated (□) surface codes. For small p, we see the above discussed signatures: the rotated surface codes circuits are not distance preserving and show a scaling $p_L \propto p^{\lceil (d+1)/4 \rceil}$, consistent with a halved distance. The unrotated surface codes with CZZ gates show the fault-tolerant scaling, i.e., $p_L \propto p^{\lfloor (d+1)/2 \rfloor}$. Compared to an implementation with CZ gates in the unrotated surface codes, the absolute value of the logical error rate is also lower, consistent with previous observations [27,30]. We attribute this to the shorter depth and smaller number of fault locations in the CZZ circuits. Notably, with the optimistic assumptions on the noise, the threshold using CZZ gates is much higher compared to the implementation with CZ gates and is increased from $p_{\text{th}}^{(\text{CZ})} \approx 0.63 \pm 0.02\%$ to $p_{\text{th}}^{(\text{CZZ})} \approx 0.83 \pm 0.02\%$; see Fig. 3(b). This is a 32% increase that we again attribute to the smaller number of fault locations. An overview of all obtained thresholds is shown in Table S4 (cf. Supplemental Material [37]).

Qubit-resource comparison for FT QEC—Typically, for practical implementations, the rotated surface code is preferred over its unrotated counterpart because of the smaller qubit count. The unrotated surface code uses $\tilde{n}_{\text{u}} = 4d^2 - 4d + 1$ physical qubits (data + auxiliary) compared to the rotated surface code with $\tilde{n}_{\text{r}} = 2d^2 - 1$, essentially halving the amount of physical qubits required for large distances. This often results in better performance of

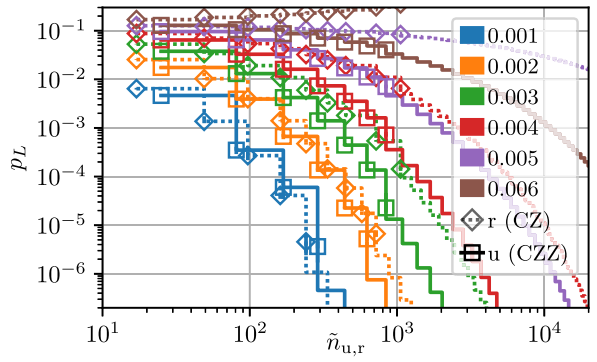

FIG. 4. Number of physical qubits required to reach target logical error rates for d rounds of stabilizer measurements under circuit level noise of strengths $p \in (0.1\%\text{–}0.6\%)$. Comparison of fault-tolerant rotated surface code circuits using CZ gates (rotated square, dotted) and fault-tolerant unrotated surface codes with CZZ gates (square, solid). Extrapolated by the exponential fit function described in the main text. From $p > 0.2\%$, unrotated surface codes consistently require fewer physical qubits than rotated surface codes to reach a target logical error rate.

rotated surface codes for a fixed number of physical qubits. In the following, we show that, in a realistic noise regime, the unrotated surface code with CZZ gates can actually achieve a target logical error rate with *fewer* physical qubits than the traditional rotated surface code circuits using CZ gates. We plot the logical error rate achieved by surface codes against the number of physical qubits in Fig. 4 and compare a CZ-rotated with a CZZ-unrotated implementation for near-term experimentally relevant subthreshold physical error rates in the regime of 0.1%–0.6%. Our key observation is that there is a threshold physical error rate above which the unrotated surface codes require *less* physical qubits to achieve a target logical error rate. We find this error rate at $p_{\mathrm{th}}^{(\circ)} \approx 0.2\%$. To extrapolate to small logical error rates, we fit $p_L(n) = c_0(p/c_1)^{c_2\sqrt{n}}$. Fit parameters are outlined in Supplemental Material Table S2 [37]. At $p = 0.2\%$ and to reach a target logical error rate of 10^{-6}, a value that is considered sufficient for quantum computers to solve useful tasks like factoring of numbers [49], a rotated surface code implemented fault-tolerantly with two-qubit CZ gates has to have distance $d_{\mathrm{r}} = 21$, corresponding to $\tilde{n}_{\mathrm{r}} = 881$ physical qubits. This is already 40% higher than the $\tilde{n}_{\mathrm{u}} = 625$ ($d_{\mathrm{u}} = 13$) qubits for the unrotated surface codes using CZZ gates.

Conclusion—We have investigated the application of three-qubit gates for stabilizer measurement circuits in rotated and unrotated surface codes. We have shown how CZZ-gate-based circuits in unrotated surface codes are fault tolerant, even for an adversarial uniform depolarizing noise model on the support of the three-qubit gates. For an optimistic parameter regime for the achievable fidelity of the multi-qubit gates, logical error rates are lower and thresholds are higher due to a smaller number of fault locations. In particular, we have shown that, for near-term experimentally relevant error rates, unrotated surface codes with CZZ gates can be the less-qubit intensive version to reach a target logical error rate.

Our results with uniform depolarizing noise also suggest that a closer investigation of the noise channels of multi-qubit gates can lead to further improvements. In a parallel work, we construct a CZZ gate that effectively realizes two parallel CZ gates with transmon qubits [29]. We show that an optimization for minimizing fault-tolerance breaking faults can reduce the logical error rates also for rotated surface codes. Several other works have made similar observations about correlated errors. This includes Refs. [50,51] that find dominant noise contributions from weight-2 Z-Pauli terms.

These results put multi-qubit gates back on the map as potentially highly valuable building blocks for QEC which are compatible with FT circuit design principles. Investigating which other quantum low-density parity-check codes like lifted product or bivariate bicycle codes [52–54] allow for fault-tolerant parallelized stabilizer readout is an interesting open question and might improve practical feasibility of such larger classes of QEC codes.

Note added—We have became aware of related work on quantum error correction via three-qubit gates in Rydberg atom arrays in Ref. [55].

Acknowledgments—We gratefully acknowledge support by the European Union's Horizon Europe research and innovation programme under Grant Agreement No. 101114305 ("MILLENION-SGA1" EU Project). This research is also part of the Munich Quantum Valley (K-8), which is supported by the Bavarian state government with funds from the Hightech Agenda Bayern Plus. We additionally acknowledge support by the Federal Ministry of Research, Technology and Space of Germany (BMFTR) project MUNIQC-ATOMS (Grant No. 13N16070) and the BMFTR project GeQCoS (Grant No. 13N15684). M. M. also acknowledges support for the research by the European ERC Starting Grant QNets through Grant No. 804247 and by IARPA and the U.S. Army Research Office, under the Entangled Logical Qubits program through Cooperative Agreement No. W911NF-23-2-0216. M. M. and J. O. acknowledge support by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Germany's Excellence Strategy "Cluster of Excellence Matter and Light for Quantum Computing (ML4Q) EXC 2004/1" No. 390534769. The authors gratefully acknowledge the computing time provided to them at the NHR Center NHR4CES at RWTH Aachen University (Project No. p0020074). This is funded by the Federal Ministry of Research, Technology and Space and the state governments participating on the basis of the resolutions of the GWK for national high performance computing at universities.

The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of IARPA, the Army Research Office, or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

Data availability—The data that support the findings of this article are openly available [56].

[1] E. Knill, R. Laflamme, and W. H. Zurek, Resilient quantum computation: Error models and thresholds, Proc. R. Soc. A **454**, 365 (1998).
[2] B. M. Terhal, Quantum error correction for quantum memories, Rev. Mod. Phys. **87**, 307 (2015).
[3] P. Aliferis, D. Gottesman, and J. Preskill, Quantum accuracy threshold for concatenated distance-3 codes, Quantum Inf. Comput. **6**, 97 (2006).
[4] P. Shor, Fault-tolerant quantum computation, in *Proceedings of 37th Conference on Foundations of Computer Science* (IEEE, Los Alamitos, California, 1996), pp. 56–65, 10.1109/SFCS.1996.548464.
[5] A. M. Steane, Active stabilization, quantum computation, and quantum state synthesis, Phys. Rev. Lett. **78**, 2252 (1997).
[6] T. J. Yoder and I. H. Kim, The surface code with a twist, Quantum **1**, 2 (2017).
[7] R. Chao and B. W. Reichardt, Quantum error correction with only two extra qubits, Phys. Rev. Lett. **121**, 050502 (2018).
[8] C. Chamberland and M. E. Beverland, Flag fault-tolerant error correction with arbitrary distance codes, Quantum **2**, 53 (2018).
[9] T. Tansuwannont and D. Leung, Achieving fault tolerance on capped color codes with few ancillas, PRX Quantum **3**, 030322 (2022).
[10] A. G. Manes and J. Claes, Distance-preserving stabilizer measurements in hypergraph product codes, Quantum **9**, 1618 (2025).
[11] Y. Tomita and K. M. Svore, Low-distance surface codes under realistic quantum noise, Phys. Rev. A **90**, 062320 (2014).
[12] N. Berthusen, J. Dreiling, C. Foltz, J. P. Gaebler, T. M. Gatterman, D. Gresh, N. Hewitt, M. Mills, S. A. Moses, B. Neyenhuis, P. Siegfried, and D. Hayes, Experiments with the four-dimensional surface code on a quantum charge-coupled device quantum computer, Phys. Rev. A **110**, 062413 (2024).
[13] S. Krinner, N. Lacroix, A. Remm, A. D. Paolo, E. Genois, C. Leroux, C. Hellings, S. Lazar, F. Swiadek, J. Herrmann, G. J. Norris, C. K. Andersen, M. Müller, A. Blais, C. Eichler, and A. Wallraff, Realizing repeated quantum error correction in a distance-three surface code, Nature (London) **605**, 669 (2022).
[14] Y. Zhao *et al.*, Realization of an error-correcting surface code with superconducting qubits, Phys. Rev. Lett. **129**, 030501 (2022).
[15] Google Quantum AI, Suppressing quantum errors by scaling a surface code logical qubit, Nature (London) **614**, 676 (2023).
[16] Google Quantum AI and Collaborators, Quantum error correction below the surface code threshold, Nature (London) **638**, 920 (2025).
[17] J. F. Marques, B. M. Varbanov, M. S. Moreira, H. Ali, N. Muthusubramanian, C. Zachariadis, F. Battistel, M. Beekman, N. Haider, W. Vlothuizen, A. Bruno, B. M. Terhal, and L. DiCarlo, Logical-qubit operations in an error-detecting surface code, Nat. Phys. **18**, 80 (2022).
[18] J. Zhang, Z.-Y. Chen, Y.-J. Wang, B.-H. Lu, H.-F. Zhang, J.-N. Li, P. Duan, Y.-C. Wu, and G.-P. Guo, Demonstrating a universal logical gate set in error-detecting surface codes on a superconducting quantum processor, npj Quantum Inf. **11**, 177 (2025).
[19] S. Burton, E. Durso-Sabina, and N. C. Brown, Genons, double covers and fault-tolerant Clifford gates, arXiv:2406.09951.
[20] D. Bluvstein *et al.*, Logical quantum processor based on reconfigurable atom arrays, Nature (London) **626**, 58 (2024).
[21] M. D. Lukin, M. Fleischhauer, R. Cote, L. M. Duan, D. Jaksch, J. I. Cirac, and P. Zoller, Dipole blockade and quantum information processing in mesoscopic atomic ensembles, Phys. Rev. Lett. **87**, 037901 (2001).
[22] S. J. Evered, D. Bluvstein, M. Kalinowski, S. Ebadi, T. Manovitz, H. Zhou, S. H. Li, A. A. Geim, T. T. Wang, N. Maskara, H. Levine, G. Semeghini, M. Greiner, V. Vuletić, and M. D. Lukin, High-fidelity parallel entangling gates on a neutral-atom quantum computer, Nature (London) **622**, 268 (2023).
[23] A. Bermudez, X. Xu, R. Nigmatullin, J. O'Gorman, V. Negnevitsky, P. Schindler, T. Monz, U. G. Poschinger, C. Hempel, J. Home, F. Schmidt-Kaler, M. Biercuk, R. Blatt, S. Benjamin, and M. Müller, Assessing the progress of trapped-ion processors towards fault-tolerant quantum computation, Phys. Rev. X **7**, 041061 (2017).
[24] D. P. DiVincenzo and F. Solgun, Multi-qubit parity measurement in circuit quantum electrodynamics, New J. Phys. **15**, 075001 (2013).
[25] Y. Kim, A. Morvan, L. B. Nguyen, R. K. Naik, C. Jünger, L. Chen, J. M. Kreikebaum, D. I. Santiago, and I. Siddiqi, High-fidelity three-qubit iToffoli gate for fixed-frequency superconducting qubits, Nat. Phys. **18**, 783 (2022).
[26] G. Üstün, A. Morello, and S. Devitt, Single-step parity check gate set for quantum error correction, Quantum Sci. Technol. **9**, 035037 (2024).
[27] M. J. Reagor, T. C. Bohdanowicz, D. R. Perez, E. A. Sete, and W. J. Zeng, Hardware optimized parity check gates for superconducting surface codes, arXiv:2211.06382.
[28] D. Schwerdt, Y. Shapira, T. Manovitz, and R. Ozeri, Comparing two-qubit and multiqubit gates within the toric code, Phys. Rev. A **105**, 022612 (2022).
[29] S. Tasler, J. Old, L. Heunisch, V. Feulner, T. Eckstein, M. Müller, and M. J. Hartmann, Optimizing superconducting three-qubit gates for surface-code error correction, arXiv:2506.09028.
[30] S. Jandura and G. Pupillo, Surface code stabilizer measurements for Rydberg atoms, arXiv:2405.16621.

[31] D. Gottesman, *Stabilizer Codes and Quantum Error Correction* (California Institute of Technology, Pasadena, California, 1997).
[32] E. Dennis, A. Kitaev, A. Landahl, and J. Preskill, Topological quantum memory, J. Math. Phys. (N.Y.) **43**, 4452 (2002).
[33] H. Bombin and M. A. Martin-Delgado, Optimal resources for topological two-dimensional stabilizer codes: Comparative study, Phys. Rev. A **76**, 012305 (2007).
[34] D. Horsman, A. G. Fowler, S. Devitt, and R. Van Meter, Surface code quantum computing by lattice surgery, New J. Phys. **14**, 123011 (2012).
[35] D. Gottesman, *Surviving as a Quantum Computer in a Classical World* (2024), https://www.cs.umd.edu/class/spring2024/cmsc858G/.
[36] J.-P. Tillich and G. Zémor, Quantum LDPC codes with positive rate and minimum distance proportional to the square root of the blocklength, IEEE Trans. Inf. Theory **60**, 1193 (2013).
[37] See Supplemental Material at http://link.aps.org/supplemental/10.1103/sblg-fbq4 contains details on circuits, on simulation and verification methods, as well as additional simulations related to the CZZ gate noise strength, which includes Refs. [38–45].
[38] C. Gidney, Decorrelated depolarization, https://algassert.com/post/2001 (2020), accessed: 14-Febuary-2025.
[39] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, Surface codes: Towards practical large-scale quantum computation, Phys. Rev. A **86**, 032324 (2012).
[40] O. Melchert, autoScale.py—A program for automatic finite-size scaling analyses: A user's guide, arXiv:0910.5403.
[41] A. Sorge, PYFSSA 0.7.6, Zenodo 10.5281/zenodo.35293 (2015).
[42] A. Sørensen and K. Mølmer, Entanglement and quantum computation with ions in thermal motion, Phys. Rev. A **62**, 022311 (2000).
[43] E. Zahedinejad, J. Ghosh, and B. C. Sanders, Designing high-fidelity single-shot three-qubit gates: A machine-learning approach, Phys. Rev. Appl. **6**, 054005 (2016).
[44] C. J. Ballance, T. P. Harty, N. M. Linke, M. A. Sepiol, and D. M. Lucas, High-fidelity quantum logic gates using trapped-ion hyperfine qubits, Phys. Rev. Lett. **117**, 060504 (2016).
[45] L. Abdurakhimov *et al.*, Technology and performance benchmarks of IQM's 20-Qubit quantum computer, arXiv:2408.12433.
[46] C. Gidney, Stim: A fast stabilizer circuit simulator, Quantum **5**, 497 (2021).
[47] C. Gidney, M. Newman, and M. McEwen, Benchmarking the planar honeycomb code, Quantum **6**, 813 (2022).
[48] O. Higgott, T. C. Bohdanowicz, A. Kubica, S. T. Flammia, and E. T. Campbell, Improved decoding of circuit noise and fragile boundaries of tailored surface codes, Phys. Rev. X **13**, 031007 (2023).
[49] J. Preskill, Reliable quantum computers, Proc. R. Soc. A **454**, 385 (1998).
[50] T. Itoko, M. Malekakhlagh, N. Kanazawa, and M. Takita, Three-qubit parity gate via simultaneous cross-resonance drives, Phys. Rev. Appl. **21**, 034018 (2024).
[51] X. Xu, S. Wang, R. Joshi, R. Hai, and M. H. Ansari, Parity cross-resonance: A multiqubit gate, arXiv:2508.10807.
[52] Q. Xu, J. P. Bonilla Ataides, C. A. Pattison, N. Raveendran, D. Bluvstein, J. Wurtz, B. Vasić, M. D. Lukin, L. Jiang, and H. Zhou, Constant-overhead fault-tolerant quantum computation with reconfigurable atom arrays, Nat. Phys. **20**, 1084 (2024).
[53] S. Bravyi, A. W. Cross, J. M. Gambetta, D. Maslov, P. Rall, and T. J. Yoder, High-threshold and low-overhead fault-tolerant quantum memory, Nature (London) **627**, 778 (2024).
[54] J. Old, M. Rispler, and M. Müller, Lift-connected surface codes, Quantum Sci. Technol. **9**, 045012 (2024).
[55] L. Pecorari, S. Jandura, and G. Pupillo, following Letter, Low-depth quantum error correction via three-qubit gates in Rydberg atom arrays, Phys. Rev. Lett. **135**, 240602 (2025).
[56] J. Old, oldjosias/three-qubit-ft-sc: v2.0.0, 10.5281/zenodo.17816307 (2025).
[57] S. Aaronson and D. Gottesman, Improved simulation of stabilizer circuits, Phys. Rev. A **70**, 052328 (2004).
[58] P.-J. H. S. Derks, A. Townsend-Teague, A. G. Burchards, and J. Eisert, Designing fault-tolerant circuits using detector error models, Quantum **9**, 1905 (2025).

End Matter

Fault tolerance of error correction circuits—Here, we provide more technical details on the definitions of fault-tolerant circuits used in the main text. We use the following definition of circuit fault tolerance [3,9]. We consider a circuit with (Clifford) gate locations, initializations, and measurements. Additionally, we define *detectors* as sums of measurements that are *deterministic* in the absence of noise. Typically, a matrix $H \in \mathbb{F}_2^{n_{\text{detectors}} \times n_{\text{measurements}}}$ maps from bare measurement outcomes to detector flips. For a circuit measuring stabilizer generators of a QEC code that is in a $+1$ eigenstate of all generators, this can be an identity matrix. Every location $\ell \in \mathcal{L} = \{0, \ldots, n_{\text{locations}} - 1\}$ of the circuit can be faulty, which is simulated by an ideal gate followed by a Pauli noise channel with error set $E(\ell)$. For n-qubit gates and idling locations, we assume n-qubit depolarizing channels:

$$\mathcal{E}_n(\rho) = (1-p)\rho + \frac{p}{4^n - 1}\sum_{i=1}^{4^n-1} P_n^i \rho P_n^i \quad \text{with} \quad P_n^i \in \{\{I, X, Y, Z\}^n \backslash I^{\otimes n}\}. \tag{A1}$$

Single-qubit Z-basis initialization (measurement) is followed (preceded) by a bit-flip channel,

$$\mathcal{E}(\rho) = (1-p)\rho + pX\rho X. \tag{A2}$$

We label each elementary fault with the location ℓ and the nonidentity Pauli realization P of the corresponding channel, such that the set of all elementary faults is $\mathcal{F}_1 = \{F_\ell^P\}_{\ell \in \mathcal{L}, P \in E(\ell)}$. If the actual Pauli realization of the fault is not important, we typically drop the Pauli label. Each fault is efficiently propagated through the circuit using Clifford simulation [57], resulting in a (deterministic) *error* $E(F)$, a vector of measurement outcomes $\mathbf{m}(F)$, and flipped detectors $\mathbf{D}(F) = H\mathbf{m}(F)$. An order-$w$ *fault path* $\mathbf{F}$ is a set of w faults at distinct locations, $\mathbf{F} = \{F_\ell\}_{\ell \in L \subseteq \mathcal{L}, |L|=w}$. The errors and flipped detectors that result from all faults in a fault path can be calculated as $E(\mathbf{F}) = \prod_{F \in \mathbf{F}} E(F)$ and $\mathbf{D}(\mathbf{F}) = \bigoplus_{F \in \mathbf{F}} \mathbf{D}(F)$, respectively, where $\oplus$ denotes element-wise summation modulo 2.

If any fault path up to order t in p leads only to correctable errors (and could hence be corrected by a subsequent ideal round of stabilizer measurement), then we say the circuit is *distance preserving* and fault tolerant. This is captured by the notion of *distinguishable fault sets* [9].

Definition 1—We call the collection of all possible fault paths of order $\leq w$ the *fault set* $\mathcal{F}^{(w)}$. A fault set is *distinguishable* if for any pair of fault paths $\mathbf{F}_i, \mathbf{F}_j \in \mathcal{F}^{(w)}$, either (1) $\mathbf{s}[E(\mathbf{F}_i)] \neq \mathbf{s}[E(\mathbf{F}_j)]$, (2) $E(\mathbf{F}_i) \sim_{\mathcal{S}} E(\mathbf{F}_j)$, or (3) $\mathbf{D}(\mathbf{F}_i) \neq \mathbf{D}(\mathbf{F}_j)$, that is, any two fault paths either result in errors with different syndromes (1), in stabilizer-equivalent errors (2), or in different detector flips during the protocol (3).

The quantities used in this approach are visualized in the main text in Fig. 1. As an example, we show in Fig. 5(a) a detail of a Z-stabilizer measurement using two-qubit CZ gates. Depending on the order of gates, the fault set $\mathcal{F}^{(1)}$ is (b) indistinguishable or (c) distinguishable.

The key technical observation (Proposition 1 of Ref. [9]) is that iff $\mathcal{F}^{(w)}$ is distinguishable, then the smallest fault path leading to a direct, undetected logical error is in $\mathcal{F}^{(2w+1)}$. This implies that a circuit employing a code of distance d with elementary fault set $\mathcal{F}_1$ is fault tolerant iff the fault set $\mathcal{F}^{(t)}$ is distinguishable. This is a similar situation compared to fault tolerance in detector error models; see, e.g., Ref. [58].

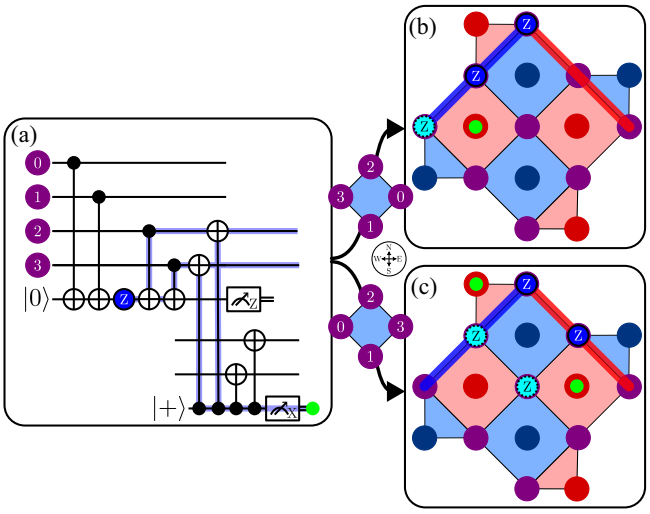

FIG. 5. Detail of stabilizer measurement circuits for the distance-3 rotated surface code. (a) A Z fault on the ancilla of a Z-stabilizer measurement can propagate to two data qubits, indicated by the blue highlighting. The propagated fault is detected in the next round of X-stabilizer measurements. (b), (c) Show the effect for two different orderings of the gates. In the rotated surface codes, we draw the X-(Z-)logical operators as thick red (blue) lines and draw flipped detectors with a light green dot. (b) If the last two gates act on the north (N) and west (W) qubit, the final Z error is parallel to the Z-logical operator. There is another first order fault with the same syndrome that is logically inequivalent implying a nondistinguishable fault set $\mathcal{F}^{(1)}$. (c) For an ordering toward the north (N) and east (E) qubit, however, faults with the same flipped detectors are stabilizer equivalent. The fault set $\mathcal{F}^{(1)}$ is thus distinguishable.