Towards 1-D conduction in gate-defined quantum point contacts on GeSn quantum wells

Prateek Kaul *[1,4], Jan Karthein[1,4], Jonas Buchhorn[1,4], Taizo Kawano[2], Taisei Usubuchi[2], Jun Ishihara[2], Nicolas Rotaru[3], Detlev Grützmacher[1,4], Qing-Tai Zhao[1], Oussama Moutanabbir[3], Makoto Kohda[2], Thomas Schäpers[1,2,4] and Dan Buca[1]

[1]Peter Gruenberg Institute 9 (PGI-9) and JARA-Fundamentals of Future Information Technologies, Forschungszentrum Juelich, Germany
[2]Department of Material Engineering, Tohoku University, Japan
[3]Department of Engineering Physics, École Polytechnique de Montréal, Montréal, Canada
[4]RWTH Aachen University - 52062 Aachen, Germany
Tel: +49 2461/61-85593, E-mail: p.kaul@fz-juelich.de

In the light of the growing energy demands of AI-based computing [1], spin-based computing approaches, such as spintronics and spin qubits, offer the potential to reduce the high energy consumption associated with traditional charge-based computation [2,3]. In recent years, CMOS compatibility, low nuclear spins, high spin-orbit interaction (SOI), and low effective masses has made the hole system in Ge very desirable [4]. The novel Sn-based group-IV alloys with properties expected to surpass those of pure Ge - are emerging as the next step of materials for such spin-based applications.

Recent reports have shown phase-coherent transport of Γ-electrons [5] and demonstration of 2D hole gases (2DHG) in GeSn alloys, with experimental proof of the theoretically predicted enhancements with low effective mass, high g-factors and high Rashba spin-orbit interaction [6]. Fundamental material parameters required to design novel devices such as gate-defined quantum point contacts (QPC) and quantum dots (QD) are presented, the first steps of which form the crux of this abstract. Therefore, the work focuses on demonstration and characterization of the one-dimensional transport of holes in quantum point contacts, based on the previously defined Ge/GeSn quantum well system.

The fabrication process is similar to the gated Hall bars in ref. [6] with an additional gate step to form the split-gates. Split-gates are defined using electron-beam lithography with constriction widths down to 50 nm. Between each gate step, 15 nm HfO_2 grown using atomic layer deposition is used as gate-dielectric. The final device is shown in Fig. 1a with the fine gates shown clearly in the inset with a constriction gate length of 100 nm and constriction width of 50 nm.

Gate-dependent transport measurements are performed at 1.3K in a variable temperature insert setup. The sample is excited with a current of 10 nA and the voltage is measured using standard lock-in techniques to obtain conductance (G = I/V). The top gate is kept at -1.4V in order to induce a 2DHG. The fine gates are shorted together and the voltage (V_{fg}) is swept.

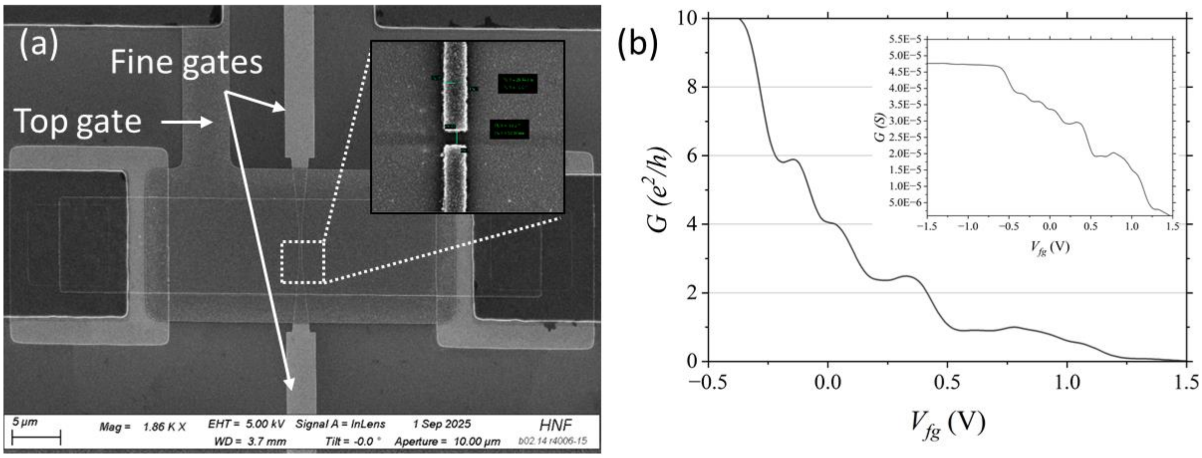

Fig. 1: QPC on Ge/GeSn QW: (a) SEM image of the QPC device with top and fine gates denoted. Highlighted area provided in the inset to show the fine gates with a separation of 50 nm more clearly. (b) Conductance of the QPC as a function of fine-gate voltage (V_{fg}) in units of the conductance quantum after correction for resistance of the whole device. Raw data in the inset.

The raw data from the gate sweep is plotted in the inset of Fig. 1b and steps can be observed as the device pinches off. The conductance of the QPC is plotted after correcting the series resistance of the whole device (by subtracting the on-resistance at V_{fg} = -1V) in Fig. 1b and shows steps at multiples of 2,4,6 of the conductance quantum corresponding to the three spin-degenerate levels, proving that confinement by the fine gates is well defined and 1-D conduction is observed. Further measurements with application of magnetic fields as well at different dc-biases are underway to obtain quantization energies and their dependence on the magnetic field [7]. However, the preliminary results already show the viability of hosting 1-D conduction and sets forward experimentation to possibly obtain QDs on such heterostructures.

References

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