Measurement-Free Quantum Error Correction Optimized for Biased Noise

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In this paper, we derive optimized measurement-free protocols for quantum error correction and the implementation of a universal gate set optimized for an error model that is noise biased. The noise bias is adapted for neutral-atom platforms, where two- and multi-qubit gates are realized with Rydberg interactions and are thus expected to be the dominant source of noise. Careful design of the gates allows us to further reduce the noise model to Pauli-Z errors. In addition, the presented circuits are robust to arbitrary single-qubit gate errors, and we demonstrate that the break-even point can be significantly improved compared to fully fault-tolerant measurement-free schemes. The obtained logical qubits with their suppressed error rates on logical gate operations can then be used as building blocks in a first step of error correction in order to push the effective error rates below the threshold of a fully fault-tolerant and scalable quantum error-correction scheme.

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I. INTRODUCTION

Achieving fault tolerance is one of the key challenges in the field of quantum computing. Quantum error correction (QEC) is a promising tool to protect quantum information against noise [1]. Recently, great progress has been made in the implementation of QEC codes on various quantum computing platforms [2–7]. Fault-tolerant quantum computing requires the ability to encode logical qubits, to correct errors, and to perform logical gates, while suppressing the uncontrolled spread of errors during these operations. However, a QEC code with a transversal universal logical gate set cannot exist [8]. Promising candidates for the completion of universal logical gate sets are, e.g., magic state injection [9,10] and code switching [11,12]. However, most of these implementations as well as many QEC protocols require midcircuit measurements and feedforward operations. On many platforms, measurements are slow and thus induce high error rates on idling qubits. There are several proposals to speed up measurements, such as enhancing the photon signal using optical cavities [13,14] or by means of several auxiliary qubits [15,16]. An alternative is measurement-free QEC [17–24]. Here, instead of measuring auxiliary qubits and applying feedback depending on the measurement outcome, the coherent feedback is directly implemented with quantum gates controlled by the auxiliary qubits. Entropy is then removed from the system by resetting the auxiliary qubits afterward. Fault-tolerant circuits for error correction without midcircuit measurements have been proposed in Refs. [25,26], and recently, measurement-free, fault-tolerant, and scalable universal logical gate sets have been constructed [27,28]. Although measurement-free QEC does not require midcircuit measurements, it comes with the cost of additional quantum gates in the feedback and thus higher gate fidelities are required. To reduce the requirements and optimize the threshold, it is beneficial to tailor the QEC protocols toward the characteristics of the respective platforms [29–31].

One promising platform for quantum computing are neutral atoms that are trapped in optical tweezers [5,6,32–40]. Tweezer arrays allow one to arrange atoms in flexible geometries and offer the possibility of reshuffling atoms during the computation, which implies high connectivities [41]. Furthermore, the arrays can be scaled up to large numbers of qubits, and recently arrays with thousands of qubits have been demonstrated [40]. The qubits are encoded in long-lived electronic states, e.g., different hyperfine ground states or clock states. High-fidelity

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single-qubit gates can be implemented using laser or microwave pulses. Entangling gates make use of the Rydberg blockade mechanism, where the excitation of one atom to a Rydberg state blocks the excitation of neighboring atoms [42]. Furthermore, the blockade mechanism natively supports the implementation of multi-qubit gates. In recent years, great progress has been made in achieving high-fidelity single- and two-qubit gates [34–37,43–45]. Typical sources of noise are laser noise, photon recoil, and decay from the Rydberg state. Careful gate design allows to simplify the physical noise model, e.g., by converting all errors to erasure errors [46,47] or to phase errors [31,48].

In this work, we construct reduced QEC circuits and a universal logical gate set for a measurement-free setup, where Z errors on two- and multi-qubit gates dominate the noise model. This biased-noise model allows us to decrease the qubit and gate overhead and thus push the break-even point (at which logical errors become less likely than physical errors) into a regime that is feasible with state-of-the-art experiments. We encode the logical qubits in $[[7,1,3]]$ Steane codes, which allows for the transversal realization of Clifford gates. To implement the T gate we invent protocols for measurement-free magic state injection that are fault tolerant under the biased-noise model. Remarkably, we find that the protocols are even robust to arbitrary errors on single-qubit gates. Furthermore, we show that the discussed protocols can still be used to suppress the logical error rate even if the noise is not perfectly biased and bit-flip errors on two- and multi-qubit gates occur with a small probability.

The seven-qubit Steane code allows the correction of up to one physical error. The general idea is that such a first round of error correction optimized for a platform-specific noise model allows one to reduce the error rate of the logical operations below the threshold of a scalable and fully fault-tolerant error-correction protocol. The obtained logical qubits with their suppressed error rates can then be used as building blocks for more general QEC codes, where physical error rates lie above the threshold, to perform universal quantum computation.

The rest of this work is structured as follows. In Sec. II we review the seven-qubit Steane code and introduce the biased-noise model. In Sec. III we present the reduced QEC circuits and the T gate and discuss the logical-noise model of all relevant quantum operations. In Sec. IV we consider more general noise models and discuss the effects of imperfect noise bias. In Sec. V we discuss possible implementations on Rydberg platforms. Finally, we conclude in Sec. VI.

II. SETUP

Our goal is to provide logical qubits with reduced error rates that can be used as building blocks for higher-level error-correction protocols or to directly perform quantum algorithms. This requires the ability to encode information into the logical subspace, QEC protocols, and a universal logical gate set. While all these building blocks are usually built on midcircuit measurements, we aim to provide measurement-free protocols.

As logical qubits we use the seven-qubit Steane code [49]. The $[[7,1,3]]$ Steane code encodes $k=1$ logical qubit into $n=7$ physical qubits. The code has distance $d=3$ and is designed to independently correct bit-flip errors and phase errors on up to one qubit. The code is defined by the stabilizer group generated by the operators (see Fig. 1)

$$\begin{aligned} &X_0X_1X_2X_3, \quad Z_0Z_1Z_2Z_3,\\ &X_0X_3X_4X_5, \quad Z_0Z_3Z_4Z_5,\\ &X_0X_1X_5X_6, \quad Z_0Z_1Z_5Z_6. \end{aligned} \tag{1}$$

The X stabilizers enable the correction of Z errors and the Z stabilizers enable the correction of X errors. The logical operators $X_L = X_1X_2X_6$ and $Z_L = Z_1Z_2Z_6$ act on one side of the triangle (see Fig. 1). A convenient property of the Steane code is that many logical gates can be performed transversally; in particular, the logical H gate is realized by applying a physical H gate to every single data qubit, the logical S gate is realized by applying a physical $S^\dagger$ gate to every data qubit, and the logical CZ-gate is obtained by applying physical CZ-gates to every pair of data qubits in the two code blocks. The only gate that is missing for universality is the T gate, which can be implemented by means of magic state injection or code switching.

A compact circuit for fault-tolerantly encoding $|0_L\rangle$ without midcircuit measurements is given in Ref. [25] and fault-tolerant QEC cycles without midcircuit measurements are presented in Refs. [25,26]. As already mentioned, for the universal gate set on the Steane code one only needs to implement a T gate, as all other gates needed for universality can be performed transversally. In Ref. [27], a measurement-free fault-tolerant T gate for the Steane code is presented based on code switching. Here, we consider a platform-specific noise model, to reduce the requirements for the error-correction cycles and the T gate.

Inspired by Rydberg quantum processors [31,48], we consider a platform that natively supports single-qubit rotations (in particular the X, H, S, and T gates) as well as multi-controlled Z gates (the CZ-, CCZ-, and CCCZ-gates), and controlled-phase- (CP) gates. Initially, we assume that the only gates that can fail are the two- and multi-qubit gates with noise channels

$$\mathcal{E}_l(\rho) = (1-p)\rho + \frac{p}{2^l-1}\sum_{P\in\{I,Z\}^{\otimes l}\setminus I^{\otimes l}} P\rho P, \tag{2}$$

where l is the number of qubits involved in the gate and p is the error rate. The noise model is illustrated exemplarily

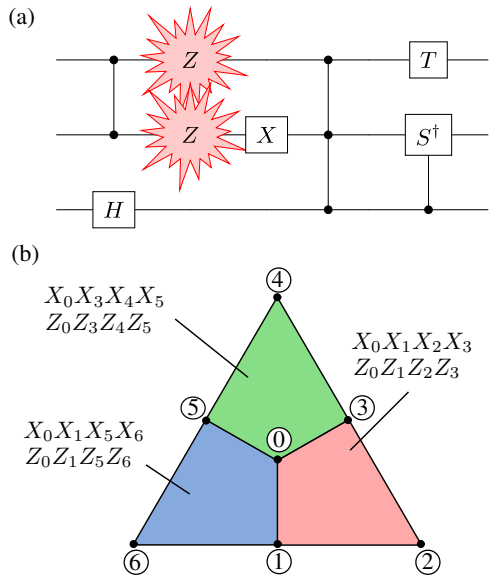

FIG. 1. (a) An exemplary circuit. Our set of basis gates includes controlled-phase gates [in particular the controlled-Z- (CZ) gate and the controlled-S (CS†) gate], the H, X, and T gates and the multi-controlled Z gates (e.g., the CCZ-gate). Initially, we assume the noise model defined in Eq. (2), where only Z-type errors appear after two- and multi-qubit gates. (b) The $[[7,1,3]]$-qubit Steane code. The code has distance $d=3$ and is designed to correct bit-flip errors and phase errors on up to one qubit. The code is defined by the stabilizer group generated by the operators shown. The logical X_L and Z_L operators act on one side of the triangle.

in Fig. 1 and a detailed discussion of the validity of this noise model is given in Appendix A. In Sec. IV we extend our results to more general noise models including faulty single-qubit gates, faulty initialization, and bit-flip errors after two- and multi-qubit gates.

The biased-noise model suggests that it is sufficient to use a QEC code for correcting Z errors only. However, with the above gate set Z errors can be converted into X errors that are then no longer correctable. For example, a controlled-X (CX) gate with the assumed gate set would be compiled into two H gates and a CZ-gate. If the CZ-gate fails and a Z error occurs, the H gate rotates the Z error into an X error. Thus, we consider the seven-qubit Steane code that can correct X errors as well. The benefit of the biased-noise model enters in the form of reduced requirements for fault-tolerant error-correction cycles and the logical T gate.

III. LOGICAL QUBITS WITH BIASED NOISE

In this section we first present the measurement-free circuits for encoding of $|0_L\rangle$, error correction and the T gate and in particular show that the requirements for the error-correction cycle and the implementation of the T gate can be reduced for the biased-noise model. Afterward, we discuss the logical-noise model of all building blocks and compare the measurement-free QEC cycle and T gate with measurement-based schemes in the presence of idling noise.

A. Encoding of $|0_L\rangle$

We use the circuit presented in Ref. [25] to encode the state $|0_L\rangle$ in a measurement-free fashion. The encoding circuit is shown in Appendix E, in Fig. 9. The logical zero state is initially encoded non-fault-tolerantly. Note that while in general weight-2 errors cannot be corrected in the $[[7,1,3]]$ Steane code, this is possible when encoding the $|0_L\rangle$ state, since here the desired logical state is known. To detect potential weight-2 errors, the operator Z_L and the stabilizer $Z_0Z_2Z_4Z_6$ are subsequently mapped out into auxiliary qubits. If a dangerous weight-2 error has occurred, both auxiliary qubits are flipped. In this case, the qubit in the middle of the Steane triangle has to be flipped, such that at most a weight-1 error is left. To correct the error without measurement, one applies a controlled-controlled-X (CCX) gate, controlled by the two auxiliary qubits. The circuit is fault tolerant with respect to a general depolarizing noise model. However, also for the biased noise model weight-2 errors during the non-fault-tolerant encoding can appear, making the Z_L and stabilizer extractions indispensable.

B. Error-correction cycle with biased noise

The reduced error-correction cycle for the Steane code with biased noise is illustrated in Fig. 2. We verify numerically that the QEC protocol is fault tolerant with respect to the biased-noise model in Eq. (2) by simulating all possible error patterns, where one gate fails (see also Appendix B). In the Steane code X and Z errors can be corrected independently. Thus, we first extract the Z stabilizers to detect X errors and apply a coherent feedback operation to correct them. To correct Z errors, we then apply a logical H gate (a physical H gate to all data qubits) to transform Z errors into X errors and again apply the circuit for correcting X errors. Finally, another logical H gate is applied to map the state back to the initial logical state. The extraction of an overcomplete set of stabilizers in the second half of the protocol ensures that a single error on the syndrome qubits cannot lead to wrong feedback, such that a faulty error-correction cycle cannot introduce combinations of X and Z errors. In the first half of the error-correction protocol such errors can appear if a CZ-gate fails on both qubits during the stabilizer extraction. Such a fault leads immediately to a Z error on one data qubit and in addition to an X error after the feedback [propagated by the gate marked in red in Fig. 2(b)]. However, in the second half of the protocol the Z error is corrected, such that the remaining error is a weight-1 X error.

It is important to point out that the Steane code allows one to correct X and Z errors independently and combinations of X and Z errors are thus in principle correctable.

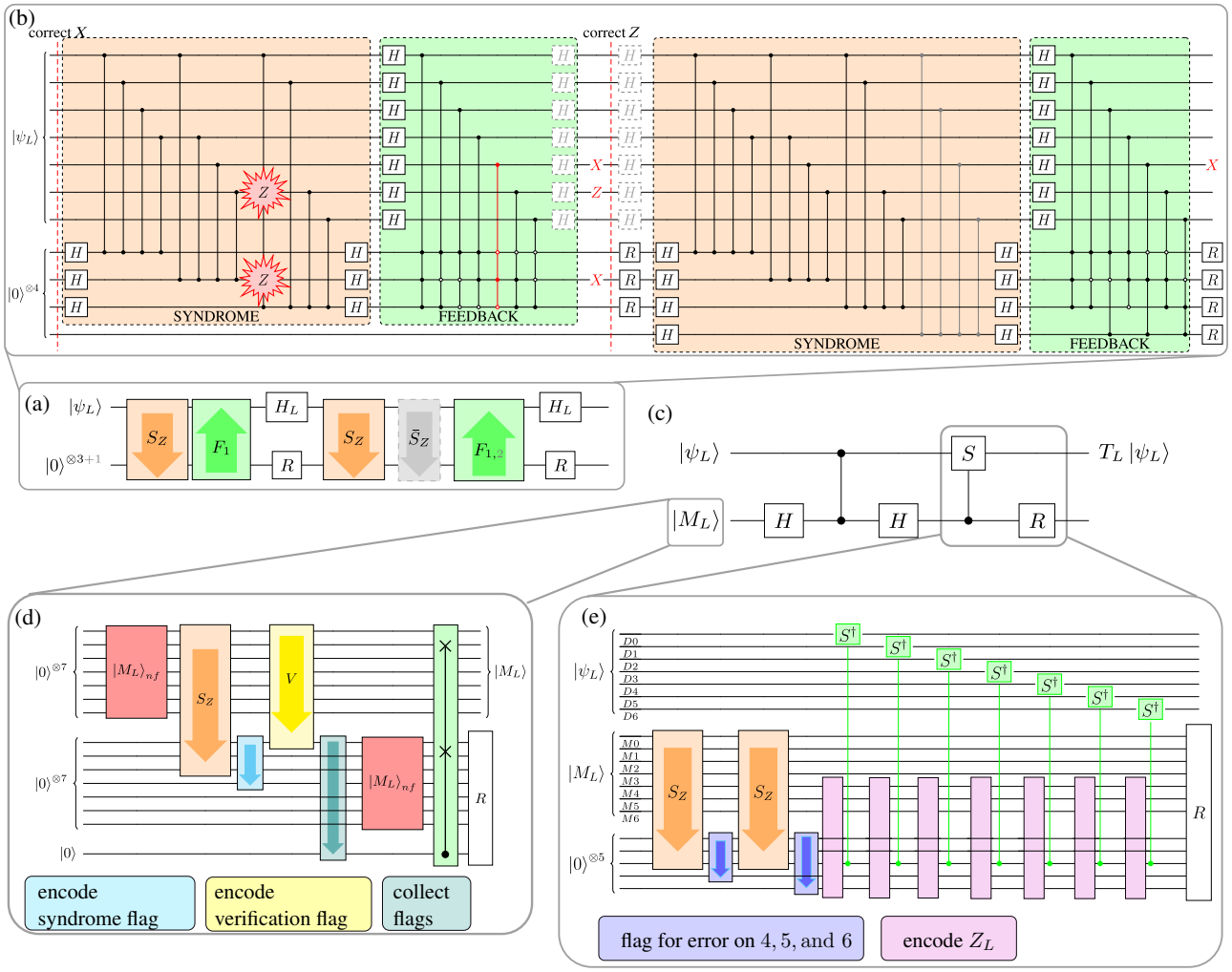

FIG. 2. Circuits for error correction and the T gate. (a) The schematic circuit for the error-correction scheme. For the second round of stabilizer extraction an additional stabilizer $X_0X_2X_4X_6$ (gray gates) has to be mapped out to avoid combinations of X and Z errors. However, this is only required before performing logical T and S gates. Otherwise, the extraction of an overcomplete set is not required and the feedback for correcting Z errors is similar to the feedback for correcting X errors (first green box). We refer to this as the reduced error-correction cycle. (b) The detailed error-correction circuit. (c) Magic state injection. (d) Logical encoding of the magic state. (e) The logical CS-gate with subsequent reset on the control. The detailed circuits for the encoding of the magic state and the logical CS-gate with subsequent reset are shown in Appendix E. The operation R describes qubit reset.

However, a logical S or T gate transforms such an error combination into a different weight-2 error that is not correctable. Therefore, we have to extract the overcomplete set of stabilizers before performing a logical phase gate. This implies that the circuit can be shortened by removing the additional stabilizer extraction if no S or T gate follows before the next error-correction round. In this shortened circuit, the feedback for correcting Z errors is similar to the feedback for correcting X errors. In the following, we refer to this as the *reduced error-correction cycle*.

Typically, when considering more general noise models such as the depolarizing noise model, error-correction protocols come along with more overhead. Here, we give a brief overview of why our error-correction protocol is applicable for biased noise. One typical kind of error preventing fault tolerance is the hook error, where one syndrome qubit is flipped during the syndrome extraction and the error then spreads to several data qubits via the remaining entangling gates in the syndrome extraction. However, since the biased-noise model gives rise only to Z errors after two-qubit gates, hook errors cannot occur. Similarly, failures during the feedback on the syndrome qubits do not have any effect, since Z-type errors commute with CCCZ-gates. Another typical error type consists of errors during the syndrome extraction on data qubits that lead to erroneous corrections. For example, if an X error happens on data qubit 0 during the extraction of the first Z stabilizer this triggers the remaining stabilizers, but the first stabilizer

is not affected, which leads to an erroneous correction of data qubit 5 and thus a weight-2 error. However, for the biased-noise model the only errors that can happen during the extraction of the stabilizers are Z errors, which do not trigger Z stabilizers.

C. T gate with magic state injection

One way to implement a logical T gate on the Steane code is magic state injection. Here, the idea is to prepare a logical auxiliary qubit in a magic state

$$|M_L\rangle = (|0_L\rangle + \exp(i\pi/4)\,|1_L\rangle)/\sqrt{2}, \tag{3}$$

that has imprinted the desired $\pi/4$ phase. The phase is then injected onto the logical qubit by entangling it with the magic state and after measuring the auxiliary logical qubit applying a logical S gate depending on the outcome. This approach is especially suitable for the Steane code with the transversal S gate. To perform magic state injection in a measurement-free manner, one can in principle replace the measurement with subsequent S gate by a logical CS-gate [19]. However, the logical CS-gate is not transversal. Thus, to perform a logical T gate, we have to find a way to encode the magic state in a measurement-free manner and to implement a measurement-free CS-gate. Since the magic state is thrown away after the injection, we can relax the requirements on the measurement-free CS-gate. The schematic circuit for the magic state preparation and the logical CS-gate with subsequent reset on the control qubit is shown in Fig. 2; the detailed circuits are shown in Appendix E.

To fault-tolerantly encode the magic state, we initially encode it non-fault-tolerantly [red box in Fig. 2(d)]. This is then followed by the extraction of all three Z stabilizers (orange box) and a verification step (yellow box). The verification ensures that the prepared state is the magic state $|M_L\rangle$ and not the orthogonal state $Z_L\,|M_L\rangle$. If the state $Z_L\,|M_L\rangle$ was prepared, the verification flag would be raised. The extraction of Z stabilizers is needed, since pairs of weight-1 X and Z errors that can appear during the non-fault-tolerant encoding are transformed into noncorrectable errors by the verification. In a measurement-based scheme one would now measure the syndromes and the verification flag, and then prepare a new magic state if the verification flag was raised or an X error was detected. To make this measurement-free, we always encode a second magic state in a non-fault-tolerant manner, analogously to the first magic state preparation. Furthermore, the information if any X error has occurred is encoded into a flag (the syndrome flag). Finally, we collect the information of the syndrome flag and the verification flag into one new flag that is used to control a logical SWAP-gate on the two magic states. If the syndrome extraction or the verification detects an error, the two magic states are swapped and the second magic state is used for the T gate. The logical SWAP-gate with single-qubit control can be implemented with logical CCZ- and H gates. To reduce the number of required qubits, we first encode the syndrome and verification flags and prepare the final control flag and afterward encode the second magic state as illustrated in Fig. 2.

To perform the CS-gate with subsequent reset, we encode the logical Z-operator $Z_L = Z_4Z_5Z_6$ of the logical magic state qubit into auxiliary qubits [pink boxes in Fig. 2(e)], which are then used to control physical CS-gates [19]. To ensure fault tolerance, every CS-gate is controlled by a freshly encoded auxiliary qubit. In addition, there are two rounds of Z stabilizer measurements (orange boxes) before extracting the logical Z-operator, to detect errors on qubits 4, 5, and 6. If such an error is detected, the information on the auxiliary qubit is flipped (included in the extraction of logical Z in Fig. 2). Resetting one of the auxiliary qubits collapses the magic state into the state $|0_L\rangle$ or $|1_L\rangle$. However, since the magic state injection requires only a classical control anyway, this does not affect the successful implementation of the T gate.

Again, fault tolerance of the T gate with magic state injection with respect to the biased-noise model in Eq. (2) is verified numerically.

A promising alternative to achieve a logical universal gate set is code switching, where one switches between codes with complementary gate sets. As a comparison we simplify the measurement-free code switching protocols presented in Ref. [27] to the biased-noise model in Eq. (2). However, we find that with the noise bias a T gate based on reduced code switching has a substantially lower break-even point than the T gate based on our scheme for magic state injection. Thus, we focus on the magic state injection. Nevertheless, the reduced code switching can be useful for, e.g., the implementation of logical CCX-gates, which require only one round of code switching on every involved logical qubit, but at least four T gates and thus four rounds of magic state injection.

D. Logical-noise model

Next, we analyze the effective noise of the logical building blocks (gadgets). To find the effective errors on the logical qubit, we randomly place errors in a gadget using Monte Carlo sampling (see Appendix B). We then perform the faulty gadget on the test state $(|0_L\rangle + e^{i\pi/8}\,|1_L\rangle)/\sqrt{2}$ for single-qubit gadgets and $(|0_L0_L\rangle + e^{i\pi/8}\,|1_L0_L\rangle + e^{i\pi/8}\,|0_L1_L\rangle - e^{i\pi/4}\,|1_L1_L\rangle)/2$ for two-qubit gadgets. Afterward, we compare the final state with the state one obtains after performing the ideal gadget and deduce the Kraus operators. Note that in general to find the Kraus operators one has to perform state tomography. However, since we only place Pauli errors, the possible final errors in the considered circuits are X, Y, Z, and S-type errors, which can all be clearly distinguished using

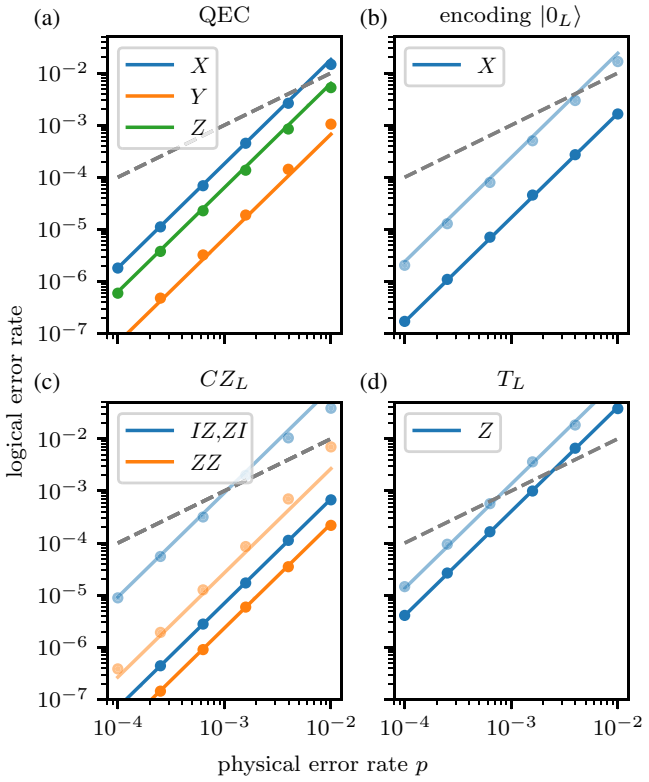

FIG. 3. Characterization of the logical-noise model for (a) the error-correction cycle, and the encoding of (b) $|0_L\rangle$, (c) a logical CZ-gate, and (d) a logical T gate. Here and in the following, the dashed line represents the physical error rate p, to indicate the break-even point. For the encoding and the logical gates the dark lines refer to the bare gate and the light lines to the gate surrounded by error-correction cycles (extended rectangles). The points show the numerically simulated data and lines are the analytical estimates for the logical error rates (see Appendix C). The bare logical CZ- and T gates can only give rise to Z errors. In principle, for the logical CZ-gate and the T gate surrounded by QEC one also finds X and Y-type errors. X and Y-type errors for the extended CZ- and T gate and the noise model for extended H and S gate are shown in Appendix C.

the above state. The rates of these errors for the QEC cycle, the CZ-gate, the encoding of $|0_L\rangle$, and the T gate are shown in dark colors in Fig. 3. In the following, we first discuss the logical-noise model of the error-correction circuit and then summarize the main findings for the encoding, the logical CZ-gate, and the logical T gate.

We find that the error-correction cycle gives rise to X, Y, and Z-type errors. During the correction of X errors the extraction of the Z stabilizers can lead to Z errors while the feedback can result in X errors. During the correction of Z errors the stabilizer extraction gives rise to X errors and the feedback can lead to Z errors. Since we extract one more X stabilizer than Z stabilizers, the probability of X errors during syndrome extraction is higher than the probability of Z errors. Furthermore, if an overcomplete set of stabilizers is used for the feedback an error on a syndrome cannot lead to wrong corrections on data qubits. Thus, the probability of having X errors is higher than the probability of Z errors. Logical Y errors can only appear if there are at least two X errors and two Z errors on the data qubits. In leading order (p^2) this is only the case if one CZ-gate fails during the extraction of the Z stabilizers on both qubits and one CZ-gate during the extraction of the X stabilizers on both qubits. As discussed before, overcomplete stabilizer extraction is not always required. For the reduced error-correction cycle (not shown), where only six stabilizers are mapped out, the probabilities of having a logical X error are reduced with respect to the overcomplete error-correction cycle, while the probability of having a Z error is increased.

The only logical error on the encoding of $|0_L\rangle$ is the X error. Since physical CZ gates can only have Z errors, the bare logical CZ-gate also only gives rise to Z errors. In particular, logical Z errors on both logical qubits are strongly suppressed, since they can only occur if two physical CZ gates fail on both involved qubits. The logical T gate also only introduces Z errors. In any case, the physical CZ- and CS-gates only give rise to Z errors on the data qubits of the logical qubit. On the magic state X errors can appear as well as on the auxiliary qubits during the logical CS-gate. However, the latter lead to wrongly applied S gates on the logical qubit and thus again to Z-type errors, while the former lead with equal probabilities to logical S_L or $S_L^\dagger$ which is equivalent to a noise channel with Kraus operators I_L and Z_L.

So far, we have considered bare logical gates. However, the resulting noise model is not sufficient to estimate the probability of some quantum algorithm to fail on a logical level. The reason is that the correctable weight-1 errors are not accounted for in our logical-noise model. If several gates are performed successively, the weight-1 errors accumulate and can lead to a logical error. The accumulation of errors can be prevented by performing error-correction cycles between the gates. In the worst case, there is an error-correction cycle after each gate and an upper bound for the logical error rates can be estimated simulating the logical-noise model of a so-called extended rectangle including a gadget framed by error-correction cycles [50,51]. As the error-correction cycle that follows a gate is at the same time the error-correction cycle that precedes the next gate, we can subtract the logical error rate of one error-correction cycle from the logical error rate of the extended rectangle to estimate the upper bound on the logical error rates. By default, we use the reduced error-correction cycle to frame the bare gates. However, for the logical T gate the preceding cycle uses an overcomplete set of stabilizers. It depends on the algorithm where and how often error correction cycles are performed and the effective noise per gate lies between the error rates of the bare gates and the extended rectangles. The logical-noise

model including error correction is shown in light colors in Fig. 3.

As expected, the logical error rates for the extended rectangles are higher. In particular, we note that the probability of having a Z error on both logical qubits after a CZ-gate is also increased. This is because such errors can also appear if both preceding error-correction cycles have an XZ error, or one of the preceding error-correction cycles has an XZ error and in addition one physical CZ-gate fails. A detailed analysis of the logical-noise models is given in Appendix C.

In our analysis, we have so far assumed that multi-qubit gates error rates similar to those of two-qubit gates. However, high-fidelity CCCZ-gates have not yet been demonstrated. As a lower bound for the break-even point, we thus derive the break-even point for the QEC cycle and the T gate with all CCZ- and CCCZ-gates decomposed by single- and two-qubit gates [25,27]. We find that the break-even point of the QEC cycle is in this case lowered by a factor of 10, while the break-even point of the T gate decreases by a factor of 4. For the QEC-cycle lower error rates and thus higher break-even points can be achieved using auxiliary qubits to encode the CCCZ-gate (see Ref. [26] and Sec. V). However, these results emphasize that the availability of at least high-fidelity three-qubit gates is crucial for measurement-free quantum error correction.

E. Comparison with measurement-based schemes

Finally, we compare the performance of our measurement-free schemes with a measurement-based approach. Thus, we extend the noise model in Eq. (2) by idling noise and measurement errors. Measurements are performed in the Z basis and thus measurement errors correspond to a flip X before the measurement takes place. We assume measurement errors to occur with a probability $p_{\text{meas}} = 0.4p$ [5]. The dominant errors during idling are Z errors [41]. Since typical durations of gates are several orders of magnitude smaller than the qubit coherence times, idling errors during gates can be neglected [44,45,52,53]. The noise channel for the idling errors during measurements is given by

$$\mathcal{E}_{\text{idle,meas}}(\rho) = (1-p_I)\rho + p_I Z\rho Z. \tag{4}$$

A measurement-based QEC cycle, that is optimized for the biased noise, is obtained by taking the measurement-free version shown in Fig. 2 and replacing the two gate-based feedbacks with measurements and feedforward feedback. Similarly, measurement-based magic state preparation optimized for biased noise is given by non-fault-tolerant encoding of the magic state, followed by Z stabilizer extraction and the encoding of a verification flag. Then, all syndrome qubits and the verification flag are measured and if necessary a second magic state is prepared non-fault-tolerantly. The injection is done in the usual way (see, e.g., Ref. [10]).

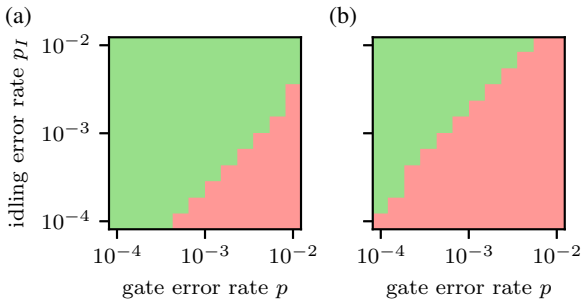

FIG. 4. Comparison of (a) the measurement-free QEC cycle and (b) the T gate with measurement-based schemes. In the green region, the measurement-free schemes have lower logical error rates than the measurement-based version. In the red region measurement-based schemes perform better. The error rates are obtained by summing over the error rates of input states $|0_L\rangle$ and $|+_L\rangle$.

In Fig. 4 we compare the logical error rates of measurement-based and measurement-free schemes for different error rates.

IV. EFFECTS OF IMPERFECT NOISE BIAS

So far we have considered a simplified noise model, where only Z-type errors can happen on two- and multi-qubit gates. In this section we discuss the effects of more general noise models. First, we consider failures on single-qubit gates and afterward we discuss the effect of X and Y errors on two- and multi-qubit gates.

A. Faulty single-qubit gates

In addition to the noise model defined in Eq. (2), we allow X, Y, and Z errors for the single-qubit gates (H, X, T, and $T^\dagger$) with probabilities $p_1/3$. The corresponding noise channel is

$$\mathcal{E}_1(\rho) = (1-p_1)\rho + p_1/3 \sum_{P\in\{X,Y,Z\}} P\rho P. \tag{5}$$

Furthermore, we assume that the qubit initialization also fails with probability p_1. If the initialization fails a qubit is prepared in $|1\rangle$ instead of $|0\rangle$. This is described by the noise channel

$$\mathcal{E}_I(\rho) = (1-p_1)\rho + p_1 X\rho X. \tag{6}$$

We find numerically that all circuits presented in the previous section are still fault tolerant under these conditions. This can be understood in the following way. Typically, fault tolerance is endangered by two- and multi-qubit gates failing simultaneously on data qubits and syndrome qubits

and hook errors during syndrome extraction and magic state verification. While simultaneous errors on two qubits can obviously not be induced by faulty single-qubit gates, hook errors might in principle occur. However, the syndrome extraction consists of one H gate followed by four CZ-gates. Thus, if the H gate or the syndrome initialization fails, the effect on the data qubits is a stabilizer. Any single-qubit error during the magic state verification may result in a logical error on the first magic state, but is then always swapped with the second magic state and the scheme is still fault tolerant.

In Fig. 5 we show the break-even point for different $\alpha = p_1/p$ for the T gate and the QEC cycle. One data point in Fig. 5(b) is obtained in the following way [see also Fig. 5(a)]. We simulate the logical error rates for fixed α and different p for initial states $|0_L\rangle$ and $|+_L\rangle$ [54]. We then fit the sum of the error rates for $|0_L\rangle$ and $|+_L\rangle$ with a function of the form $ap^2 + bp^3$ and evaluate the break-even point, where the logical error rate is smaller than the physical error rate p, with $p_c = (-a + \sqrt{a^2 + 4b})/(2b)$. As expected, the break-even point is shifted to smaller error rates with increasing single-qubit failure rates p_1. The dependence on p_1/p can be estimated in the following way. The probability of having two errors in the circuit is given by $c_{11}p_1^2 + c_{12}p_1 p + c_{22}p^2$, where c_{11} is the number of possibilities that two single-qubit gates fail, c_{12} the number of pairs of errors on a single and one two-qubit gate, and c_{22} the number of errors on two two-qubit gates. The break-even point is then approximately given by

$$p_c = \left(c_{11}\alpha^2 + c_{12}\alpha + c_{22}\right)^{-1}. \tag{7}$$

B. Bit flips on multi-qubit gates

If we allow for X and Y errors on two- and multi-qubit gates, the presented QEC circuit and the T gate are no longer fault tolerant. However, if the probabilities of X and Y errors are significantly smaller than for Z-type errors, our circuits can still suppress the logical error rate. To analyze this quantitatively, we consider the following noise model for two- and multi-qubit gates:

$$\tilde{\mathcal{E}}_l(\rho) = (1-p)\rho + \frac{p(1-\epsilon)}{2^l - 1} \sum_{P \in \{I,Z\}^{\otimes l} \setminus I^{\otimes l}} P\rho P + \frac{p\epsilon}{2^l(2^l-1)} \sum_{P \in \{I,X,Y,Z\}^{\otimes l} \setminus \{I,Z\}^{\otimes l}} P\rho P, \tag{8}$$

where l is the number of qubits involved in the gate and ϵ is the proportion of non-Z-type errors. In the limit of $\epsilon = 0$ we obtain the perfectly Z-biased noise model.

In this case single X errors during syndrome extraction, the verification of the magic state, or feedback can lead to logical errors. However, for small values ϵ our circuits for the QEC cycle and the T gate can still suppress the logical error rate. Furthermore, the logical noise of the T gate for nonzero ϵ is still dominated by Z errors, since the Steane code corrects all types of Pauli errors. In particular, the physical X errors that destroy the fault tolerance of the logical T gate can only lead to logical Z errors. The logical error rates with imperfect noise bias for the QEC cycle and the T gate are shown in Fig. 6 for different ϵ. In addition, we count the number of errors that destroy fault tolerance and estimate the critical values for ϵ, above which no break-even point exists (see Appendix D). We find that the analytically found critical value is around $\epsilon_c = 0.098$ for the QEC cycle and $\epsilon_c = 0.086$ for the T gate, which fits the numerical results.

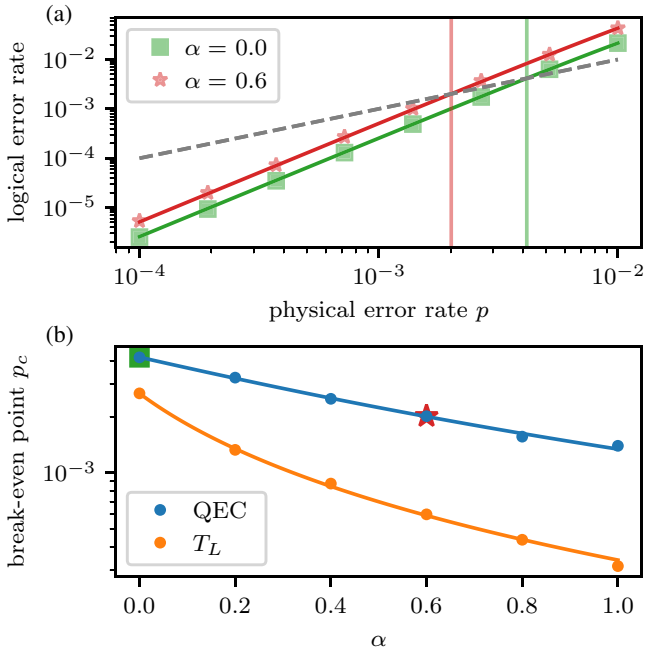

FIG. 5. (a) Exemplary determination of the break-even points for the QEC circuit. (b) The break-even points for the QEC circuit and the T gate for different error rates $\alpha = p_1/p$ of the single-qubit gates. The lines correspond to fits of the form of Eq. (7).

V. IMPLEMENTATION

In this section we exemplarily illustrate efficient implementations of the reduced error-correction cycle and the encoding of $|0_L\rangle$ on a neutral-atom platform. So far, we have assumed all-to-all connectivity. In principle, neutral-atom platforms offer this kind of connectivity due to the possibility of shuttling operations. However, tweezer movements are slow and many shuttling operations can be avoided by carefully arranging the qubits in space. Furthermore, the presented protocols include multi-qubit gates such as the CCCZ-gate. While such gates are natively available on neutral-atom platforms due to the blockade

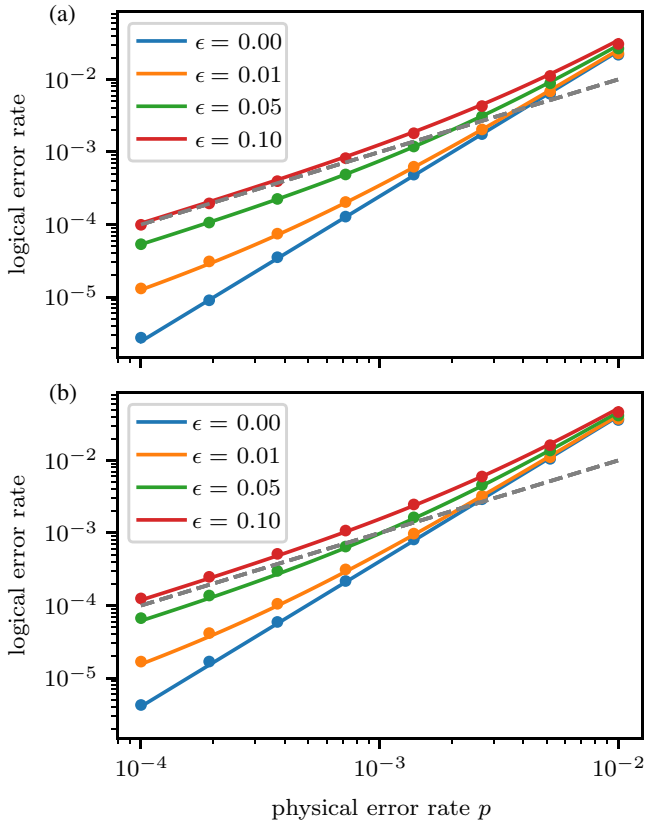

FIG. 6. The logical error rates for the imperfectly biased-noise model as specified in Eq. (8) for (a) the error-correction cycle and (b) the T gate. The shown error rates are obtained by summing over the error rates of input states $|0_L\rangle$ and $|+_L\rangle$. The lines correspond to the analytical estimates for the logical error rates (see Appendix D for the linear order and Appendix C for the quadratic).

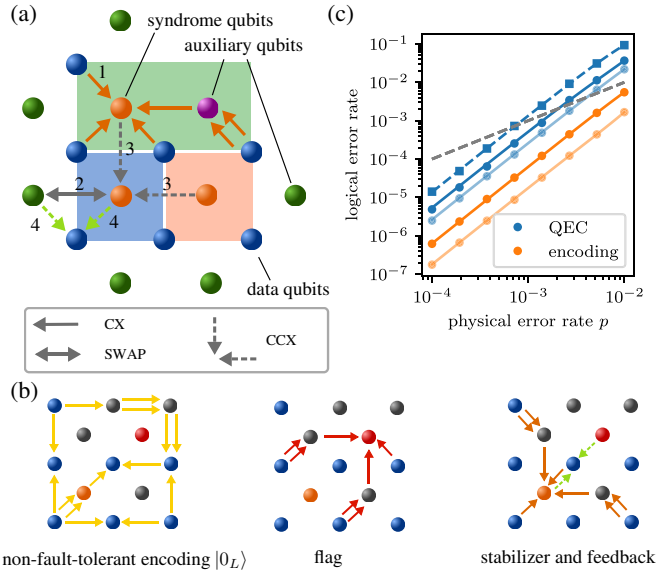

FIG. 7. The implementation of an error-correction cycle (a) and (b) the encoding of $|0_L\rangle$ (b) on a neutral-atom platform with next-nearest-neighbor interaction. The straight lines and arrows represent two-qubit gates (controlled-X, CX), and the dashed arrows represent three-qubit gates (CCX). Two parallel arrows indicate that after encoding the information into stabilizer or flag qubits the entangling gate is applied again to disentangle the auxiliary qubit. For the error-correction cycle this is not shown for steps 2 and 3, to keep the figure clear. However, steps 2 and 3 are always reverted. For the error-correction cycle step 1 (orange arrows) illustrates the extraction of one stabilizer, while steps 2–4 illustrate the feedback on one data qubit. For the encoding, we show the full implementation divided into three parts (non-fault-tolerant encoding, flag extraction, and stabilizer extraction with feedback). (c) Comparison of the logical error rates of the error-correction cycle and the encoding for all-to-all connectivity (light color) and next-nearest-neighbor connectivity (dark color). The dashed curve shows the logical error rate for $p_{\mathrm{CCZ}} = 4.2p$.

mechanism [45,53,55], high-fidelity multi-qubit gates have not yet been realized experimentally. Here, we present possible implementations on a two-dimensional lattice with next-nearest-neighbor interactions, that require at most one shuttling operation and do not require four-qubit gates. The arrangement of the atoms is shown in Fig. 7. The qubits are placed such that most stabilizers can be mapped out without any additional operation.

For correcting X errors first all three Z stabilizers are mapped out into the syndrome qubits [step 1 in Fig. 7(a)]. While the red and the blue stabilizers can be mapped out without any additional operation, the extraction of the green stabilizer requires an intermediate auxiliary qubit, to perform operations between distant qubits. In particular, potential errors on the data qubit in the bottom-right corner of the green stabilizer are copied to the purple auxiliary qubit via a CX-gate [56]. Then, the error information is transferred to the syndrome qubit via another CX-gate. Finally, the auxiliary qubit and the data qubit are disentangled via an additional CX-gate. For the feedback on one data qubit, the syndrome qubit next to the data qubit has to be swapped with an auxiliary qubit (step 2). Then, the syndrome information of the two distant syndrome qubits is encoded into the auxiliary qubit using a next-nearest-neighbor CCX-gate (step 3). Subsequently, a CCX-gate between the auxiliary qubit, the closer syndrome qubit, and the data qubit is applied to perform the correction (step 4). Finally, steps 3 and 2 are reverted. This is repeated for the feedback on all remaining data qubits always with a new (or reset) auxiliary qubit to ensure fault tolerance. The feedback on the data qubit in the middle does not require the SWAP step (step 2); here, the information of the syndrome qubits of the green and red stabilizer is encoded into the orange auxiliary qubit. For the next round of error correction one either resets all auxiliary qubits (including syndromes) or provides fresh qubits via shuttling. Thus, a full error-correction cycle

requires at most one shuttling operation, if resets are not available. However, the implementation of error correction with overcomplete stabilizer extraction might require more shuttling operations.

For the encoding we first encode $|0_L\rangle$ non-fault-tolerantly by entangling data qubits. Here, operations between distant qubits can again be performed using intermediate auxiliary qubits. Then, Z_L is mapped to the red flag-qubit. Finally, the stabilizer $X_0X_2X_4X_6$ is mapped to the orange syndrome-qubit and feedback based on the flag and the syndrome qubit is applied to the data qubit in the middle of the Steane triangle.

The logical error rates for next-nearest-neighbor connectivity (dark color) and all-to-all connectivity with four-qubit gates (light color) are compared in Fig. 7(c). For the QEC cycle, we in addition show the logical error rates for three-qubit gate infidelities of $p_{CCZ} = 4.2p$ [45], where p is the two-qubit-gate infidelity. For the encoding we obtain similar logical error rates for $p_{CCZ} = 4.2p$ and $p_{CCZ} = p$. The logical error rates are higher than for all-to-all connectivity, due to the additional gates required for the next-nearest-neighbor connectivity. However, the break-even points are still in an experimentally realistic regime.

VI. CONCLUSIONS AND OUTLOOK

In this work, we have constructed measurement-free error-correction protocols and a universal gate set for setups, where the noise is dominated by phase errors on two- and multi-qubit gates. The noise bias has enabled us to reduce the qubit and gate overhead compared to previous measurement-free proposals [25–28] and thus to push the break-even point into a regime that is feasible with state-of-the-art neutral-atom experiments. We have analyzed the logical-noise model of the logical qubits as well as the impact of imperfections in the noise bias. For an asymmetric depolarizing noise model we have found that the presented schemes can be used to suppress the error rate if more than 90% of the errors in the two- and multi-qubit gates are Z errors.

In our work we have focused on the Steane code; however, we expect that the discussed protocols can be extended to other low-distance Calderbank-Shor-Steane (CSS) codes. Here, the detailed discussion of the circuit construction with biased noise in Sec. III might serve as instructions to reduce the measurement-free QEC circuit for other codes [25,26] and to introduce generalized measurement-free magic state injection schemes.

Our protocols allow to correct up to one Z or X error on the logical qubits. While this is not sufficient for suppressing errors arbitrarily well, our logical qubits might be used to push the logical error rate below the threshold of a fully fault-tolerant and scalable error-correcting code. The idea is then to use our logical qubits as data qubits for higher-level error-correction protocols. In particular, we want to point out that these protocols include measurement-based error-correction schemes, even if measurements are slow. The reason is that the Steane code can be used to correct any single-qubit Pauli error, including errors that might occur while waiting for measurement results. Thus, the probability of having logical idling errors can also be suppressed. In conclusion, logical qubits encoded in the Steane code together with our platform-specific protocols might be a good starting point for the implementation of arbitrary scalable and universal error-correcting codes.

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DATA AVAILABILITY

The data that support the findings of this paper are openly available [57].

APPENDIX A: DETAILS OF THE BIASED-NOISE MODEL

The ability to have a strong noise bias for two-qubit gates on Rydberg platforms has been discussed in several theory proposals [31,48]. The main idea is that leakage errors can be converted into Z-type errors. In the following we discuss this in more detail.

The fidelities of two- and multi-qubit gates are fundamentally limited by the finite lifetime of the Rydberg state. The ability to entangle qubits and thus the need of interactions between qubits require temporary population of the Rydberg state. However, Rydberg states suffer from decay and thus imprint decay channels on the qubit states. The possible decay processes depend on the encoding of the qubits and the choice of the Rydberg state. For the following discussion we need to distinguish three scenarios:

(a) decay to the qubit state $|0\rangle$
(b) decay to the qubit state $|1\rangle$
(c) decay out of the qubit subspace

In typical implementations of CZ-gates, CP-gates, or CCCZ-gates, only the qubit state $|1\rangle$ has to be coupled to the Rydberg state [52,53]. Thus, for such two- or multi-qubit gates the qubit state $|1\rangle$ decays effectively via the channels discussed above, while the $|0\rangle$-state is not affected. Consequently, decay to the qubit state $|1\rangle$ leads to phase-type errors. In the even that the atom has left the qubit subspace it can be reinitialized in the qubit subspace using, e.g., optical pumping [31] or SWAP-type gate operations [58,59]. The state in which the qubit is reinitialized determines the final effective noise. If it is initialized in a maximally mixed state the noise is described by a depolarizing noise model. However, if the qubit is reinitialized in the state $|1\rangle$, no bit flips have occurred and the only errors that can appear are phase errors, as the qubit has now effectively decayed from the state $|1\rangle$ to the state $|1\rangle$.

Decay to the $|0\rangle$-state leads inevitably to X-type errors and also in the reinitialization imperfections might lead to population of the $|0\rangle$-state and thus to X errors. However, for the example of ^{171}Yb the proportion of errors that are converted to Z errors is expected to be around 98% [48].

APPENDIX B: NUMERICAL SIMULATIONS

For the biased-noise model we verify fault tolerance of all circuits by simulating all possible faulty circuits, where one gate fails. To determine the logical-noise model and the logical error rates (Figs. 3 and 7), we then simulate 10^4 circuits with a minimum of two randomly placed faults.

For the imperfect biased noise (Fig. 6) we know that single faults can already lead to logical errors. Thus, we simulate 10^6 circuits with a minimum of one randomly placed fault.

All simulations are performed using exact state vector simulations in QISKIT [60].

APPENDIX C: DETAILED ANALYSIS OF THE LOGICAL-NOISE MODEL

In addition to the numerical simulations we estimate the logical-noise model analytically. Furthermore, we show the noise model of the CZ-, T, H, and S gates surrounded by QEC cycles.

1. Error-correction cycle

a. Reduced error-correction cycle

Initially, we calculate the error rates on the physical data qubits based on the number of faulty gates they are involved in. Then, we count the number of possibilities of placing two of those single-qubit errors and estimate the logical error rates. We consider the biased-noise model defined in Eq. (2). Technically, there are only Z errors; however, since the correction of Z errors is done by framing the circuit for correcting X errors with H gates, Z errors can be transformed into X errors.

During the simplified error-correction cycle, a single X or Z error on the data qubits happens if a CZ-gate during the syndrome extraction fails on a data qubit (the probability of this is $2/3p$ for the qubits in the corner, $2 \times 2/3p$ for the sides, and $3 \times 2/3p$ for the center of the triangle) or if the feedback gate fails (the probability of this is $8/15$ for all qubits). In addition, an error on the qubits in the corner happens if a syndrome qubit is flipped during the stabilizer extraction ($4 \times 2/3$). Thus, the total probability of having a single X error is $p_c = 58/15p$ for the corner, $p_s = 28/15p$ for the sides, and $p_m = 38/15p$ for the center. There are three possibilities of placing two errors on corners or sides, three of placing one error on a corner and one on a side, and three each of placing one error in the middle and one on a side or a corner. In leading order one then obtains a probability of $p_{X,\mathrm{rQEC}} = 142.5p^2$ of having a logical X error.

The probability of having a logical Z error is smaller, since Z errors that happen during the correction of X errors might be corrected in the second half of the error-correction cycle. Thus we have to subtract all combinations of Z errors that come from the first stabilizer extractions and Z errors during the second feedback and obtain $p_{Z,\mathrm{rQEC}} = 120.1p^2$.

However, some of the discussed error combinations lead to X and Z errors and thus to logical Y errors. Logical Y errors can only happen if there are at least two X and two Z errors on the data qubits. This is only the case if one CZ-gate fails on both qubits during the extraction of the Z stabilizers and one during the extraction of the X stabilizers. The probability for one CZ-gate to fail on both qubits is $p/3$. There are 12 CZ-gates during the extraction of the Z stabilizers and thus 12 possibilities for a single fail, so in total there are 144 possibilities for one fail during X stabilizer extraction and one during Z stabilizer extraction. From this we have to subtract all configurations in which the two Z or X errors cancel out. Errors can cancel out if they happen on the corner of the Steane triangle, so there are three options for having an X or Z error on the corner and four for the corresponding syndrome

to be flipped. Thus, the probability of a logical Y error is $(144 - 2 \times 3 \times 4) \times (p/3)^2 = 13.3p^2$. Subtracting this from the previously estimated probability for a logical X or Z error we obtain the following probabilities for a logical X, Y, or Z error:

$$\begin{aligned} p_{X,\mathrm{rQEC}} &= 142.5p^2 - 13.3p^2 = 129.2p^2, \\ p_{Y,\mathrm{rQEC}} &= 13.3p^2, \\ p_{Z,\mathrm{rQEC}} &= 120.1p^2 - 13.3p^2 = 106.8p^2. \end{aligned} \tag{C1}$$

b. Error-correction cycle

In error correction with overcomplete stabilizer extraction the probability of having an X error due to syndrome extraction on the corner and in the middle is increased ($4/3$ for the corner and $8/3$ for the middle). The probability of having a Z error is reduced, since errors on syndromes only lead to logical errors if there is already a single Z error in the beginning of the Z error correction. It is thus convenient to initially only take into account the probability of having Z errors during the syndrome extraction. The probabilities for single Z errors are then $p_c = 2/3$, $p_s = 4/3$, and $p_m = 2$ and the probability of a logical Z error is then $26.7p^2$. In addition a logical Z error can appear if two CCCZ-gates in the feedback fail. The probability of this is $21(8/15)^2p^2$. And finally, if there is a Z error on the side (in the middle) of the triangle there are two (three) possibilities, where an additional error on the syndromes leads to a logical error. This gives an additional $37.3p^2$. In total, we thus obtain $70p^2$. Again, we have not yet taken Y errors into account. Logical Y errors appear only if during the first and during the second round of stabilizer extraction a CZ-gate fails on both qubits. Since with the overcomplete stabilizer extraction logical Z errors are less likely, we initially determine the probability that two failing CZ-gates give a logical Z error. As discussed before this can only happen if the first Z error is on the side or in the middle of the triangle, which gives a probability of $37.3/4p^2$. [Here the factor of $1/4$ comes in; since this time we only allow for errors on both qubits, that happens with a probability of $1/3p$, while previously we also allowed for errors on one qubit $(2/3p)$.] From this we have to subtract the probability of having two X errors on the same corner, which is $24/9p^2$. Finally we obtain

$$\begin{aligned} p_{X,\mathrm{QEC}} &= 181.7p^2, \\ p_{Y,\mathrm{QEC}} &= 6.7p^2, \\ p_{Z,\mathrm{QEC}} &= 63.3p^2. \end{aligned} \tag{C2}$$

2. Encoding

For the encoding of logical $|0_L\rangle$ we first note that only X errors have a nontrivial effect on the encoded logical state. Since physical CZ- and CCZ-gates only give rise to Z errors, the only data qubits that can have an X error are qubits 0, 1, 3, and 5 where an H gate is performed after a CZ- or CCZ-gate. The probability of an X error on qubit 0 is $2 \times 2/3p + 4/7p$ and for qubits 1, 3, and 5 the probability is $2 \times 2/3p$. There are three possibilities of placing two errors on qubits 1, 3, and 5 and two possibilities of placing one error on qubit 1 or 5 and one on qubit 0. Errors on qubits 3 and 0 cancel out. Thus, the probability of having a logical X error after the bare non-fault-tolerant encoding is approximately $10.6p^2$. Furthermore, a logical X error appears if there happens to be an error on qubit 3 and in addition the verification flag or the syndrome is flipped. The probability of this is $6.2p^2$; thus the probability of having a logical error in the encoding is

$$p_{X,\mathrm{Enc}} = 16.8p^2. \tag{C3}$$

3. CZ-gate

For the logical CZ-gate a logical error on only one logical qubit happens if two gates fail either on the same qubit or one gate fails on one qubit and one gate on both. For the first case there are 21 possibilities with probability $p^2/9$, while for the last case there are 42 possibilities with probability $p^2/9$. The total probability of a logical ZI error or IZ-error is thus

$$p_{ZI,\,\mathrm{CZ}} = 63/9p^2 = 7p^2. \tag{C4}$$

The probability of a logical Z error on both logical qubits is smaller, since the only possibility is that two physical CZ-gates fail on both qubits. Thus, there are 21 possibilities with probability $p^2/9$ and the probability of a logical ZZ-error is

$$p_{ZZ,\,\mathrm{CZ}} = 7/3p^2. \tag{C5}$$

4. *T* gate

Logical errors during the T gate with magic state injection can appear in the following way. Either errors happen directly on the logical state if one of the CZ- or CS-gates fail or errors that happen on the magic qubit imply errors on the logical state.

We start with the effects that errors on the magic qubit have on the logical qubit. Z errors on the magic state flow to the logical qubit via the logical CX operation in the beginning of the injection and thus directly translate into Z errors on the logical qubit. Logical X and Y errors on the magic state (also during the logical CX-gate in the injection) imply a wrongly applied logical S_L if the magic qubit is in $|0_L\rangle$ and a logical $S_L^\dagger$ if the magic qubit is in $|1_L\rangle$. After tracing out the magic qubit this leads to a logical-noise channel with Kraus operators $\mathrm{I}_L/\sqrt{2}$ and $\mathrm{Z}_L/\sqrt{2}$ on the logical qubit. Flips on the two flags during the logical CS-gate with subsequent reset and a single X error on the

magic state data qubits 4, 5, or 6 in combination with an X error on one of those flags have the same effect.

Taking into account the previous considerations and the fact that the CZ- and the CS-gates give only rise to Z errors, the logical T gate can only have Z errors. The probability of a logical Z error is given by half the probability of having a logical X error on the magic state and the probability of having a weight-2 Z error during the magic state preparation and injection. In the following we derive both probabilities.

Single X errors on the magic state can appear after the CX-gate with probability $2/3p$, after the controlled-SWAP-(CSWAP) gate with probability $2/3p$ and in the verification with probability $1/3p$. For the verification we do not count errors where the gate fails on both qubits, since this results in a raised flag. However, if two gates during the verification fail on both qubits the flag is flipped twice and the logical qubit has a logical X error. Thus, we have to add an additional $21/9p^2$. The total probability of having a single X error on the magic state is thus $(2/3 + 4/3 + 1/3)p = 7/3p$. Finally, to flip one of the flags in the logical CS-gate with subsequent reset either an error has to happen on the syndrome qubits for $Z_0Z_1Z_2Z_3$ and $Z_0Z_1Z_5Z_6$ or during the encoding of the flag. The probability of such a flip is thus $(4 \times 2 \times 2/3 + 8/15)p = 98/15$. In summary, the probability of a weight-2 X or Y error on the magic qubit is then

$$p_{X,M} = \left(21\left(\frac{7}{3}\right)^2 + \left(\frac{98}{15}\right)^2 + 2 \times 3\frac{7}{3}\frac{98}{15} + \frac{21}{9}\right)p^2 \approx 251p^2. \tag{C6}$$

Single Z errors on the logical qubit can appear after the CZ- and CS-gate each with a probability of $2/3p$. Another possibility for having Z-type errors on the logical qubits is an accidental flip of one control qubit that controls the CS-gate. The probability of this is $0.5(3 \times 2/3 + 4/7)p$, where the factor of 0.5 comes in because a wrongly applied S is only half a Z error. Furthermore, logical Z errors on the magic state appear during the CSWAP-type feedback with a probability of $4/7p$ and in the verification with a probability of $1/2 \times 1/3p$. Again, for the verification we only have to count errors that happen on both qubits, if two such errors happen, since otherwise the flag is raised. However, weight-2 errors in the verification give also always rise to logical X errors and are thus already taken into account. Similarly, Z errors on both qubits during the CZ-gate in the injection lead to logical X errors. Thus, we have to subtract $(1 + 1/4) \times 21/9p^2$ from the final end result. A single Z error during the syndrome extraction in the magic state preparation raises the flag and thus does not matter. However, a logical error during the syndrome extraction can appear with probability 26/3. The probability of having a single Z error on one data qubit is thus $(2/3 + 2/3 + (3 \times 2/3 + 4/7)/2 + 4/7 + 1/6)p \approx 3.36p$ and the probability of having a weight-2 Z error is as follows:

$$p_{Z,a} = \left(21 \times 3.36^2 - 1.25 \times \frac{21}{9} + \frac{26}{3}\right)p^2 \approx 242p^2. \tag{C7}$$

Last but not least, logical Z errors on the magic state can appear if the second non-fault-tolerant magic state encoding fails and in addition the flag for doing the SWAP is raised. There are only two error positions in the non-fault-tolerant encoding that can lead to a logical Z error and the probability is thus $4/3p$. The flag is raised if there is a single Z error during the first encoding ($11p$), if there is a single Z error during the Z stabilizer extraction on the data qubits ($12 \times 1/3p$), if there is an error on the syndrome qubits ($12 \times 2/3p$), if there is an error on the ancilla in the verification ($7 \times 2/3p$), or during the final flag encoding ($3 \times 8/15p$). Errors on data qubits during the X-syndrome extraction count only half, since they raise the flag in only half of the runs. The total probability for this scenario is then

$$p_{Z,b} = \left(11 + \frac{12}{3} + \frac{24}{3} + \frac{14}{3} + \frac{24}{15}\right)\frac{4}{3}p^2 \approx 39p^2. \tag{C8}$$

In summary a logical Z error appears after a logical T gate with a probability of

$$p_{Z,T} = (p_{X,M}/2 + p_{Z,a} + p_{Z,b})p^2 \approx 406p^2, \tag{C9}$$

where the factor of $1/2$ comes in since a logical X error on the magic state implies a logical Z error on the logical qubit only half of the time.

5. Extended rectangles

To determine the error probabilities of the extended rectangle, we use the coefficients determined above and combine their square roots to estimate the error rates of the extended rectangles. Here, the idea is that the number of possibilities of placing two errors in a circuit is roughly given by the number of possibilities of placing one error multiplied with itself. We first estimate analytical values for the curves shown in Fig. 3 and afterward discuss logical X- and Y-type errors that occur for the logical CZ-, T, H, and S gates surrounded by QEC cycles, but that do not originate from the bare gates.

For the extended encoding we then obtain

$$p_{X,\mathrm{extEnc}} = (\sqrt{p_{X,\mathrm{Enc}}} + \sqrt{p_{X,\mathrm{rQEC}}})^2 \approx 239.5p^2. \tag{C10}$$

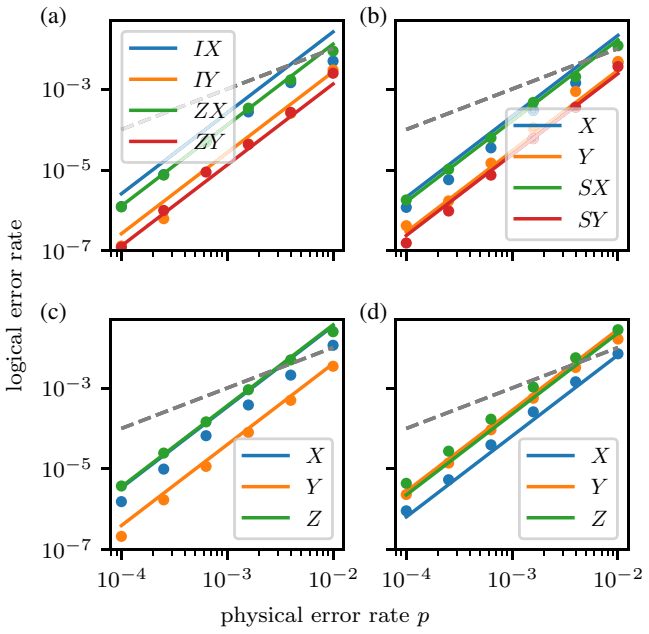

FIG. 8. Characterization of the logical-noise model for (a) the logical CZ-gate, CZ_L, (b) the logical T gate, T_L, (c) the logical H gate, H_L, and (d) the logical S gate, S_L, surrounded by QEC. The points show the numerically simulated data and the lines are the analytical estimates for the logical error rates. For the CZ- and T gates, Z-type errors are shown in Fig. 3. Thus, we do not show them again.

For the extended CZ-gate we obtain

$$\begin{aligned} p_{ZI,\mathrm{extCZ}} &= (2\sqrt{p_{Z,\mathrm{rQEC}}} + \sqrt{p_{ZI,\,\mathrm{CZ}}})^2 \\ &\quad + (\sqrt{p_{X,\mathrm{rQEC}}} + \sqrt{p_{Y,\mathrm{rQEC}}}) \\ &\quad \times (\sqrt{p_{Z,\mathrm{rQEC}}} + \sqrt{p_{Y,\mathrm{rQEC}}} + \sqrt{p_{ZI,\,\mathrm{CZ}}}) \\ &\quad - p_{Z,\mathrm{rQEC}} \\ &\approx 936.144p^2, \\ p_{ZZ,\mathrm{extCZ}} &= (\sqrt{p_{Y,\mathrm{rQEC}}} + \sqrt{p_{ZZ,\,\mathrm{CZ}}})^2 \approx 26.8, \end{aligned} \tag{C11}$$

where we also take into account that X errors on data qubits lead to Z errors on the data qubits of the other logical qubit after the CZ-gate.

For the extended T gate we use

$$\begin{aligned} p_{Z,\mathrm{extT}} &= (\sqrt{p_{Z,\mathrm{rQEC}}} + \sqrt{p_{Z,\mathrm{QEC}}} + \sqrt{p_{Z,T}})^2 - p_{Z,\mathrm{rQEC}} \\ &\approx 1372.28p^2. \end{aligned} \tag{C12}$$

In Fig. 8 we show the probability for X- and Y-type errors to occur in the extended rectangle CZ- and T gates and the logical-noise model of the extended logical H and S gates.

For the CZ-gate a logical X error in the first QEC round leads to a logical Z error on the other logical qubit. In Fig. 8 we refer to this as ZX; similarly a logical Y error before the bare logical CZ-gate leads to ZY. Thus, we find

$$\begin{aligned} p_{ZX,\mathrm{extCZ}} &= p_{X,\mathrm{rQEC}}, \\ p_{ZY,\mathrm{extCZ}} &= p_{Y,\mathrm{rQEC}}. \end{aligned} \tag{C13}$$

A single physical X error before the CZ-gate will not affect the logical information of the other qubit and thus can only give IX-type errors, if in addition an X error happens during the second round of error correction. Similar arguments hold for IY. We thus estimate the probability for IX and IY errors as

$$\begin{aligned} p_{IX,\mathrm{extCZ}} &= 2p_{X,\mathrm{rQEC}}, \\ p_{IY,\mathrm{extCZ}} &= 2p_{Y,\mathrm{rQEC}}, \end{aligned} \tag{C14}$$

where the factor of 2 accounts for the fact that the number of possibilities of placing two errors in two different parts of the circuit is twice the number of possibilities one has when placing them in the same part, since in the first case they are distinguishable while in the second case they are not. However, our analytical approximations of $p_{IX,\mathrm{extCZ}}$ and $p_{IY,\mathrm{extCZ}}$ seem to overestimate the logical error rates (see Fig. 8). The reason is that some of the single physical X errors that occur during the first round of QEC might be corrected in the second round of QEC, before weight-2 errors can accumulate.

As expected, the T gate transforms logical X errors into SX type errors and logical Y errors into SY-type errors. Naively one would thus assume that error rate for logical SX errors (SY errors) is given by the probability of having an X error (Y error) in the QEC cycle. However, our realization of the logical T gate transforms combinations with one physical X error and one physical Y error half of the time into a logical SX error and half of the time into a logical SY error. The logical error rates for SX and SY errors can be approximated as

$$\begin{aligned} p_{SX,\mathrm{extT}} &= p_{X,\mathrm{QEC}} - \sqrt{p_{X,\mathrm{QEC}}p_{Y,\mathrm{QEC}}}/2 \\ &\approx 164.305p^2, \\ p_{SY,\mathrm{extT}} &= p_{Y,\mathrm{QEC}} + \sqrt{p_{X,\mathrm{QEC}}p_{Y,\mathrm{QEC}}}/2 \\ &\approx 24.069p^2. \end{aligned} \tag{C15}$$

X and Y errors can occur if two X and Y-type errors occur in the second error-correction round or if one appears in the first and one in the second. Since we always subtract the probability that one error-correction cycle will fail, we only have to count the combinations, where one error has happened in the first QEC cycle and one in the second. The T gate transforms physical X errors into SX errors which corresponds to a equal-weight superposition of an X and an Y error and similarly for incoming physical

Y errors. Logical Y errors occur only if the final errors are two Y errors and the probabilities can thus be estimated as

$$\begin{aligned} p_{X,\mathrm{extT}} &= (\sqrt{p_{X,\mathrm{QEC}}} + \sqrt{p_{Y,\mathrm{QEC}}})\sqrt{p_{X,\mathrm{rQEC}}} \\ &\quad + (\sqrt{p_{X,\mathrm{QEC}}} + \sqrt{p_{Y,\mathrm{QEC}}})\sqrt{p_{Y,\mathrm{rQEC}}}/2 \\ &\approx 211.874p^2, \\ p_{Y,\mathrm{extT}} &= (\sqrt{p_{X,\mathrm{QEC}}} + \sqrt{p_{Y,\mathrm{QEC}}})\sqrt{p_{Y,\mathrm{rQEC}}}/2 \\ &\approx 29.3244p^2. \end{aligned} \tag{C16}$$

The H gate transforms X errors into Z errors and vice versa. Thus, the probability of having logical X, Y, and Z errors in the extended logical H gate can be estimated as follows:

$$\begin{aligned} p_{X,\mathrm{extH}} &= (\sqrt{p_{Z,\mathrm{rQEC}}} + \sqrt{p_{X,\mathrm{rQEC}}})^2 - p_{X,\mathrm{rQEC}} \\ &\approx 341.653p^2, \\ p_{Y,\mathrm{extH}} &= (\sqrt{p_{Y,\mathrm{rQEC}}} + \sqrt{p_{Y,\mathrm{rQEC}}})^2 - p_{Y,\mathrm{rQEC}} \\ &\approx 39.999p^2, \\ p_{Z,\mathrm{extH}} &= (\sqrt{p_{X,\mathrm{rQEC}}} + \sqrt{p_{Z,\mathrm{rQEC}}})^2 - p_{Z,\mathrm{rQEC}} \\ &\approx 364.053p^2. \end{aligned} \tag{C17}$$

Again, our analytical approximation slightly overestimates the logical error rates for logical X errors, since we do not account for possible corrections of single physical errors in the second round of QEC.

The S gate transforms X errors into Y errors and vice versa. Thus, the probability of having logical X, Y, and Z errors in the extended logical H gate can be estimated as follows:

$$\begin{aligned} p_{X,\mathrm{extS}} &= (\sqrt{p_{Y,\mathrm{QEC}}} + \sqrt{p_{X,\mathrm{rQEC}}})^2 - p_{X,\mathrm{rQEC}} \\ &\approx 65.3575p^2, \\ p_{Y,\mathrm{extS}} &= (\sqrt{p_{X,\mathrm{QEC}}} + \sqrt{p_{Y,\mathrm{rQEC}}})^2 - p_{Y,\mathrm{rQEC}} \\ &\approx 280.149p^2, \\ p_{Z,\mathrm{extS}} &= (\sqrt{p_{Z,\mathrm{QEC}}} + \sqrt{p_{Z,\mathrm{rQEC}}})^2 - p_{Z,\mathrm{rQEC}} \\ &\approx 227.723p^2. \end{aligned} \tag{C18}$$

APPENDIX D: ANALYTICAL ARGUMENTS FOR IMPERFECT BIASED NOISE

Here, we estimate the critical values for the noise bias ϵ.

1. Error-correction cycle

a. Reduced error-correction cycle

In the reduced error-correction cycle there are four possible scenarios, where X or Y errors on one physical gate lead to a logical X or Z error. In the following we discuss the possibilities of causing logical X errors. For symmetry reasons, the probabilities of having logical Z errors are the same.

The first scenario are flips of the syndrome qubits during the stabilizer extraction that lead to hook errors. For each stabilizer extraction block the critical CZ-gates are the second and the third. (the second if there is no Z error on the involved data qubit and the third if there is a Z error on the involved data qubit). In both cases the probability of one CZ-gate having such an error is approximately $1/3\epsilon p$. In total there are three stabilizer extraction blocks, where hook errors imply logical X errors and thus the probability of a logical X error due to hook errors is $2\epsilon p$.

The second scenario is X errors on the data qubits (but not the syndromes) during the extraction of the Z stabilizers that lead to wrong syndromes and thus to wrong corrections. Errors during the extraction of the last stabilizer do not matter. During the extraction of the second stabilizer there are only two qubits, that are also involved in the extraction of the last stabilizer, and in the first stabilizer there are three qubits (all except the corner) that are also involved in the extraction of the other stabilizers. The probability of one CZ-gate having an X or Y error on the data qubit is $1/4\epsilon p$ and thus the probability of a logical error due to the second scenario is $5/4\epsilon p$.

The third scenario is X errors on the data qubits in combination with flips of the syndromes that can appear during the stabilizer extraction. Here, during the first extraction errors do not matter, while during the extraction of the second stabilizer there are two problematic CZ-gates and during the extraction of the third stabilizer there are three. Thus, the probability of a logical error due to the third scenario is $5/4\epsilon p$.

The last scenario consists of flips on the syndrome qubits during the feedback, that lead to wrong corrections. If the gate that flips the syndromes at the same time also fails on the involved data qubit this results in a logical error. If the first feedback gate fails there are six possibilities for syndrome flips that imply a wrong correction. For the second feedback gate there are five possibilities, for the third feedback gate four, and so on. The total probability for a logical X error due to the third scenario is then $21/15\epsilon p$. In total the probability of a logical X error as well as a logical Z error is thus $5.9\epsilon p + \mathcal{O}(p^2)$ and the probability of having any logical error is $11.8\epsilon p + \mathcal{O}(p^2)$. Thus, the critical value for ϵ is $\epsilon_c \approx 0.084$.

b. Error-correction cycle

For error correction with overcomplete stabilizer extraction the probability of hook errors is $4 \times 2/3\epsilon p$. However, there are only two problematic X errors on the data qubits during the extraction of the Z stabilizers and thus the probability for a logical error during each of the second and third scenarios is $\epsilon p/2$. Furthermore, during the feedback

TABLE I. The number of two- and multi-qubit gates required for the different circuits with all-to-all connectivity (rows 1–5) and next-nearest-neighbor (nnn) connectivity (rows 6 and 7).

	CZ	CCZ	CCCZ	CP	Qubits
Reduced QEC	24	0	14	0	10
Overcomplete QEC	28	0	14	0	11
Logical T gate	95	29	3	7	22
Magic encoding	41	22	1	0	15
Logical CS with subsequent reset	47	7	2	7	19
nnn reduced QEC	92	42	0	0	17
nnn encoding	29	1	0	0	13

there are only three problematic errors during the first CCCZ-gate, two during the second and third, and one during the fourth. The probability of a logical error during the feedback is thus $3/5\epsilon p$. In total the probability of a logical error is then $(5.9 + 4.266)\epsilon p + \mathcal{O}(p^2) \approx 10.17\epsilon p + \mathcal{O}(p^2)$ and the critical value for ϵ is $\epsilon_c \approx 0.098$.

2. *T* gate

For the T gate with magic state injection we initially consider the magic state preparation. First, we note that now weight-2 Z errors, that are not detected by the verification, can appear if in the non-fault-tolerant encoding of the magic state a physical CZ-gate has an X-Z error. The probability of this is $9/12$. Next, we consider hook errors during the extraction of the Z stabilizers and note that Y errors on the syndrome trigger the flag as well, so the only problematic errors are X errors on syndromes, which appear with a probability of $2/6\epsilon p$. Thus, the contribution is $3 \times 2/6\epsilon p = \epsilon p$. Hook errors in the verification lead to logical X errors, which as discussed in Appendix C give rise to logical Z errors in the injection with a probability of 50%. Errors during the last gate in the verification do not matter and again, only X errors have to be counted, as Y errors also raise the flag. In summary, the contribution from the verification is thus $0.5 \times 6 \times 2/6\epsilon p = \epsilon p$. In the CSWAP-type feedback, errors on the control between the second and fifth swap lead to X errors on the data qubits if the two qubits participating in the swap are in different states, which is roughly the case half of the time. The probability of one CSWAP (disassembled into three CCZs and one H) flipping the control qubit is $3 \times 4/7\epsilon p$ and the total contribution from the CSWAP-type feedback is $0.25 \times 5 \times 3 \times 4/7\epsilon p \approx 2\epsilon p$, where the second factor of $1/2$ stems from the fact that logical X errors on the magic state imply a logical Z error on the data qubits for only half of the time.

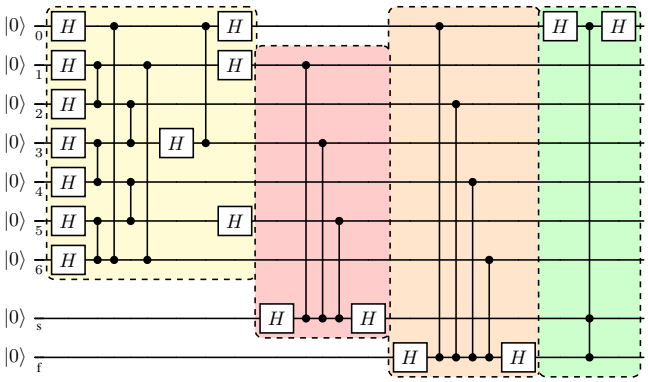

FIG. 9. The circuit for encoding logical zero on the [[7, 1, 3]] Steane code [25].

During the logical CS-gate with subsequent reset logical errors occur if qubit 4, 5, or 6 is flipped during the syndrome extraction or the extraction of Z_L. Both lead again to an S-type logical error on the logical qubit and thus lead to a logical error only half of the time. In each round of syndrome extraction there are five gates where such a flip can happen. During the second round the probability for such a flip is $2/3\epsilon p$ and during the first round it is $1/2\epsilon p$, since here the combination of a Y error on the data qubit and a Z error on the syndrome qubit is still correctable via the two flags. The total contribution from the syndrome extraction is thus $0.5 \times 4 \times (2/3 + 1/2)\epsilon p = 2.34\epsilon p$.

A flip during the last round of Z_L extraction does not matter; a flip in the round before gives a weight-1 and thus correctable error and a flip in the fifth round gives a weight-2 S-type error and thus only $1/4$ logical error. Flips in rounds 1–4 lead to a logical S error. The contribution

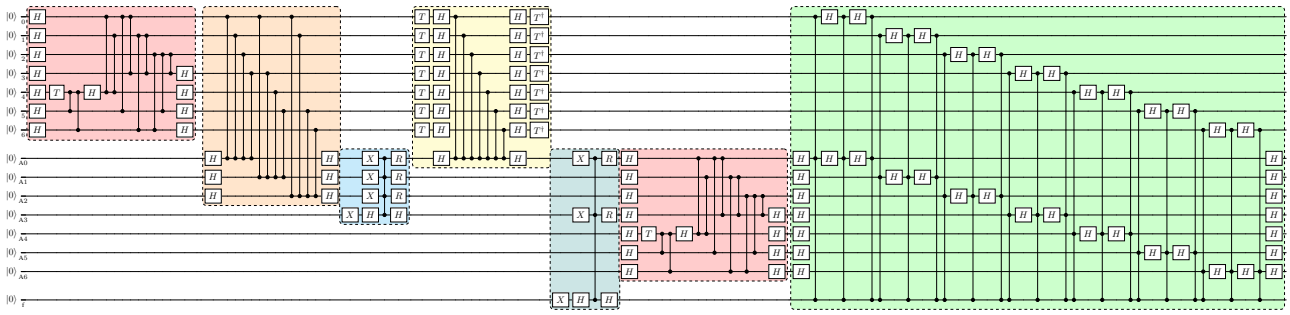

FIG. 10. The circuit for magic state encoding. The colors are chosen to fit Fig. 2.

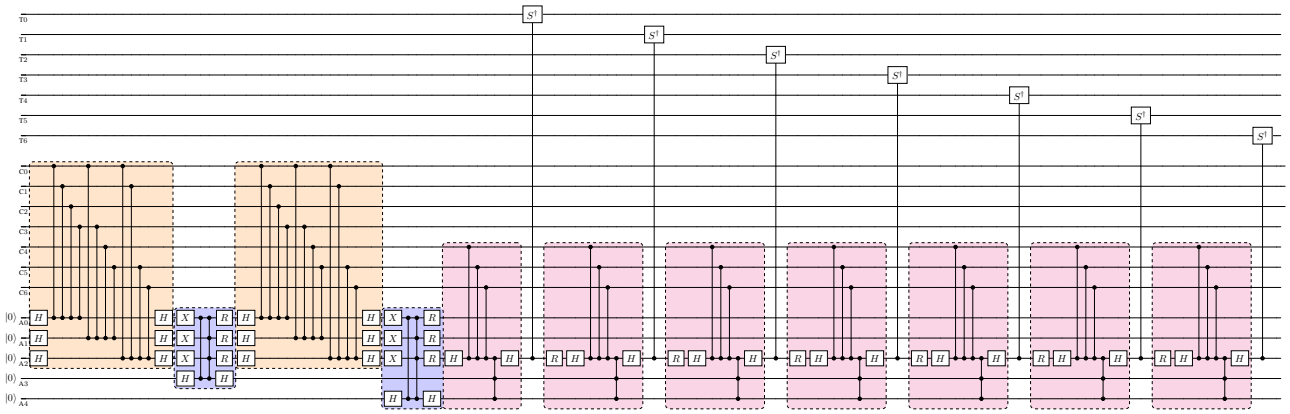

FIG. 11. The circuit for the logical CS-gate with subsequent reset on the control. The colors are chosen to fit Fig. 2.

from logical Z extraction is thus $0.5 \times 4 \times 3 \times 2/3\epsilon p + 1/4 \times 3 \times 2/3\epsilon p = 4.5\epsilon p$.

The total probability of a logical error during the T gate is then $11.5\epsilon p + \mathcal{O}(p^2)$. Thus, the estimated critical value for ϵ is $\epsilon_c \approx 0.86$.

APPENDIX E: RESOURCES AND CIRCUITS

Table I lists the number of two- and multiqubit gates required for the different circuits. In Fig. 9 we show the full circuit for encoding $|0_L\rangle$ on the Steane code, Fig. 10 shows the full circuit for magic state encoding, and Fig. 11 shows the full circuit for the logical CS-gate.

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accounted with both input states, such that the final result again gives an upper bound for the logical error rates.

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