Journal of Applied Physics ARTICLE pubs.aip.org/aip/jap

Full factorial analysis of gradual switching in thermally oxidized memristive devices

Cite as: J. Appl. Phys. **135**, 234901 (2024); doi: 10.1063/5.0214036
Submitted: 15 April 2024 · Accepted: 3 June 2024 ·
Published Online: 17 June 2024

View Online Export Citation CrossMark

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ABSTRACT

Memristive devices are promising candidates for synaptic memories in neuromorphic computing systems, but the insufficient reliability of the analog behavior has been a challenge. Lateral oxide scaling with bottom-up technologies such as thermal oxidation, coupled with new device architectures, can improve the reliability. However, the effect of thermal oxide growth on analog device behavior remains unclear. In this study, we fabricate a variety of resistive switching thermal oxides on tantalum electrode surfaces and develop a method for rapid full factorial electrical analysis. The analysis uses 2500 unique control parameter combinations of current limits and RESET-stop-voltages to compare device behavior across millions of modulated current–voltage sweeps. We clarify the mechanisms that shift the device behavior from abrupt towards gradual SET transitions, a desirable characteristic for emulating analog plasticity. We found that a mildly negative differential resistance and an increased internal series resistance at the metal–oxide interface contribute to the stabilization of the gradual SET transitions. These findings highlight the importance of fine-tuning the bottom-up oxide growth for improving switching performance.

I. INTRODUCTION

The transistor count within a processing unit has historically served as a key metric for evaluating computing performance. Recently, the rise of tasks related to artificial intelligence has triggered a paradigm shift from computing to memory-intensive demands, necessitating advancements in large-scale data processing. Performing these complex tasks with a conventional von Neumann architecture requires transfer of large amounts of data between the physically separated processing and memory units. The resulting memory transfer latency and power demand predominantly limit future computing performance, rather than merely transistor count.[1–5] Neuromorphic systems aim to alleviate this inherent bottleneck by mimicking the close interconnection of processing and memory in the energy-efficient human brain.[6,7]

Memristive devices, based on resistive switching random access memory (ReRAM), emulate the synaptic plasticity by analog weight updating. Oxide-based valence-change-mechanism (VCM) devices are a prominent candidate, enabling the conductance modulation of an oxygen-deficient filamentary region by voltage application.[8–10] Analog in-memory computing with memristive device arrays requires the device's conductance to be tunable in a continuous range of values.[11–14] Unfortunately, these filamentary devices tend to have an abrupt SET transition from the high-resistance-state (HRS) into the low-resistance-state (LRS) that occurs within less than 10 ns.[15–18] This abrupt transition is difficult to control, typically resulting in binary conductance states. Achieving stable analog behavior that is resilient to variations of electrical control parameters is critical for developing performant neuromorphic hardware.

Integration of these memristive devices in neuromorphic hardware is significantly hindered by reliability challenges.[19–22] Improvements in reliability have been shown by laterally scaling the switching oxide.[23–25] However, conventional top-down technologies face oxide scalability challenges, which can be addressed through the combination of new device architectures with bottom-up technologies. These architectures often rely on local oxidation of electrode surfaces for the fabrication of filamentary VCM devices. Nano-scaling approaches using bottom-up oxide growth

are demonstrated in architectures utilizing three-dimensional integration,[24,26] via scaling[27–29] and sidewall technology.[23]

Despite the extensive study of thermal oxidation of tantalum at larger oxide thicknesses,[30–33] the effects on memristive device properties with around 5 nm thin thermal oxides remain unclear. Additionally, recent studies using ultra-thin thermal oxides for nano-scaled device architectures demonstrate a proof-of-concept for abrupt binary switching in these devices, but predominantly adopt a heuristic approach to determine arbitrary oxidation conditions.[23,24,26–29]

These architectures often involve chemical–mechanical polishing (CMP) in ambient atmosphere, causing inherent native oxidation of the ohmic electrodes with high oxygen affinity. The consideration of this preceding native oxidation for bottom-up growth of ultra-thin oxides is essential but often disregarded for optimizing memristive device properties.

In this study, we analyze the bottom-up growth of ultra-thin tantalum oxide layers specifically for their application in memristive devices, with a focus on having a preceding native oxidation. We develop a comprehensive full factorial electrical analysis method to evaluate selected thermal oxides for their analog switching properties across a large range of electrical control parameters. This approach enables us to clarify the underlying mechanism of stabilizing the desired analog SET transitions. Complementary analysis of gradual RESET transitions reveals additional advantages in minimizing resistance state write-variability.

II. METHODS

A. Sample fabrication

In this study, we fabricated two kinds of samples: Devices for oxide characterization (capacitance, leakage current, and forming voltage) and devices for full factorial analysis of resistive switching properties. The former consists of a sputter-deposited planar electrode stack of titanium nitride (TiN) and tantalum (Ta), with selectively exposed TiN for contact to the bottom electrode. The Ta layer had a minimum thickness of at least 30 nm, preventing full oxidation in subsequent processing. A native oxide was allowed to develop over a minimum period of two days under ambient atmospheric conditions. Subsequently, rapid thermal annealing (RTA) was used for thermal oxidation of the Ta surface at various temperatures and durations in a dry oxygen atmosphere. The samples that we describe as "without native oxide" were processed by thermal oxidation approximately within 5 min of Ta sputter-deposition. The device fabrication was completed by the sputter-deposition of a lithographically scaled $50 \times 50\,\mu m^2$ platinum (Pt) top contact pad, serving as the 30 nm thick active electrode.

For the full factorial analysis, devices were scaled down to a $2 \times 6\,\mu m^2$ crossbar design to minimize parasitic capacitance and leakage current. These devices consist of a 6 μm Ta electrode stripe covering a 2 μm-wide Pt bottom electrode. After native oxide formation and thermal oxidation of the Ta surface, a 2 μm Pt active electrode was sputter-deposited to form a crossbar configuration.

B. Oxide characterization

Layer thicknesses were measured and analyzed using x-ray reflectometry (XRR) on a Panalytical MPD Pro system, with the built-in software package X'Pert Reflectivity, on a Si/SiO_2(400 nm) substrate. Capacitance of our $50 \times 50\,\mu m^2$ devices was measured with a HP4284A LCR-Meter at a small signal frequency of 10 kHz and a voltage amplitude of 50 mV. Leakage measurements were performed with a Keithley 6430 and a Femto PreAmp current amplifier with voltage sweeps ramping between 0.2 and −0.2 V. For highly insulating oxides, a slow sweep duration of 104 s was adopted to minimize capacitive charging current. Pristine resistance was determined by fitting a linear regression to the slope of the I–V sweep for voltages between 0.05 and −0.15 V. The asymmetric voltage range aims to exclude capacitive charge current effects caused by directional change of voltage ramping at the +0.2 V extrema. The DC forming voltages were determined by applying triangular voltage sweeps at a rate of 2.63 V s^{-1} with a Keithley 6430.

C. Full factorial analysis: Measurement procedure

Traditional electrical analysis of the variability-prone resistive switching devices often lacks statistical meaningfulness. Cycle-to-cycle and device-to-device variability, history-dependence across thousands of cycles, and interdependent influence of external control parameters on switching properties make sophisticated methodology a requirement for conclusive statements on device behavior.

In this study, we improved upon conventional electrical characterization by programming customized waveform trains for a rapid current-limiting setup, initially introduced by Hennen *et al.*[34] This setup is capable of continuously capturing complete current–voltage (I–V) sweeps at high speeds. It is equipped with dual input voltage channels for managing the control waveforms: $V_a(t)$ determines the voltage applied to the device, while a control voltage $V_c(t)$ sets the current limit I_{limit} for the negative (SET) polarity. $V_a(t)$ is composed of concatenated bipolar triangular sweeps. Each sweep has a period of 1 ms and ramps between a constant maximum applied voltage in SET polarity ($V_{set,stop} = -1.8$ V) and a variable maximum RESET sweep voltage ($V_{reset,stop}$).

Figure 1 shows the modulation of the two independent control variables in our full factorial analysis. Panel (a) displays the extracted $V_{reset,stop}$ values for the initial 320 I–V sweeps within the $V_a(t)$ waveform. $V_{reset,stop}$ is swept back and forth through 50 linearly spaced values from 1.4 to 1.89 V, with a step size of 0.01 V between consecutive I–V sweeps. Figure 1(b) depicts the variable current limit values set by the $V_c(t)$ for the same set of I–V sweeps. The $V_c(t)$ control waveform is a piecewise constant signal with step transitions at selected zero voltage crossings between sweeps of the $V_a(t)$ voltage waveform. On a larger scale, the I_{limit} values are swept back and forth through 50 linearly spaced values between 150 and 650 μA, with an incremental step of 10 μA, as depicted in Fig. 1(c).

Figure 1(d) illustrates how we combined the waveforms $V_a(t)$ and $V_c(t)$ to sequentially navigate through the Cartesian product of the control parameter ranges. We initiate the waveforms with a low $V_{reset,stop}$ and low I_{limit} value, sweeping through the $V_{reset,stop}$ range in first instance, before sweeping through the I_{limit} range in second instance. We use a Rigol DG5102 arbitrary waveform generator to output the programmed waveforms in a synchronous manner. This setup allowed for a comprehensive single ten-second measurement shot, stressing the device-under-test (DUT) with 2500 unique

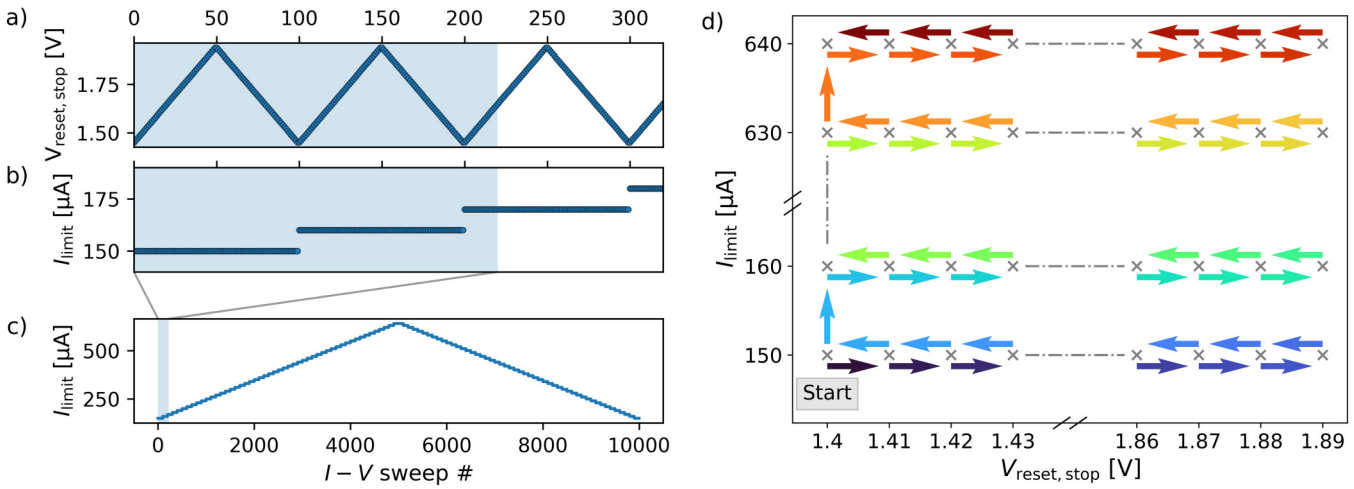

FIG. 1. The figure illustrates the measurement procedure of the full factorial analysis. Synchronized dual input of the programmed control waveforms into our current-limiting amplifier allow the rapid modulation of $V_{reset,stop}$ and I_{limit} for each bipolar I–V sweep. Panels (a) and (b) display the programmed $V_{reset,stop}$ and I_{limit} values for the first 320 I–V sweeps. $V_{reset,stop}$ is modulated back and forth within 100 I–V sweeps, maintaining a constant I_{limit}. The I_{limit} is modulated back and forth within 10 000 I–V sweeps (c), corresponding to a single 10 s measurement shot. The systematic progression through the Cartesian product of the control parameter ranges is shown in (d), starting with low $V_{reset,stop}$ and low I_{limit}, with increments of ± 0.01 V and 10 μA, respectively. Once the end point is reached, the reverse path is taken to revert back to the starting parameters to complete one measurement shot.

control parameter combinations, revisiting each condition four times per shot. This measurement shot is repeated 11 times for each DUT, resulting in a total of 110 000 I–V sweeps. The first waveform shot of 10 000 I–V sweeps serves as pre-conditioning and is excluded from further analysis.

In summary, we analyze 10 DUT per oxidation condition, which amounts to 1 000 000 I–V sweeps across 50×50 control parameters with 400 I–V sweeps each.

III. RESULTS AND DISCUSSION

A. Bottom-up growth of the switching oxide and electrical thin film analysis

Before analyzing the effects of thermal oxidation parameters on memristive device behavior, we want to define reasonable ranges for oxidation temperature and duration. The study puts a focus on back end of line (BEOL) compatible temperatures. As advanced nano-scaling approaches involving chemical–mechanical polishing (CMP) inevitably result in native oxidation of exposed ohmic electrodes,[23] we analyze the effect of a preceding native oxide on the thermal oxidation.

We compare XRR measurements in Fig. 2 from oxide growth on tantalum (Ta) thin films with and without preexisting native oxide. In Fig. 2, we depict the evolution of oxide and metal thickness over time, starting with 40 nm of sputtered tantalum before oxidation (horizontal dashed line). In the case of 300 °C (bottom row) without native oxide (left column), we observe a consumption of the metal layer (gray) with a progressively thicker oxide layer for longer oxidation durations. The ratio of oxide thickness grown to metal thickness consumed, which we term as "geometric stoichiometry," is depicted as shade of blue. Abundant oxide growth with little consumption of metallic tantalum indicates a higher oxygen content. Notably, the geometric stoichiometry is influenced by changes in film density (porosity) and cannot be interpreted as a purely chemical stoichiometry.

The oxidation of a Ta thin film with no preceding native oxide shows continuous consumption of metallic Ta and a continuously growing oxide thickness. Oxidation at 350 °C (top left) yields faster oxide growth with higher geometric stoichiometry than at 300 °C. The total film thickness increases from the initial 40 nm of deposited Ta, depicted by the total layer thickness change reaching above the horizontal dashed line for longer oxidation durations.

Similarly, for oxidation of a Ta thin film with a preceding native oxide (right column), we observe a slower growth behavior for lower oxidation temperatures. The bilayer thickness at 0 min starts above the reference thickness (dashed line) due to native oxide growth. At the beginning of thermal oxidation, the XRR measurements show a decrease from the initial native oxide thickness, correlating with a decrease in geometric stoichiometry and total bilayer thickness. In accordance with previous studies, we presume that in the initial stages of oxidation, oxygen from the native oxide dissolves faster into the metallic tantalum than is being supplied through the air–oxide interface.[35] This causes gradual stoichiometry changes from the native oxide that cannot be accurately depicted by a simple bilayer model in our XRR measurements. Subsequently, the regions depicting a thinning of native oxide likely correspond with oxygen-enriched tantalum at the oxide–metal interface and a complex (sub-)stoichiometry profile of oxide. Previous studies have discussed this dissolution of oxygen in tantalum, but the effects on resistive switching characteristics remained uninvestigated.[30,33,35] Furthermore, it is evident from Fig. 2 that the presence or absence of a preceding native oxide is

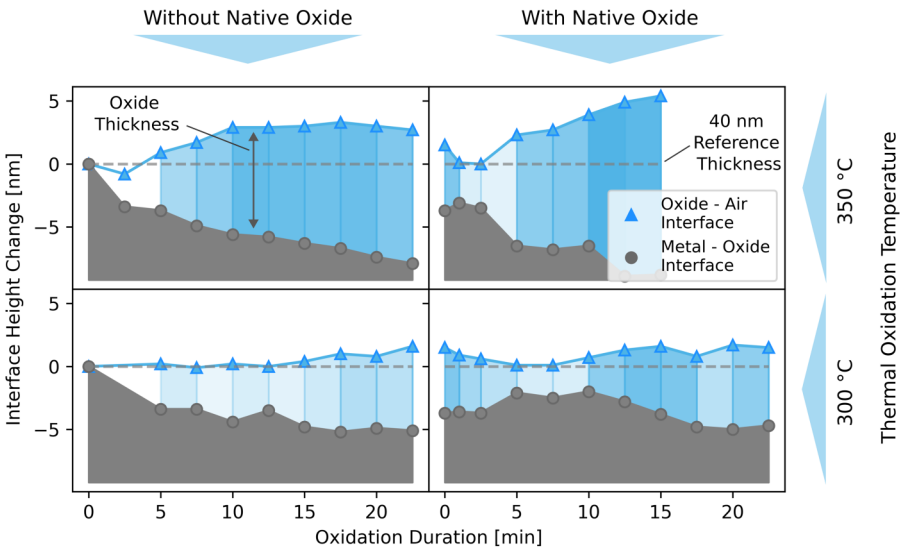

FIG. 2. XRR layer thickness evolution of a tantalum metal and oxide thin film stack during thermal oxidation at 300 °C (bottom row) and 350 °C (top row). The results show a difference in oxide growth without (left column) and with (right column) preceding native oxide. An oxidation duration of 0 min without native oxide corresponds to a reference layer thickness of 40 nm sputtered Ta (horizontal dashed line). During thermal oxidation, metallic Ta is consumed and thicker oxide layers are formed. The color gradient indicates the geometric stoichiometry (thickness of oxide grown vs metal consumed), which is further discussed in the main text, and has values ranging between 0.88 (white) and 1.61 (dark blue). The lower geometric stoichiometries in the right column may correspond to oxygen diffusion from the native oxide into the metal during the early stages of thermal oxidation.

relevant for bottom-up growth of resistive switching oxides, especially for ultra-thin ReRAM-specific oxide thicknesses. Consideration of this aspect is essential when using bottom-up oxide growth for advanced fabrication methods of ReRAM cells.

We complement the oxide growth study on native oxide with electrical capacitance measurements to get further insight into potential stoichiometry changes, as dissolution of oxygen from oxide into tantalum may affect relative permittivity of oxide. Figure 3(a) depicts the relative permittivity of oxide for various oxidation temperatures and durations, each starting with a native oxide at 0 min. The relative permittivity reaches values of around 25 for higher temperatures or longer oxidation durations, which is in line with previously reported values.[36–40] The thermal oxides from 250 °C start with a comparably low permittivity of 10–15, which consistently increases to a value of 22 for 17.5 min of oxidation. Here, an increasing relative permittivity indicates changes in stoichiometry. For 300 °C, we observe a decrease in relative permittivity for initial oxidation until 7.5 min, possibly caused by oxygen dissolution from oxide into Ta in the initial stages of oxidation. The relative permittivity rises to values of ∼ 25 for longer oxidation durations. While the relative permittivity is calculated with our measured oxide thickness, the pure electrical capacitance measurement (see supplementary Fig. S1) presents the same trend, while being independent of the XRR thickness measurements. Only 250 and 300 °C show an upwards trend of electrical capacitance during oxide growth, indicating increases in relative permittivity. The 250 °C data set has more pronounced error bars, because the HP4284A LCRMeter is sensitive to the higher leakage current for these thermal oxides.

Figure 3(b) depicts the pristine resistance of the thermal oxides determined by current leakage measurements through a $50 \times 50\,\mu m^2$ large contact area. Thicker thermal oxides from 400 °C (red) quickly reach resistances at the resolution limit (gray shading) of the source measure unit. On the lower end of the temperature range, the 250 °C thermal oxides have a high leakage current. This can interfere with using the thermal oxides for resistive switching when the leakage current reaches the current limit before forming the device. As the leakage current scales with the active device area, smaller devices are unaffected by this problem, enabling the use of lower oxidation temperatures for scaled resistive switching devices. We observe only small differences in pristine resistance between 300 and 350 °C thermal oxides.

While leakage may set a lower limit of usable oxidation parameters, the forming voltage of a device sets an upper limit. Constraints in maximum voltage of on-chip peripheral circuitry and parasitic capacitances causing a current overshoot[41–44] motivate reducing the forming voltage as much as possible. Figure 3(c) depicts the forming voltage of the same devices used for the previous capacitance and leakage measurements. Rapid oxide growth at 400 °C causes undesirable high forming voltage even at short oxidation durations. While oxidation at 350 °C results in forming voltages below 5 V, an increase in forming voltage is to be expected when nano-scaling the device area or using fast pulses. This effectively limits reasonable oxidation temperatures to 300 °C and below for using bottom-up oxide growth in industrially oriented on-chip resistive switching devices.

B. Full factorial analysis of memristive device properties

We use a factorial measurement protocol on our customized measurement setup (see Sec. II) to study the effects of selected thermal oxidation parameters on resistive switching behavior of memristive devices. Here, we compare the switching oxides grown by bottom-up electrode oxidation at 300 °C for 10 min (device A) and 250 °C for 10 min (device B) with a preceding native oxide. We focus on devices with a preceding native oxide, as advanced nano-scaling processes involving CMP in ambient atmosphere will

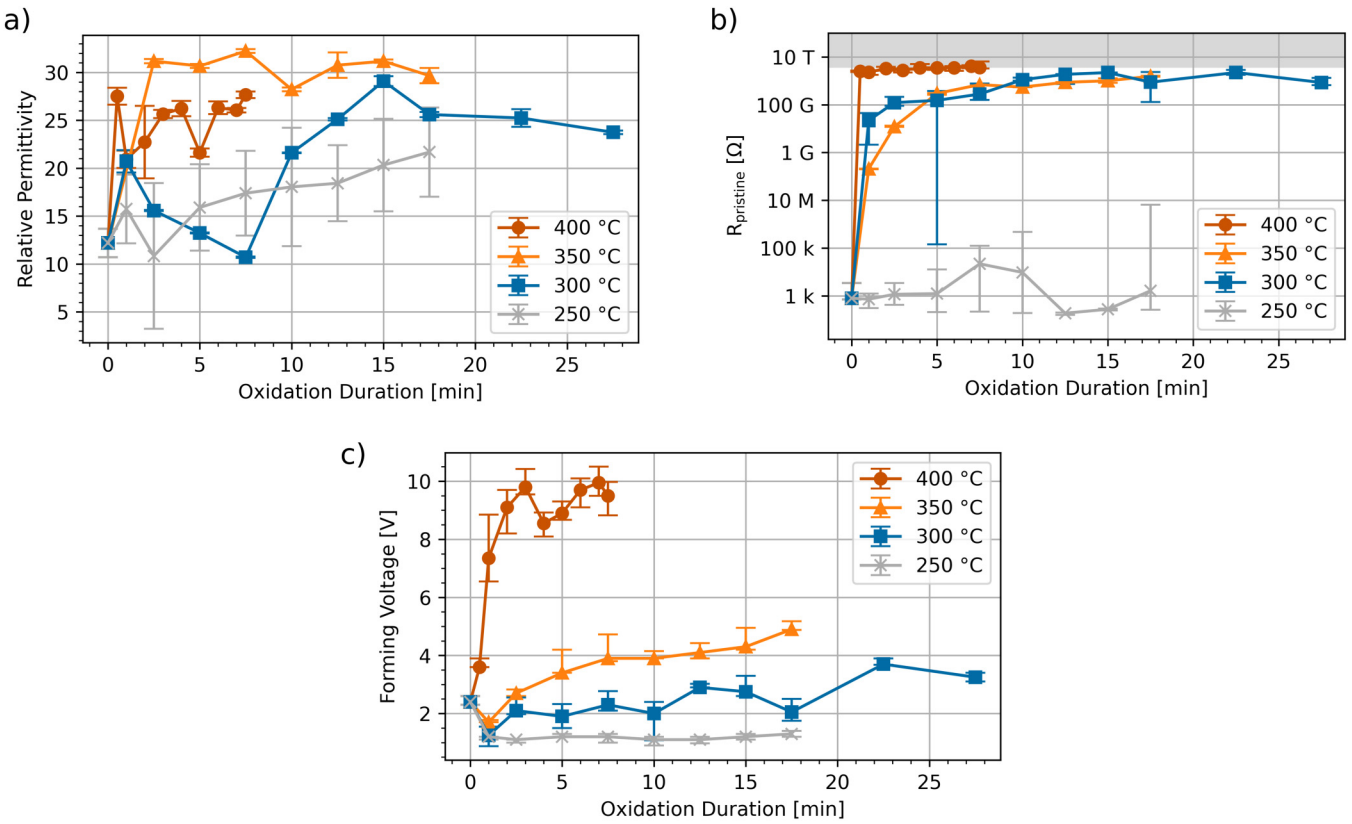

FIG. 3. Electrical measurements of thermally oxidized tantalum (with preceding native oxide at 0 min) for various oxidation durations and temperatures. (a) Relative permittivity of the TiN/Ta/TaO_x/Pt thin film stack. (b) Resistance of the $50 \times 50\,\mu m^2$ oxide area extracted from leakage measurements. The gray box indicates the resolution limit of the setup. (c) Forming voltages of the $50 \times 50\,\mu m^2$ devices at a sweep rate of $2.63\,V\,s^{-1}$. The error bars indicate first and third quartiles.

also inherently lead to native oxide formation. The active device area is $2 \times 6\,\mu m^2$ and both devices are, besides the oxide growth conditions, fabricated identically. We stress both devices with the same electrical waveforms to allow for optimal comparison.

Figure 4 depicts the I–V sweeps of both devices for various control parameter combinations of I_{limit} and $V_{reset,stop}$. Device A has a larger R_{off}/R_{on} window for a given electrical control parameter set. This originates from different SET and RESET transitions when comparing the thermal oxides. The RESET behavior of device A at positive voltages shows two distinct current peaks, which are followed by an abrupt RESET transition into a high HRS. Similarly, we also observe a typical abrupt SET transition into low LRS, especially for high $V_{reset,stop}$ values (rightmost column).

In contrast, device B shows a less binary RESET transition than device A. This allows for access to intermediate resistance states from the RESET side for lower $V_{reset,stop}$ amplitude (leftmost column). Due to interaction of device behavior with peripheral circuitry, reports of memristive devices typically show a gradual RESET transition, contrasted by an abrupt SET transition.[45] However, our device B also has the desired gradual transition during SET (negative voltage polarity). A comparison of the SET transitions for both devices on a current–time plot emphasizes the gradual SET for device B (see supplementary Fig. S2). In Fig. 5, we take a closer look at the SET transition by extracting the SET abruptness value (SA), which we define as

$$\mathrm{SA} = \max\left|\frac{dI}{dt}\right|, \tag{1}$$

for $V \in [0, V_{set,stop}]$ and $\frac{dV}{dt} < 0$. Here, I is the electrical current, t is the time, and $V_{set,stop}$ is the maximum applied voltage in SET polarity. We extract the SET abruptness value for each individual I–V sweep in our factorial analysis data set, consisting of 1×10^6 sweeps across ten devices for each thermal oxide. Figure 5(a) depicts the median SET abruptness for all 50×50 control parameter combinations. Device A (left) reaches a maximum SA of around $100\,A\,s^{-1}$ for high $V_{reset,stop}$ and high I_{limit}. The maximum SA is partially limited by the I_{limit}, resulting in a linear correlation between SA and I_{limit} for high $V_{reset,stop}$. However, even for high I_{limit} values, the SET abruptness can be mitigated through the reduction of $V_{reset,stop}$. This observation indicates that the HRS

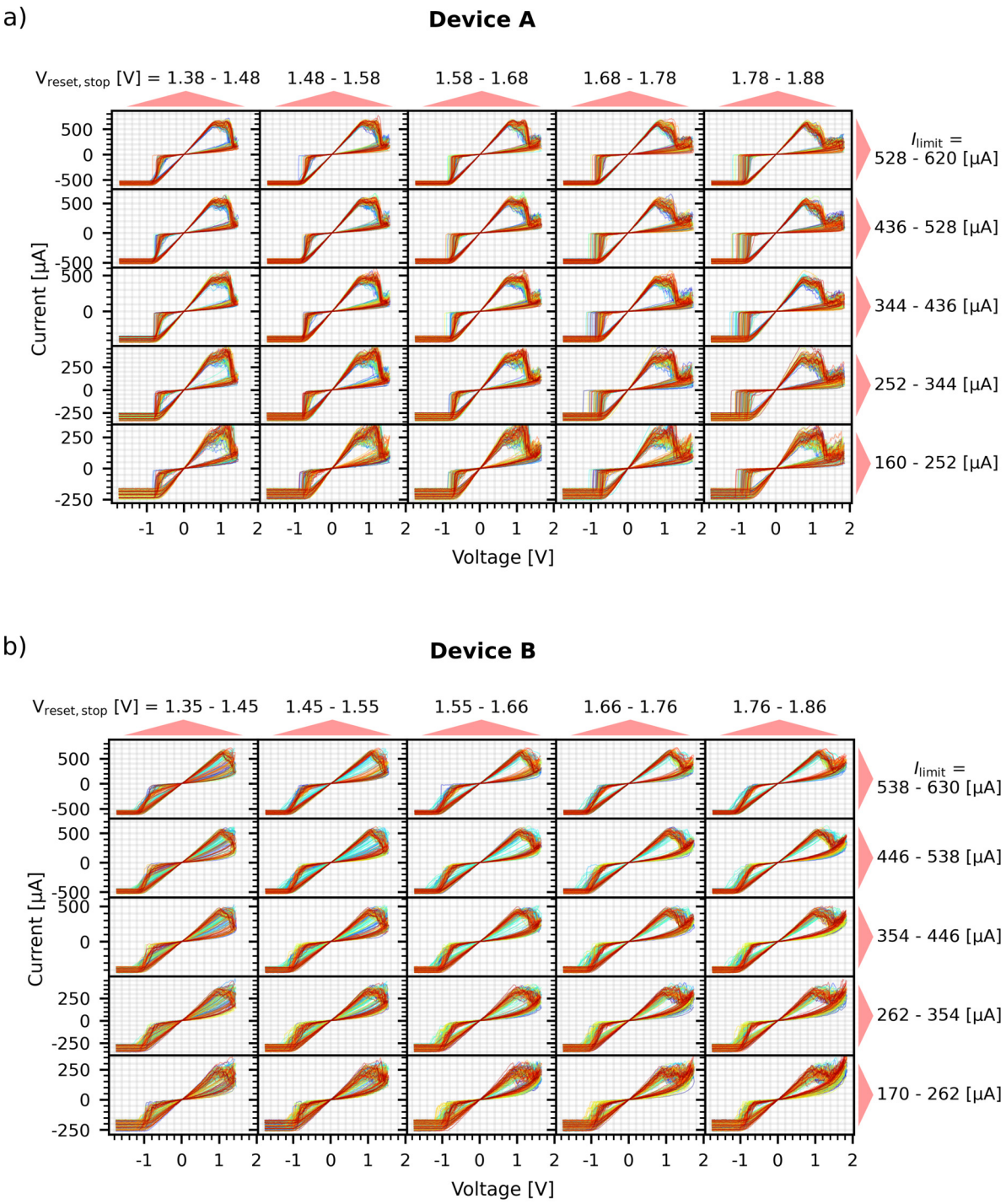

FIG. 4. *I–V* sweep comparison between device A and device B. The 2 × 6 μm^2 devices are fabricated identically, apart from the thermal oxidation of the Ta electrode surface (device A: 300 °C, 10 min; device B: 250 °C, 10 min). For better visibility, the parameterized 50 × 50 (I_{limit}, $V_{reset,stop}$) control parameter conditions from our measurements are grouped into a coarser 5 × 5 grid. In a given row, the values of $V_{reset,stop}$ increase from left to right. Within a given column, the current limit values increase from bottom to top. The current axis range of each row is adjusted according to their I_{limit}. Device B consistently shows gradual SET transitions and a different RESET characteristic.

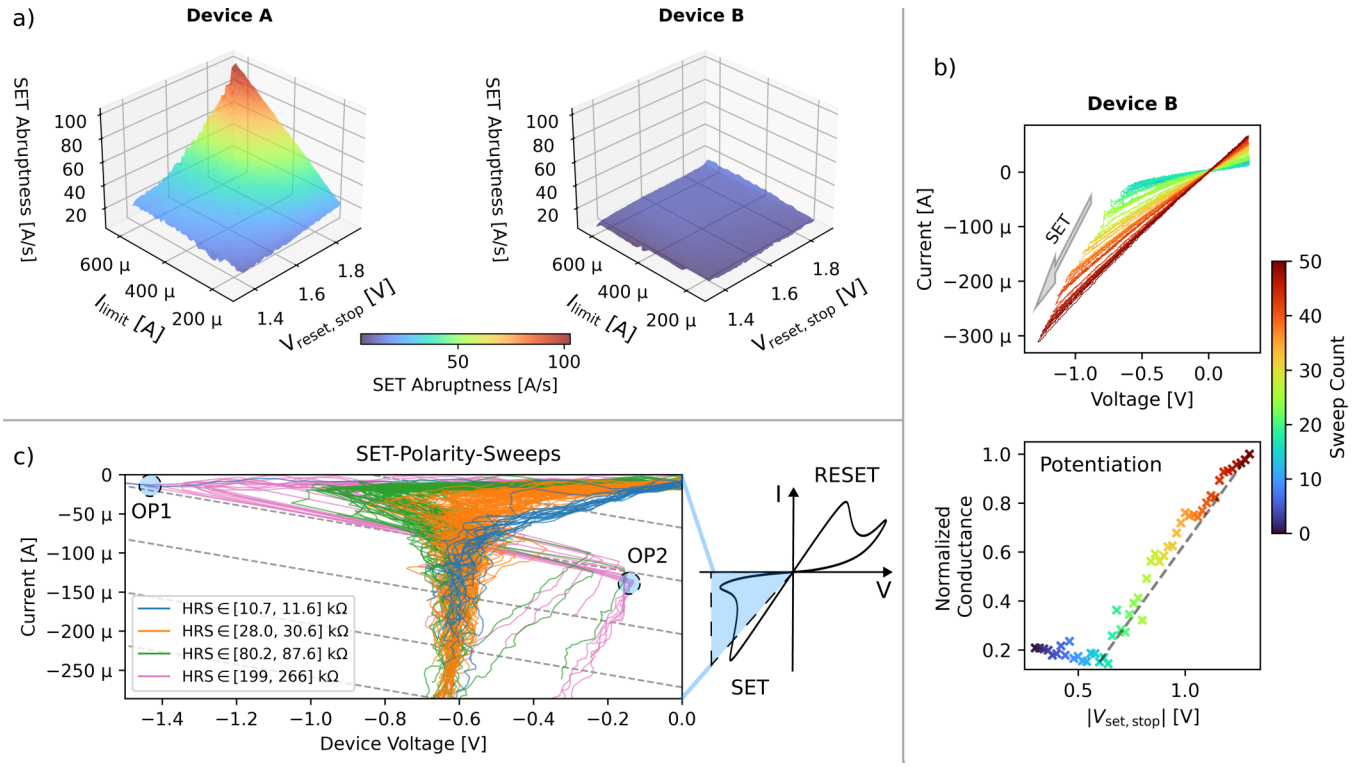

FIG. 5. (a) The SET abruptness in device A strongly correlates with I_{limit} and $V_{reset,stop}$. Device B shows stabilized gradual SET transitions across all control parameter combinations. (b) The gradual SET characteristic in device B can be exploited to access intermediate resistance states by voltage sweeping to different $V_{set,stop}$ amplitudes. Depicted are 50 individual *I*–*V* sweeps with incrementally increasing $V_{set,stop}$ at the SET polarity. Potentiation is demonstrated by gradually increasing the conductance for $|V_{set,stop}|$ larger than 0.6 V. The dashed line is a reference for linearity. (c) SET polarity sweeps with a 12 kΩ external series resistance reveal S-type NDR-characteristics that are more pronounced for higher HRS (purple). This causes abrupt and poorly controlled switching along the load line (dashed) between two operating points (OP1, OP2). Milder NDR-characteristics at lower HRS (blue) stabilize gradual SET transitions.

plays a crucial role in controlling the characteristics of the SET transition. Furthermore, it has previously been shown that abrupt SET transitions in memristive devices arise from an interaction of the load line slope from a given series resistance with the *I*–*V*-characteristic.[45] In this regard, we find that despite identical electrode dimensions, the thermal oxidation parameters of device B yield an approximately 250 Ω higher internal series resistance than in device A (see supplementary Fig. S3). Based on our discussion from the preceding native oxide growth study, we believe that oxygen-enriched Ta or sub-stoichiometric TaO_x at the oxide–metal interface from thermal oxidation is the cause of this increased internal series resistance.

Figure 5(a) shows that the device B, with a higher internal series resistance at the switching oxide interface, consistently exhibits a gradual SET transition with a low SA value of 10 A s^{-1}. This is in agreement with previous studies, where combining the switching oxide with various depth profiles of sub-stoichiometric TaO_x induced a more gradual SET characteristic.[46–51] We choose the thermal oxidation parameters for device B to stabilize low SA values for all electrical control parameters and mitigate the SET abruptness, a measure for the extent of circuit instability during the SET transition.

We exploit the absence of circuit instabilities during SET transition in device B to access intermediate resistance states for potential analog computing applications. Figure 5(b) depicts 50 bipolar *I*–*V* sweeps on device B with a fixed $V_{reset,stop}$ of 0.3 V and a maximum SET sweep voltage $|V_{set,stop}|$ increasing incrementally by 0.02 V from 0.3 to 1.3 V. Starting in the HRS, the normalized conductance of the memristive device increases after a minimal required set voltage V_{set} of around 0.6 V is surpassed. A slow sweep duration of 1 ms emphasizes that the observed analog behavior does not necessitate fast pulses. The device has a desirable nearly-linear analog weight adjustment during potentiation.

The increased internal series resistance originating from the thermal treatment in device B is one factor promoting this analog behavior during the SET sweep. However, avoiding abrupt switching from circuit instabilities further relies on optimal interaction of the load line with the *I*–*V*-characteristic during voltage sweeping. We demonstrate this concept in Fig. 5(c) on a sputtered TaO_x device, where we measure SET polarity sweeps for different HRS with a 12 kΩ external series resistance (indicated by the dashed load lines). The current as a function of device voltage, rather than applied voltage, exhibits an S-type negative differential resistance

(NDR). Our measurement reveals that the HRS is a main contributor to the shape of the NDR-characteristic. Higher HRS (purple, green) with increased V_{set} show a pronounced NDR-characteristic, while lower HRS (blue, orange) have a milder NDR-characteristic. The former filament state is prone to cause abrupt transition between two distinct operating points (exemplarily labeled with OP1 and OP2) along the load line for voltage-controlled sweeps. On the other hand, milder NDR-characteristics (blue) enable continuous sweeping of the operating point along the I–V-characteristic for analog weight adjustment. In this measurement, a sputtered TaO_x device is used to highlight the NDR-characteristic as a function of filament state, as this specific device has HRS values that are adjustable across a large range. We refer to the supplementary for a more detailed discussion of the measurement result and device fabrication (see supplementary Fig. S4).

As the NDR-characteristic strongly depends on the HRS, we extract the HRS values of 1×10^6 I–V sweeps for thermally oxidized devices A and B across all 2500 control parameters of our full factorial analysis [see Fig. 6(a)]. Despite using the same electrical waveforms for stress testing both devices, we observe different HRS values and trends for a given control parameter combination. HRS values of device A show a strong dependency on $V_{reset,stop}$ and a slight dependency on I_{limit}. Here, higher $V_{reset,stop}$ and lower I_{limit} correlate with a higher HRS. A minimum $V_{reset,stop}$ of 1.4 V is sufficient to RESET device A. In contrast, device B requires at least a $V_{reset,stop}$ of 1.5 V to successfully RESET at high I_{limit}. The voltage drop over the additional internal series resistance at the metal–oxide interface from the thermal oxidation shifts the minimum required $V_{reset,stop}$ to higher values. Notably, further increases in $V_{reset,stop}$ do not yield higher HRS in device B, constraining the

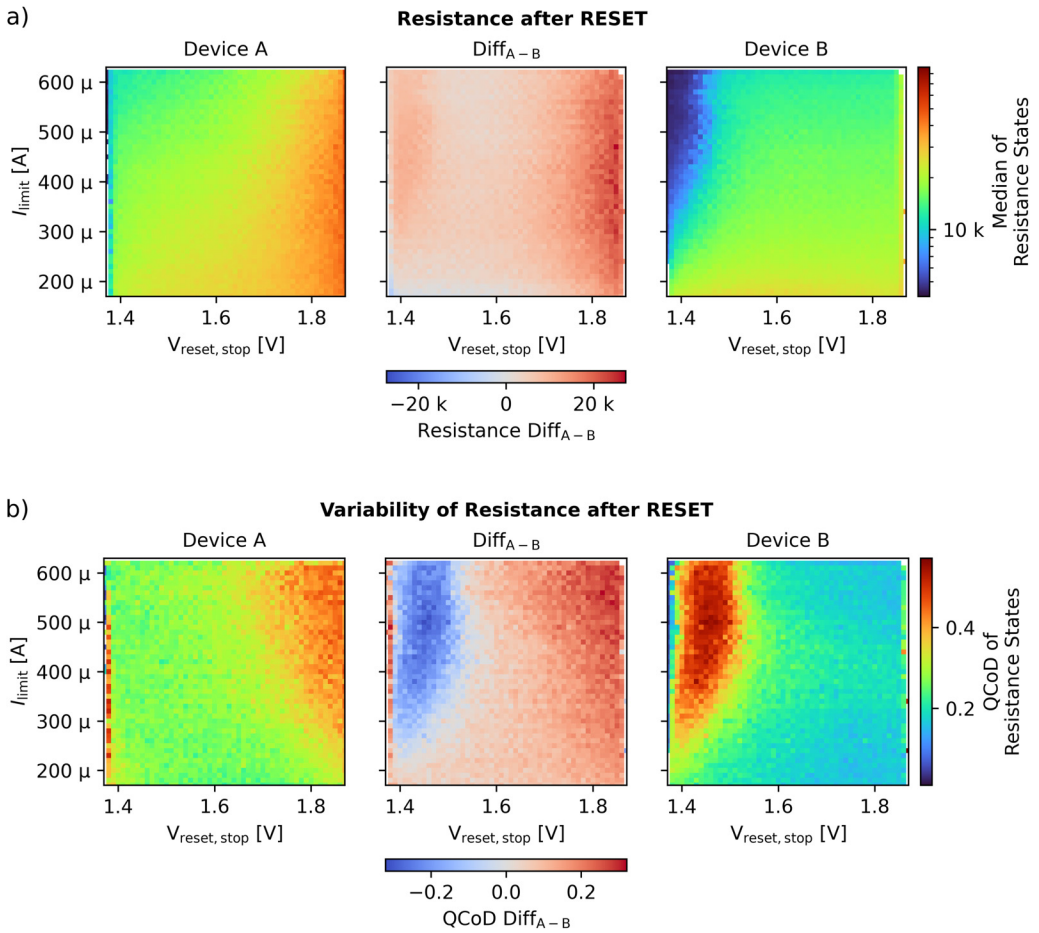

FIG. 6. (a) Comparison of devices A and B regarding their resistance states after RESET sweep, evaluated across a grid of 50 × 50 control parameters. Each data point on this grid represents the median resistance from 400 I–V sweeps across 10 DUT. The center panel depicts the difference in resistance states between the devices for identical control parameter combinations. (b) Comparison of the write-variability of resistance states after the RESET sweep. Higher values of quartile coefficient of dispersion (QCoD) indicate a higher variability. The resistance decrease and variability increase at 1.45 V in device B are caused by application of insufficient RESET voltage, originating from a voltage drop across the larger internal series resistance.

resistance state to a constant level. The differential plot of Fig. 6(a) shows that the HRS level of device B tends to be lower than device A for the same electrical control parameters. Therefore, the HRS is fixed to lower values, corresponding with mild NDR-characteristics. These properties of device B stabilize a gradual SET transition, allowing for reproducible analog switching capability across a large range of control parameters.

Insufficient reproducibility of resistance states for identical measurement parameters remains a significant challenge for filamentary oxide-based memristive devices. While improved variability of the more conductive LRS can be achieved by inserting an external series resistance to improve control during the SET event,[52] the need for lower variability of the more resistive HRS is much more critical, especially in multi-level switching applications. For this reason, we analyze the HRS variability and its origins from the RESET transition characteristics in our thermal oxide devices. Figure 6(b) depicts the quartile coefficient of dispersion QCoD $= \frac{Q_3-Q_1}{Q_3+Q_1}$ as a measure of normalized variability, where Q_1 and Q_3 are the first and third quartiles of resistance states after the RESET sweep. Device B shows a drastic increase in write-variability for low $V_{reset,stop}$, as the applied RESET voltage is close to the intrinsic V_{reset} transition, which causes a large dispersion of resistance states from partially failed RESETs. However, for sufficiently high $V_{reset,stop}$, the normalized variability of resistance states amounts to comparably low QCoD-values of around 0.2, remaining largely independent of control parameters. In contrast, device A shows larger variability in HRS for all successful RESETs [see differential plot of Fig. 6(b)]. Device A reaches a maximum QCoD-value of around 0.5, which is twice as high as observed in device B for successful RESETs. Figure 6(b) (left) reveals an increased variability of resistance states in device A for high $V_{reset,stop}$ and high I_{limit}. The influence of high $V_{reset,stop}$ on increasing variability can be explained by causing a higher HRS with lower oxygen vacancy concentrations in the conducting filament. The redistribution of oxygen vacancies in regions with low local concentrations corresponds to a higher relative impact on resistance change, resulting in a higher QCoD value. However, while low I_{limit} values correlate with higher HRS [see device A in Fig. 6(a)], the opposite is true for the variability, where high I_{limit} values correlate with increases in QCoD [see device A in Fig. 6(b)]. This indicates that the HRS is not the only contributor to resistance variability in memristive devices.

Figure 7(a) depicts the resistance variability as a function of the resistance value. Here, we depict the QCoD of HRS against the median HRS, where each marker of the plot corresponds to 400 I–V sweeps from each of the 2500 control parameters. Device A (circle markers) spans a wider range of resistance states than device B (triangular markers, bottom left cluster). The observed trend to higher variability for higher resistance states, depicted by the diagonal dashed lines, is in agreement with previous studies.[53–56] In addition to these previous findings, we observe a significant influence of the RESET abruptness (RA) on the resistance state variability, where RA is defined analogous to SA in Eq. (1). The diagonal lines indicate the trend in device A for two exemplary RESET abruptness values of around 20 and 35 A s^{-1}. A lower RESET abruptness causes a shift of the diagonal trend to higher resistances, resulting in lower variability for a given resistance state. For a resistance of 30 kΩ, a reduction of the RA from 35 to 20 A s^{-1} yields a decrease in variability by 35% from a QCoD value of 0.42 down to a value of 0.28. Device B with its gradual RESET transitions (dark blue) has the lowest HRS variability due to its lowest RA-values. However, extrapolating the RA-trend of 20 A s^{-1} from device A to lower resistances, we observe an unfavorable shift in device B, where even lower RA-values (10 A s^{-1}) are required to reach the same HRS write-variability. Therefore, device B has a worse HRS-variability for a given parameter set of resistance and RA. This is a consequence of higher LRS variability of the gradual SET transitions in device B (see supplementary Fig. S5). The increased LRS variability is transferred to the HRS variability through dispersed RESET-transition points.

Figure 7(b) shows the resistance variability as a function of RESET abruptness and reinforces the observation that the characteristic of the RESET transition has an effect on the variability of subsequent HRS states. Dashed lines representing 15 and 25 kΩ visualize the trend to higher QCoD values for higher RA. Notably, for a fixed RESET abruptness of 25 A s^{-1}, we also observe an increase in HRS

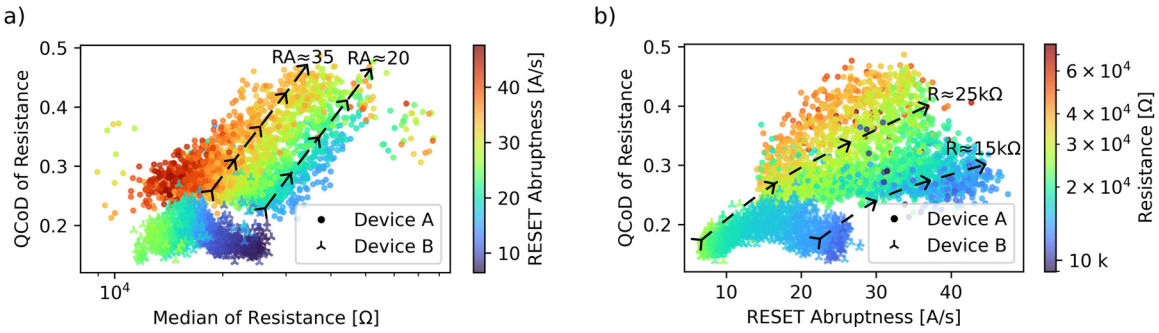

FIG. 7. (a) Resistance write-variability as a function of the resistance state. Each data point corresponds to one unique set of control parameters. The trend to higher variability for higher resistance states is shifted for different RESET abruptness values (RA, dashed lines). Shifting the trend to higher resistances for lower RA indicates device performance improvement. (b) Resistance write-variability as a function of the RESET abruptness. For a given resistance state (dashed lines), higher RA results in higher variability. Failed RESETs in device B from insufficient $V_{reset,stop} < 1.6$ V are filtered out due to artificial inflation of variability.

variability for higher resistance states. In combination with Fig. 7(a), this indicates that both the resistance state and the RESET abruptness individually contribute to increased variability.

The underlying physical mechanism of RESET abruptness increasing the HRS variability could originate from different kinetics of filament switching. A gradual RESET transition inherently links the total RESET duration to the voltage sweep rate, where long *I*–*V* sweep durations lead to slower RESET transitions. On the contrary, the abrupt RESET transitions arising from circuit instabilities occur within a shorter timeframe and cannot be slowed down by increasing the *I*–*V* sweep duration. Therefore, we suggest changes in filament morphology from the temporal difference in RESET kinetics. Here, slow and gradual RESET transitions may cause a more uniform (re-)distribution of oxygen vacancies in the filament, enabling more reproducible resistance states after RESET.

IV. CONCLUSION

In this study, we establish optimal parameter ranges of bottom-up thermal oxide growth on tantalum electrode surfaces for memristive device fabrication. Oxidation temperatures of 350 °C and above are unsuitable for the desired low forming voltages in industrially oriented devices. However, the presence of a preceding native oxide is particularly impactful for thinner oxides at lower oxidation temperatures. Distinct permittivity changes in these samples indicate a complex evolution of oxide (sub-)stoichiometry from thermal oxidation.

We develop a comprehensive measurement procedure for full factorial analysis to compare the switching characteristics of two devices, which are identical in all aspects except for their thermal oxidation parameters. Device fabrication at the lower oxidation temperature results in consistent gradual SET transitions that allow for access to intermediate resistance states. This device also shows consistently lower HRS across a large range of external control parameter combinations. In addition, the thermal oxidation conditions of this device cause a notable increase in the internal series resistance at the metal–oxide interface.

We conclude that avoiding abrupt circuit instabilities during SET transitions in our devices relies on the optimal interaction of two key features: the HRS-dependent NDR-characteristic of the memristive device and the load line alteration by the internal series resistance. Optimizing thermal oxidation parameters can stabilize this device behavior, facilitating gradual SET transitions even with slow *I*–*V* sweeps and enabling the implementation of filamentary switching for analog computing approaches.

HRS write-variability remains a significant challenge for analog devices. Beyond the resistance state itself, we introduce the RESET abruptness value as a further contributor to HRS variability. Our factorial analysis demonstrates that slow and gradual RESET transitions are associated with a decreased HRS variability, presumably from a more uniform filament morphology. Therefore, it is essential to fine-tune bottom-up oxide growth conditions to the desired memristive device behavior.

SUPPLEMENTARY MATERIAL

The referenced supplementary Figs. S1–S5 are available in the electronic supplementary material.

ACKNOWLEDGMENTS

This work was in part funded by the German Research Foundation (DFG) under Grant No. SFB 917, in part by the Federal Ministry of Education and Research (BMBF, Germany) in the Projects NEUROTEC 2 (Project Nos. 16ME0398K and 16ME0399) and NeuroSys (Nos. 03ZU1106AA and 03ZU1106BA), and is based on the Jülich Aachen Research Alliance (JARA-FIT). We want to thank Petra Grewe and Erdoglija Daliborka for fruitful discussions and support.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

P. Stasner: Conceptualization (lead); Investigation (lead); Methodology (equal); Visualization (lead); Writing – original draft (lead). **T. Hennen:** Conceptualization (supporting); Methodology (equal); Writing – original draft (supporting). **E. Gorbunova:** Investigation (supporting). **A. Garcia Munoz:** Investigation (supporting). **R. Waser:** Supervision (supporting). **D. J. Wouters:** Supervision (lead); Validation (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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