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ABSTRACT

Polycrystalline germanium (Ge) thin films have reemerged as promising materials for next-generation electronic and optoelectronic devices because of their superior electrical and optical properties. However, challenges such as high defect densities, small grain sizes, and unstable n-type conduction have limited their practical application. In this paper, we review the progress in the solid-phase crystallization of Ge thin films on insulating substrates. We first discuss conventional processes with excessive nucleation that lead to poor crystallinity and electrical properties. We then introduce advanced solid-phase crystallization strategies, highlighting the critical role of controlling the amorphous deposition temperature to control atomic density, increase grain size, and reduce acceptor defects. Additionally, the incorporation of tin (Sn) has been shown to passivate grain boundaries, while the modulation of film thickness and the introduction of interfacial layers have demonstrated the ability to mitigate carrier scattering at the substrate interface. This review also addresses impurity doping techniques for precise Fermi level control, strain engineering effects on grain boundary barrier energies, and metal-induced lateral crystallization for grain alignment. These innovations have culminated in achieving record-high carrier mobilities of 690 $cm^2\ V^{-1}\ s^{-1}$ for p-type and 450 $cm^2\ V^{-1}\ s^{-1}$ for n-type films, approaching single-crystal performance. The insights provided herein will pave the way for the development of high-performance Ge-based thin-film transistors and flexible electronic devices via low-temperature processing.

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I. INTRODUCTION

Germanium (Ge), one of the earliest discovered semiconductors, was replaced by silicon (Si) in the mainstream electronics industry.[1,2] However, its superior electrical and optical properties have brought Ge back to the spotlight as a promising material for next-generation electronics, including transistors,[3–6] solar cells,[7–9] photonic devices,[10–12] and thermoelectric generators.[13–15] Notably, multi-junction solar cells used in space applications are a prime example of Ge's industrial success. However, the high cost of single-crystal Ge substrates limits their

widespread adoption. Similarly, although Ge-based metal–oxide–semiconductor field-effect transistors (MOSFETs) have been explored owing to their high carrier mobility, their narrow bandgap leads to significant leakage current issues. Nevertheless, Ge has great potential for thin-film applications, which is the primary focus of this review.

Thin-film Ge offers key advantages over bulk Ge, which makes it particularly attractive for electronic and optoelectronic device applications. Its high optical absorption coefficient ($\sim 10^4\,cm^{-1}$ at 0.8 eV) allows efficient light absorption even in thin layers.[1] Additionally, the narrow-bandgap-induced leakage current of Ge, a major issue in bulk MOSFETs, can be mitigated by using thinner films.[16–18] Its low crystallization temperature enables the synthesis of versatile substrates such as glass, plastic, and large-scale integrated circuits (LSIs).[19–21] Moreover, Ge possesses a relatively low Young's modulus (~100 GPa) among inorganic semiconductor materials, which makes it mechanically compatible with flexible device applications. Therefore, from both the cost and performance perspectives, the development of high-quality Ge-on-insulator structures has become a critical research goal. Early approaches to producing Ge-on-insulator structures included mechanical transfer[22,23] and oxide condensation methods,[24–26] which successfully produced high-quality Ge films but required either single-crystal substrates or high processing temperatures. Rapid melting growth techniques have also achieved single-crystal-like Ge layers on insulators;[27–30] however, their reliance on Si substrates or high temperature process has limited their application. To overcome these limitations, the direct low-temperature synthesis of Ge thin films on insulating substrates has attracted significant interest for large-area devices, such as thin-film transistors and solar cells.

Ge films directly synthesized on amorphous substrates inevitably form polycrystalline structures with various defects, particularly grain boundaries. Vapor-phase crystallization methods such as sputtering[31] and chemical-vapor deposition (CVD)[32–34] have enabled the low-temperature synthesis of polycrystalline (poly-) Ge thin films. Laser annealing[35–38] and plasma irradiation,[39] a form of liquid-phase crystallization, have yielded highly crystalline (c-) Ge with grain sizes on the order of several micrometers, albeit with surface roughness issues. However, optimizing laser power and scanning direction has enabled localized single-crystal regions to achieve high carrier mobility. Solid-phase crystallization (SPC) via furnace or lamp annealing provides smooth, uniform poly-Ge layers at relatively low temperatures,[40–43] although crystallinity remains a challenge. Metal-induced crystallization (MIC),[44–47] particularly the layer exchange phenomenon,[48–50] has provided various benefits, including lowering growth temperature; however, residual metals in Ge limit its device applications. These methods have enabled the synthesis of poly-Ge thin films and their devices on flexible substrates, including plastics.[51–55] Despite these efforts, three intrinsic issues have prevented poly-Ge thin films from reaching their full potential. First, the low nucleation energy of Ge produces small grain sizes,[19,56,57] which increases carrier scattering and recombination. Second, Ge defects frequently act as acceptors,[58–61] leading to high hole concentrations (p: 10^{17}–$10^{19}\,cm^{-3}$) even without doping. Third, the low activation rate of n-type dopants,[62–65] compounded by the effects of small grains and high p, complicates stable n-type conduction.

Recent advancements, particularly in SPC techniques, have begun to address these challenges. Our studies highlight that the control of nucleation and growth in SPC increases grain size, reduces acceptor defects, and improves the carrier mobility of poly-Ge thin films.[66] Moreover, the impurity doping of high-quality poly-Ge controls the conduction type and carrier concentration.[67] These advancements have led to record-breaking poly-Ge thin film carrier mobilities: $690\,cm^2\,V^{-1}\,s^{-1}$ for p-type[68] and $450\,cm^2\,V^{-1}\,s^{-1}$ for n-type.[69] Notably, these values are among the highest reported for low-temperature-synthesized polycrystalline semiconductor thin films. Consequently, poly-Ge thin films are now recognized as strong candidates for high-performance electronic applications. In this review, we comprehensively analyzed the recent progress in SPC-based technologies for poly-Ge thin films. By highlighting the innovations in our recent achievements, we provide a holistic view of the path toward the realization of high-performance Ge thin films on insulating substrates.

II. CONVENTIONAL SOLID-PHASE CRYSTALLIZATION

Figure 1 illustrates the three fundamental stages of SPC in polycrystalline thin-film formation.[19,70] The process begins with deposition, during which an amorphous Ge (a-Ge) layer is formed on the substrate, typically through a form of vacuum evaporation. During this stage, an amorphous layer with randomly arranged atoms is prepared for crystallization via thermal annealing. The second stage, nucleation, marks the onset of crystallization. As the amorphous film is annealed, crystalline domains begin to form at isolated points. The density and distribution of these nuclei significantly affect the final grain size. A lower nucleation rate, which is often achieved at lower annealing temperatures, allows fewer nuclei to form, promoting the formation of larger grains during the growth phase. Finally, during the growth stage, the crystalline domains expand laterally and occupy the surrounding amorphous regions. This stage is driven by the lateral growth velocity, which is strongly dependent on the annealing temperature. Controlling these three stages is a key to achieving high-quality poly-Ge thin films with excellent electrical performance.

Figure 2 shows the structural and electrical characteristics of poly-Ge thin films fabricated using conventional SPC,[40] where the a-Ge precursor thin films were deposited at around room temperature (RT). The planar transmission electron microscopy (TEM) images in Figs. 2(a) and 2(b) show the microstructures formed at the growth temperatures (T_g) of 425 and 500 °C, respectively. The TEM image at $T_g = 425$ °C reveals a larger grain size of ~200 nm compared to ~80 nm at $T_g = 500$ °C. This difference is due to the lower spontaneous nucleation rate at $T_g = 425$ °C, which allows the grains to grow larger before the formation of new nuclei. However, these grain sizes are more than one order of magnitude smaller than those of Si formed via SPC.[70,71] This behavior is attributed to the small difference between the activation energies required for nucleation and growth in

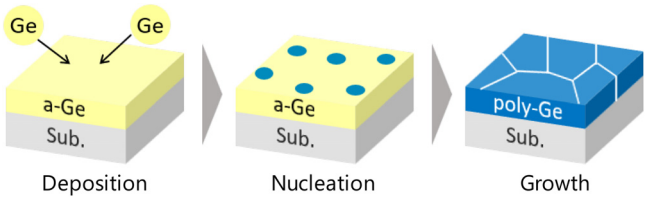

FIG. 1. Schematic of the SPC process consisting of deposition, nucleation, and growth. Typically, the annealing temperature ranges from 350 to 500 °C with durations from several minutes to tens of hours, and the substrates are amorphous insulators such as SiO_2 or plastic.

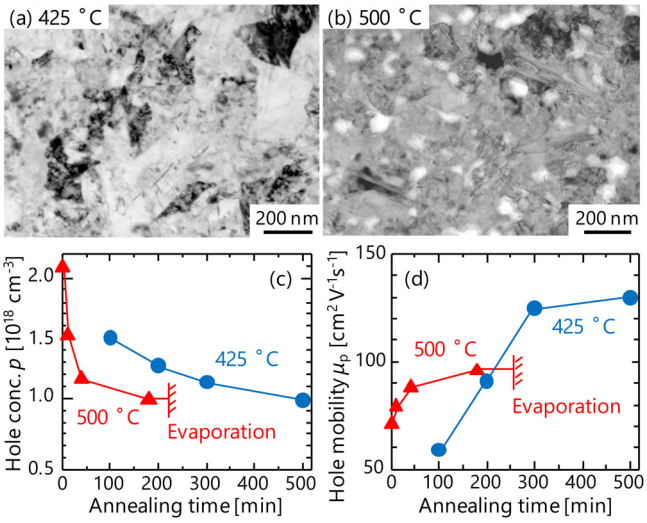

FIG. 2. Crystal and electrical properties of the poly-Ge thin films (thickness: 50 nm) formed by conventional SPC. Planar bright-field TEM images formed at (a) 425 °C for 200 min and (b) 500 °C for 180 min. (c) Hole concentration (p) and (d) hole mobility (μ_p) as a function of the annealing time.

Ge.[19,56,57] Hall effect measurements revealed that the grown films were p-type owing to hole generation from the acceptor defects.[58–61] Figures 2(c) and 2(d) present the hole concentration (p) and hole mobility (μ_p) of the Ge thin films grown at $T_g = 425$ and 500 °C, respectively. At $T_g = 500$ °C, prolonged annealing resulted in the disappearance of the Ge thin film. This phenomenon is generally observed in Ge thin films and is attributed to the reaction between the oxygen in the ambient environment and Ge, which leads to the volatilization of Ge as GeO.[18] This phenomenon can be somewhat improved by reducing the amount of oxygen present in the annealing atmosphere,[72] short-time flashlamp annealing,[73,74] or combined patterning and capping.[75,76] For both samples, p decreases while μ_p increases with annealing time. These phenomena can be understood to be the result of grain growth and acceptor defect reduction during SPC. The resulting μ_p for $T_g = 425$ °C is higher than that for $T_g = 500$ °C. This is because a lower T_g reduces grain boundary density, while the carrier mobility of poly-Ge thin films is limited by grain boundary scattering, similar to that of poly-Si thin films.[77–79] The maximum μ_p observed is 130 $cm^2\ V^{-1}\ s^{-1}$, which is significantly low considering the potential of Ge.[80,81] Additionally, p remains in the order of 10^{18} cm^{-3}, making it difficult to apply these films to semiconductor devices where precise carrier concentration control is essential. Thus, poly-Ge thin films formed via conventional SPC exhibit poor crystallinity and electrical properties.

III. ADVANCED SOLID-PHASE CRYSTALLIZATION

A. Control of amorphous deposition temperature

In 2017, we discovered that the deposition temperature (T_d) of a Ge thin film, which serves as a precursor to SPC, has a dramatic impact on the crystallinity of poly-Ge after SPC.[66] Figure 3 shows the impact of T_d on the microstructure and electrical performance of poly-Ge thin films formed by SPC. Figure 3(a) presents the scanning electron microscopy (SEM) images of the poly-Ge thin films for $T_d = 50$, 125, and 200 °C, followed by annealing at 450 °C. We note that

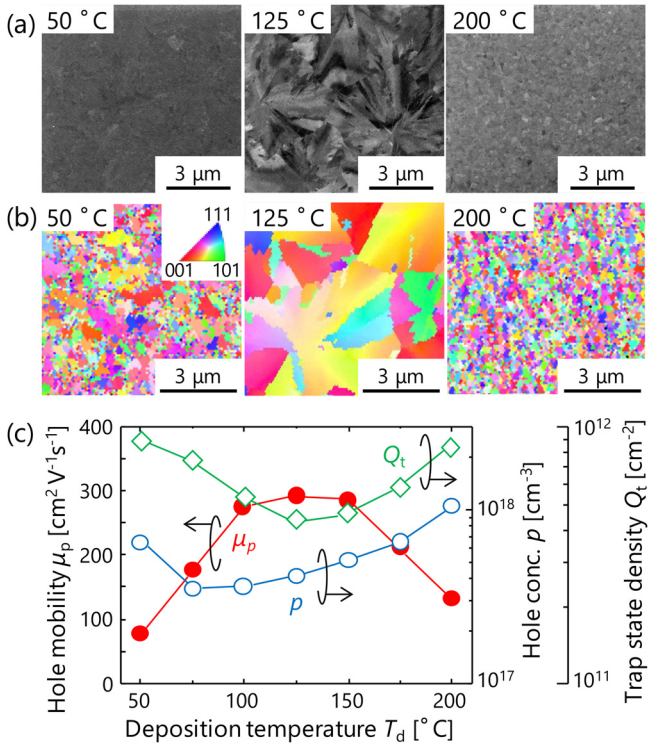

FIG. 3. Effects of the deposition temperature (T_d) on the crystal and electrical properties of the poly-Ge thin films (thickness: 100 nm) formed by SPC. (a) SEM and (b) IPF images of the samples annealed at 450 °C with $T_d = 50$, 125, and 200 °C. The coloration in the EBSD images indicates the crystal orientation according to the legend. (c) Hole mobility (μ_p), hole concentration (p), and trap state density (Q_t) of grain boundaries as a function of T_d. Here, μ_p and p were obtained from Hall effect measurements, and Q_t was calculated from their temperature dependence.[66]

$T_d = 50$ °C corresponds to the condition without substrate heating; it is the temperature that naturally increases owing to the radiative heat from the Ge evaporation source. The $T_d = 125$ °C sample displays larger and more defined grains, reflecting the channeling effect in SEM,[82] than the samples with $T_d = 50$ and 200 °C, indicating that $T_d = 125$ °C promotes optimal grain growth. Figure 3(b) shows inverse pole figure (IPF) maps obtained via electron backscattering diffraction (EBSD), highlighting the crystal orientations with distinct colors. The $T_d = 125$ °C sample has the largest grains, consistent with SEM observations, while the samples with $T_d = 50$ and 200 °C exhibit smaller grains. Figure 3(c) plots μ_p, p, and trap state density (Q_t) as functions of T_d. The highest μ_p (280 $cm^2\ V^{-1}\ s^{-1}$) is observed for $T_d = 125$ °C, which coincides with the large grain size observation. p also depends on T_d. This behavior primarily reflects the grain boundary density, considering that acceptor defects are presented in both the grain interior and grain boundaries of poly-Ge.[83,84] The Q_t values were calculated from the temperature dependence of μ_p,[66] which depended on T_d. The small Q_t at $T_d = 125$ °C contributes to high μ_p. These results highlight the critical influence of T_d on the subsequent SPC processes.

The effect of T_d on the SPC can be explained from the perspective of atomic density. Figure 4 illustrates how T_d influences the SPC process and the resulting properties of poly-Ge thin films. Figure 4(a)

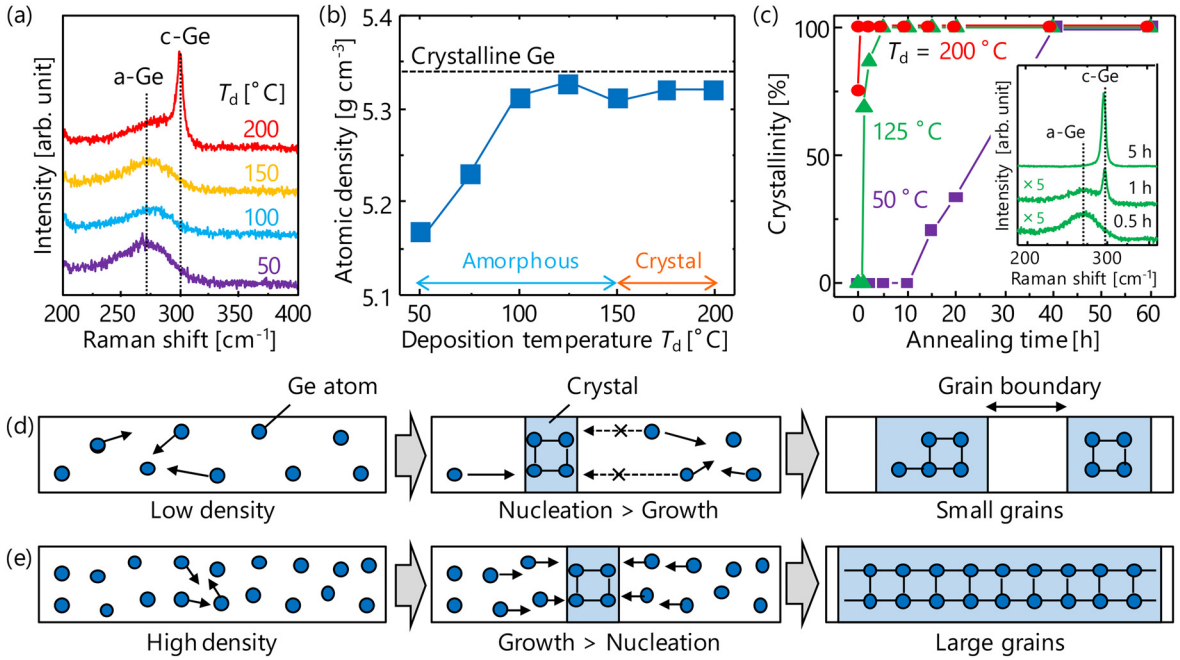

FIG. 4. Discussion of the effects of the deposition temperature (T_d) on the SPC process. (a) Raman spectra for the as-deposited Ge layers with $T_d = 50$, 100, 150, and 200 °C. (b) Atomic density of the as-deposited Ge layers as a function of T_d, determined by the XRR measurement. The data for crystalline Ge are shown by the dotted line. The distinction between amorphous and crystalline regions was determined by the Raman measurements. (c) Crystallinity for samples with $T_g = 400$ °C and $T_d = 50$, 125, and 200 °C as a function of annealing time, which was determined using the annealing-time evolution of the Raman spectra, representatively shown in the insertion ($T_d = 125$ °C). The thickness of the Ge layers is 100 nm. Schematic of the SPC process for amorphous precursor films with (d) low and (e) high atomic density.

shows Raman spectra for samples deposited at $T_d = 50$–200 °C. The samples with $T_d = 50$, 100, and 150 °C exhibit broad peaks near 270 cm^{-1}, corresponding to a-Ge.[85] The $T_d = 200$ °C sample exhibits a sharp peak near 300 cm^{-1}, corresponding to crystalline Ge (c-Ge), in addition to the a-Ge peak. These results indicate that the samples with $T_d \leq 150$ °Care in an amorphous state, while the $T_d = 200$ °C sample includes both crystalline and amorphous states, implying partial crystallization during deposition. Figure 4(b) shows the atomic density of the as-deposited Ge layers, measured by x-ray reflectivity (XRR), as a function of T_d. The density increases with T_d and approaches that of c-Ge, indicating a transition from a low-density amorphous phase to a high-density phase that closely resembles a crystalline structure. It should be noted that while the change in absolute density is around 0.5%, the difference in density between the crystalline and amorphous phases, i.e., the atomic displacement required for crystallization, is approximately an order of magnitude larger in relative terms. Figure 4(c) presents the crystallinity of the Ge layer as a function of annealing time for samples with $T_g = 400$ °C and $T_d = 50$, 125, and 200 °C, where crystallinity is defined as the ratio of the Raman peak intensity of c-Ge to that of a-Ge. The annealing time required to complete crystallization is dramatically reduced by increasing T_d. This implies that a higher T_d results in higher growth rate. Figures 4(d) and 4(e) schematically depict the SPC mechanisms for low- and high-density amorphous precursors. The generated nuclei grow laterally by incorporating surrounding atoms. As shown in Fig. 4(d), because the atomic spacing is large, another nucleation occurs before lateral growth progresses. Therefore, a low-density precursor forms isolated nuclei that grow separately, resulting in numerous grain boundaries and small grains. Conversely, Fig. 4(e) illustrates that a denser amorphous structure promotes more efficient incorporation of surrounding atoms into growing nuclei, thereby enhancing lateral grain expansion before additional nucleation events can occur. This effect stems from the shorter average atomic distances in high-density amorphous films, which reduces the atomic diffusion length required for lateral growth. Although both nucleation and lateral growth are accelerated as atomic density increases, our experimental observations indicate that lateral growth is enhanced more significantly, resulting in larger grain sizes. It is worth noting, however, that in the case of low-density amorphous Ge films ($T_d = 50$ °C), the resulting grain size is too small to allow reliable quantification of lateral growth rates. As a result, our conclusion is primarily based on experimental trends in the resulting grain size rather than the direct measurement of growth velocities or quantitatively established theory. In general, the growth rate depends on the crystallographic orientation; however, since poly-Ge layers formed by SPC are generally randomly oriented [Fig. 3(b)], this phenomenon is presumed to occur regardless of orientation. Thus, a narrow high-density regime around $T_d = 125$ °C produces large-grained poly-Ge with high crystallinity, leading to superior electrical performance.

Controlling T_d is also effective in the SPC of SiGe alloys.[86] Figure 5 presents the influence of T_d on the crystallinity and electrical properties of $Si_{1-x}Ge_x$ thin films formed by SPC. Figure 5(a) displays IPF maps obtained via EBSD, summarizing the crystal orientations for samples across a matrix of T_d values (50–350 °C) and Ge fractions (x). For each x, larger grains are observed at intermediate T_d values. As x

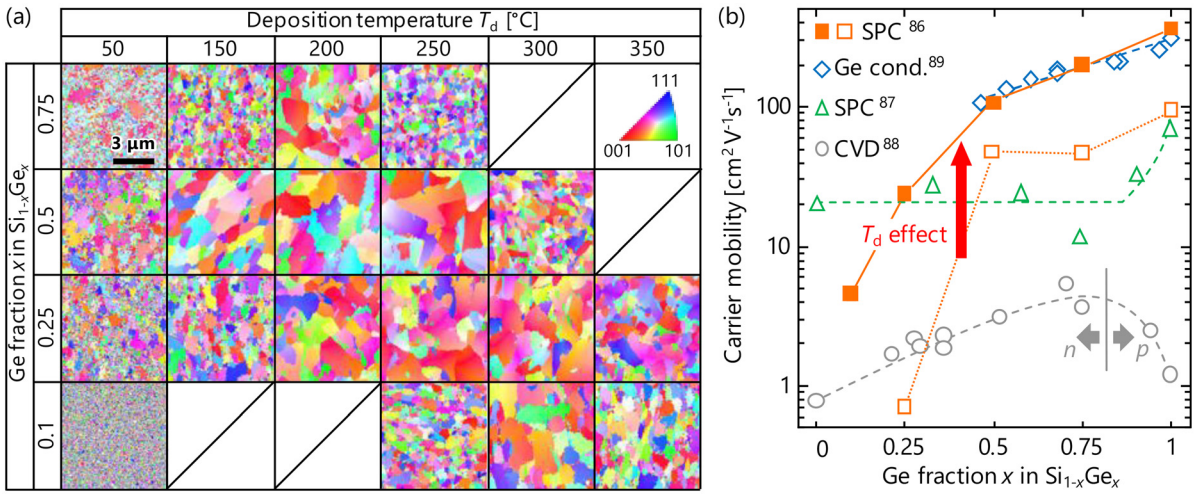

FIG. 5. Effects of the deposition temperature (T_d) on the SPC of $Si_{1-x}Ge_x$ (thickness: 200 mm). (a) IPF images summarized as a matrix composed of T_d and x. Hole mobility (μ_p) as a function of x, where the precursors were prepared with heating (closed squares: $T_d = 150\,°C$ for $x = 1$, 200 °C for $x = 0.75$ and 0.5, and 300 °C for $x = 0.25$ and 0.1) and without heating (open squares: $T_d = 50\,°C$) during deposition. The data of conventional $Si_{1-x}Ge_x$ obtained by SPC,[87] CVD,[88] and Ge condensation[89] are shown for comparison. Only the CVD samples with $x < 0.8$ have electrons as carriers, while the other samples have holes.

increases, larger grains are achieved at a lower T_d, reflecting the lower crystallization temperature of Ge compared to that of Si.[20,57] Figure 5(b) plots μ_p as a function of x for samples deposited with and without substrate heating. The samples with the optimized T_d exhibit significantly higher μ_p than those without heating ($T_d = 50\,°C$). The decrease in μ_p with decreasing x is likely attributed to an increase in the effective mass of holes[1] and the grain boundary barrier height (E_B) depending on p.[77–79] A comparison with conventional SPC and CVD highlights that heating during precursor deposition in SPC significantly enhances μ_p.[87,88] Although a direct comparison is not possible due to differences in synthesis temperature and carrier concentration, the high mobility of T_d-controlled poly-SiGe is attributed to its larger grain size and fewer grain boundaries. These results demonstrate that careful control of T_d, tailored to x, can optimize the SPC process and produce high-quality $Si_{1-x}Ge_x$ thin films with superior electrical performance, comparable to single-crystal SiGe grown at high temperatures via Ge condensation methods.[89] It has also been found that T_d control is effective for the SPC of III-V compound semiconductor thin films,[90] suggesting a high degree of universality.

B. Annealing temperature effects

As has long been known, T_g affects SPC, although not as significantly as T_d. Figure 6 demonstrates the influence of T_g on the SPC behavior of Ge thin films, highlighting differences in grain size and

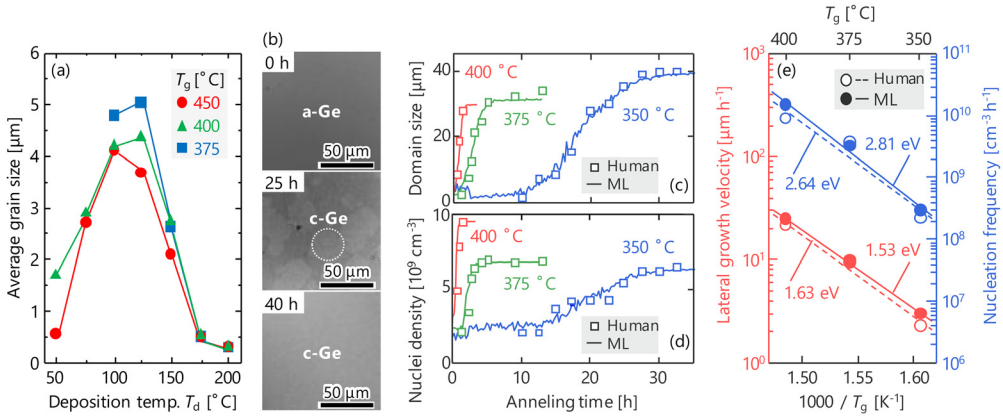

FIG. 6. Effects of the growth temperature (T_g) on the SPC of Ge (thickness: 100 mm). (a) T_g and deposition temperature (T_d) dependence of grain size calculated from EBSD analysis. (b) Time-evolution micrographs showing the SPC process at $T_g = 350\,°C$. (c) Domain size and (d) nuclei density as a function of annealing time, derived from *in situ* micrographs using machine learning and ex-situ micrographs based on human observations. (e) Arrhenius plots of the lateral growth velocity and the nucleation rate, derived from the data in (c) and (d). The activation energies for growth and nucleation are shown near the fitting lines.

growth properties. Figure 6(a) shows the dependence of grain size on T_d and T_g, obtained via EBSD analysis.[66,91] The grain size increases with T_d, reaching a maximum around 125 °C, and then decreases at higher temperatures due to excessive nucleation. The largest grain size is observed in samples with $T_g = 375$ °C, reflecting a balance between nucleation suppression and lateral growth. Figure 6(b) presents time-evolution micrographs capturing the SPC process at $T_g = 350$ °C. The micrographs show the progressive crystallization of a-Ge, with distinct grains emerging over time. Figures 6(c) and 6(d) plot the domain size and nuclei density as functions of annealing time, obtained through *in situ* micrograph analysis using both machine learning (ML) and human observations.[92,93] The ML-derived data closely match the human results but provide finer time resolution and reduced variability. These graphs clearly show that while a lower T_g results in a slower growth rate, a lower nucleation density leads to a larger domain size. Figure 6(e) shows Arrhenius plots of the lateral growth velocity and nucleation frequency derived from Figs. 6(c) and 6(d). From the ML data, the activation energies for nucleation and growth are calculated as 2.81 and 1.53 eV, respectively. The higher activation energy for nucleation suggests that nucleation is more temperature-dependent than lateral growth, meaning that the nucleation rate decreases relative to the growth rate at lower temperatures. Therefore, T_g influences the SPC mechanism, dictating the competition between nucleation and lateral growth. This behavior is consistent with classic SPC kinetics.[19,70]

Post annealing (PA) after SPC is known to reduce p originating from acceptor defects in poly-Ge.[40] Figure 7 shows how PA modifies acceptor defects, focusing on the behavior of deep and shallow acceptor levels.[84] Figure 7(a) presents the temperature dependence of p, measured experimentally and analyzed using linear regression (LR) analysis. LR analysis effectively separates the contributions of deep and shallow acceptor levels. Figure 7(b) shows the positions of the deep and shallow acceptor levels within the Ge bandgap derived from the LR analysis. The deep acceptor level is 53 meV above the valence band, whereas the shallow acceptor level is within 15 meV of the valence band. Figures 7(c) and 7(d) show the densities of the deep and shallow acceptors as functions of T_d before and after PA. Both deep and shallow acceptor densities are lower at intermediate T_d values, which is attributed to the high crystallinity of poly-Ge. The deep acceptor density decreases significantly after PA for small-grained samples with low and high T_d, suggesting the effective passivation of acceptor defects at the grain boundaries. Conversely, the PA effect for shallow acceptor density is more prominent in large-grained samples with intermediate T_d, suggesting that intra-grain acceptor defects are effectively passivated by the annealing process. This indicates that the effectiveness of PA depends on the dominant defect type, which is modulated by the grain size rather than being an inherent result of the grain size alone. From these results, the following can be inferred: deep acceptor levels are attributed to dangling bonds located at the grain boundaries, whereas shallow acceptor levels are attributed to vacancies within the grains. Thus, PA is particularly effective for large-grained poly-Ge, because it compensates for the shallow acceptor defects within the grains.

C. Sn addition in amorphous Ge

GeSn alloys have attracted significant interest as materials for advanced electronic devices because a high substitutional Sn composition in GeSn enables the transition to a direct bandgap[94,95] and enhancement of the carrier mobility.[96–98] Research has been conducted on the synthesis of poly-GeSn thin films using the poly-Ge technologies, such as CVD,[99] laser annealing,[100,101] and SPC.[102–106] A dramatic enhancement of grain size in poly-GeSn films after SPC due to a small amount of Sn addition in a-Ge thin films was reported by Sadoh *et al.* in 2016,[107] before the T_d effect was discovered. Figure 8 shows the structural and electrical properties of poly-Ge(Sn) layers when Sn is added alongside T_d control.[108,109] Figure 8(a) displays IPF maps showing the crystal orientation of poly-Ge(Sn) thin films at various T_d values and initial Sn concentrations (x_i) in the a-GeSn thin films. For $T_d = 50$ °C, the grain size significantly increases with the incorporation of Sn; however, excessive Sn reduces the grain size. Conversely, at $T_d = 125$ °C, the grain size decreases with increasing x_i. Figure 8(b) shows a cross-sectional dark-field TEM image of the $T_d = 125$ °C and $x_i = 3.2\%$ sample, indicating a uniform and defect-free GeSn thin film.

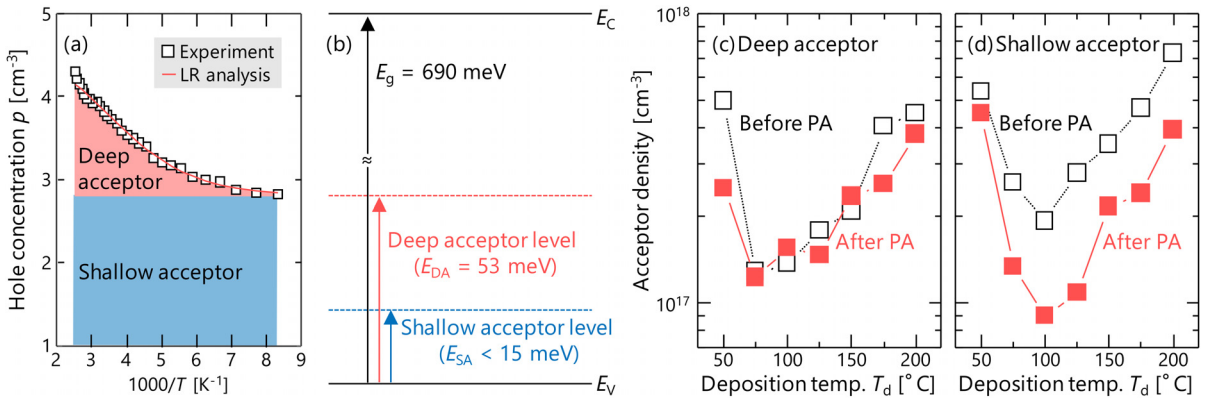

FIG. 7. Effect of post annealing (PA) on the acceptor defects in the poly-Ge layers (thickness: 100 mm). (a) Hole concentration (p) dependence on the measured temperature (T) and (b) acceptor levels shown in the bandgap structure of Ge, determined by the linear regression analysis. Densities of (c) deep and (d) shallow acceptors before and after PA as a function of the deposition temperature (T_d).

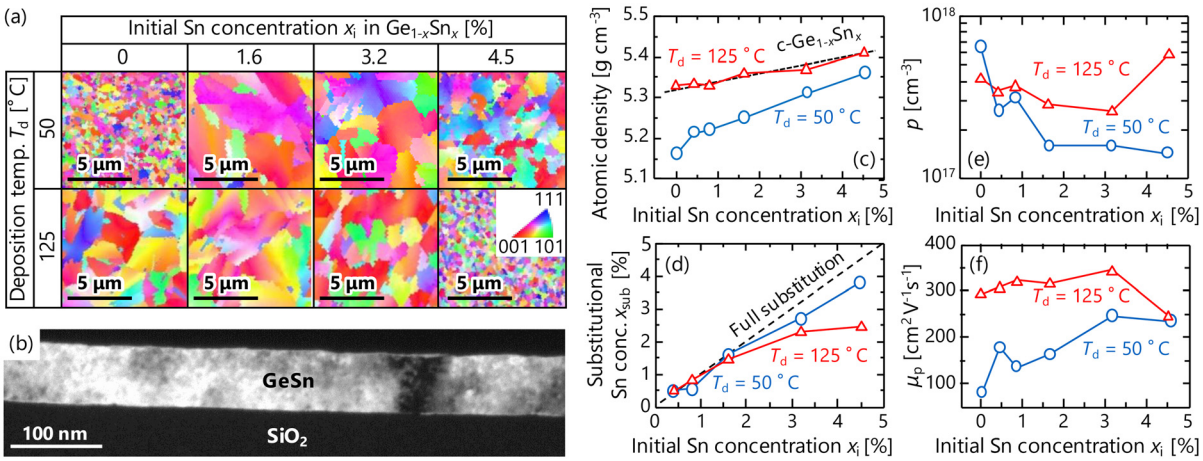

FIG. 8. Effects of Sn addition on the Ge layer (thickness: 100 mm) as an SPC precursor. (a) IPF images organized as a matrix composed of deposition temperature (T_d: 50 and 125 °C) and initial Sn concentration x_i in $Ge_{1-x}Sn_x$ (x: 0%, 1.6%, 3.2%, and 4.5%). (b) Cross-sectional dark-field TEM image of the sample with $T_d = 125$ °C and $x_i = 3.2\%$. (c) Atomic density, (d) substitutional Sn concentration (x_{sub}), (e) hole concentration (p), and (f) hole mobility (μ_p) of the GeSn layer for $T_d = 50$ and 125 °C as a function of x_i. The dotted line in (c) shows the data for c-$Ge_{1-x}Sn_x$, while that in (d) shows the line when the initial Sn is fully substituted.

As shown in the TEM image, large-grained Ge(Sn) thin films formed through T_d control or Sn addition exhibit high crystallinity.[107,109]

The mechanism of grain size enlargement due to Sn addition remains unclear; however, based on our understanding of the T_d effect, we attempted to explain it from the perspective of atomic density.[108] Figure 8(c) shows the atomic densities of GeSn thin films, obtained via XRR. For both $T_d = 50$ and 125 °C, the atomic density increases with x_i. For $T_d = 125$ °C, the atomic density of a-GeSn is equivalent to that of c-GeSn over the entire x_i. Conversely, for $T_d = 50$ °C, the atomic density of a-GeSn gradually approaches that of c-GeSn with increasing x_i range. Although an increase in atomic density due to Sn addition is confirmed, its effect is smaller than that of T_d control. The increase in grain size caused by Sn addition is possibly due to the weakening of a-Ge bonds resulting from interactions with Sn atoms, which could enhance the lateral growth of crystals. Figure 8(d) shows the substitutional Sn concentration (x_{sub}) measured from Raman spectra,[110,111] indicating the portion of Sn incorporated into the Ge lattice. For samples with $x_i \leq 1.6\%$, all Sn atoms substitute for Ge, which is reasonable considering the solubility limit of Sn in Ge.[112,113] For the samples with $x_i > 1.6\%$, although Sn is not completely substituted, x_{sub} exceeds the solubility limit. This is a commonly observed phenomenon in the growth of GeSn in nonequilibrium systems including SPC.[46,101,103] Unsubstituted Sn precipitate on the film surface and can be removed by wet etching.[109,114] Figures 8(e) and 8(f) present p and μ_p as functions of x_i. For $T_d = 50$ °C, higher x_i results in lower p and higher μ_p, likely due to the larger grain size. In particular, p drops as low as 1.4×10^{17} cm^{-3}, which represents one of the lowest levels reported for poly-Ge-based thin films. Even at $T_d = 125$ °C, Sn addition leads to a decrease in p and an increase in μ_p for $x_i \leq 3.2\%$, despite the reduction in grain size, allowing for the μ_p value of 350 cm^2 V^{-1} s^{-1}. From the measurement temperature dependence of μ_p, it has been found that Sn addition reduces Q_t and E_B by approximately 40%.[108] Therefore, the decrease in p and the increase in μ_p due to Sn addition are interpreted as being caused by grain boundary passivation in poly-Ge.

D. Thickness effects

Film thickness is an important factor, because the required specifications vary depending on the device application. Figure 9 illustrates how the thickness of poly-Ge(Sn) thin films affects their structural and electrical properties, focusing on μ_p. Figure 9(a) shows μ_p as a function of the initial Ge thickness (t_i). μ_p decreases as t_i decreases, but the reduction is particularly extreme at $t_i = 50$ nm. The inset IPF images reveal that the grain size is small for $t_i = 50$ nm due to the difficulty in achieving a high film density.[91] The small grain size could be a factor contributing to the low μ_p; however, it is important to note that the grain size is also small in the $t_i = 500$ nm sample, likely due to an increase in bulk nucleation.[19] To verify this, we reduced the film thickness while maintaining the large grain size of the poly-Ge(Sn) film with $t_i = 100$ nm and $T_d = 125$ °C using chemical-mechanical polishing (CMP).[114,115] Figure 9(b) plots μ_p as a function of thickness after CMP (t_{CMP}) for different x_i. For all samples, μ_p decreases dramatically with decreasing t_{CMP}. These results suggest that scattering factors for carriers, such as defects and fixed charges, exist near the interface between the substrate and Ge(Sn) film. The reduction in grain size and carrier mobility due to the thin-film formation of poly-Ge(Sn) is commonly observed.[107,109,116] Various strategies have been explored to suppress carrier interface scattering in applications requiring thin films, such as thin-film transistors, as discussed in the Subsection III E.

E. Effects of interfacial layer

Inserting an interfacial layer is an effective approach for suppressing heterogeneous nucleation and carrier scattering at the Ge/substrate interface.[117–119] Figure 10 shows how interfacial layers affect the crystallization behavior and μ_p of poly-Ge(Sn) layers during SPC. Figure 10(a) presents IPF images of Ge layers with and without a GeO_x underlayer. The GeO_x underlayer reduces interfacial nucleation due to the diffusion of oxygen atoms from GeO_x into Ge, resulting in large grains.[68,118] Using this method, the poly-Ge film formed on a polyimide (PI) substrate exhibits a μ_p of 690 cm^2 V^{-1} s^{-1},[68] the highest

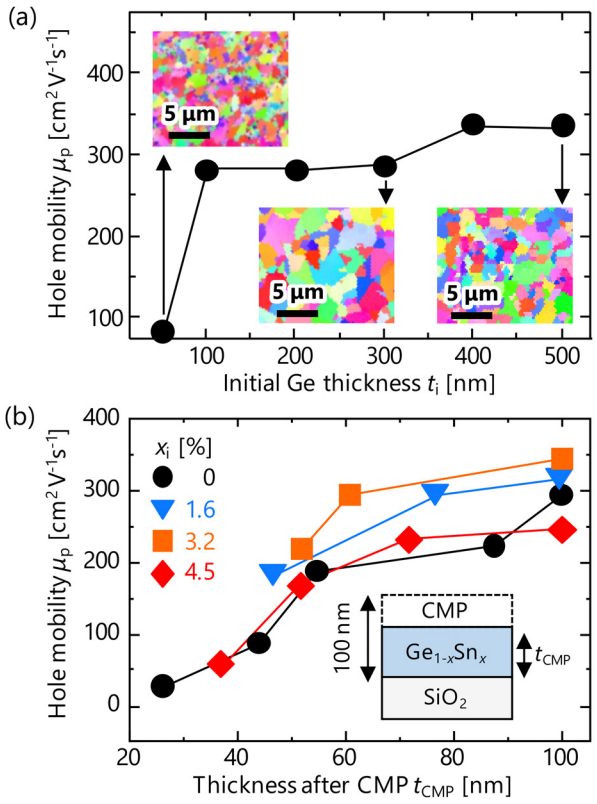

FIG. 9. Effects of thickness on the poly-$Ge_{1-x}Sn_x$ layers. (a) Hole mobility (μ_p) of Ge as a function of the initial Ge thickness t_i. The IPF images of the samples with $t_i = 50$, 300, and 500 nm are shown as inserts. (b) μ_p of $Ge_{1-x}Sn_x$ (x: 0%, 1.6%, 3.2%, and 4.5%) as a function of $Ge_{1-x}Sn_x$ thickness after CMP (t_{CMP}). The deposition (T_d) and growth temperatures (T_g) are 125 and 450 °C, respectively.

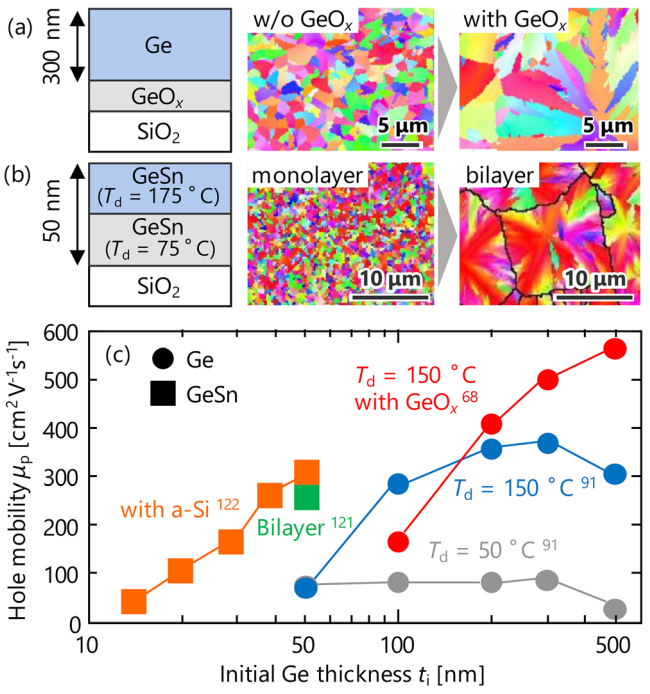

FIG. 10. Effects of interfacial nucleation suppression on the poly-$Ge_{1-x}Sn_x$ layers. (a) IPF images of the Ge layers ($T_g = 375$ °C, $T_d = 150$ °C, 300 nm thickness), with and without a GeO_x underlayer. (b) IPF images of the $Ge_{0.98}Sn_{0.02}$ ($T_g = 400$ °C) with monolayer ($T_d = 125$ °C, 50 nm thickness) and bilayer ($T_d = 75$ and 175 °C, 25 nm thickness each) structures. (c) Comparison of the hole mobility (μ_p) of the poly-Ge(Sn) layers as a function of initial Ge thickness (t_i), where reference numbers are shown near each symbol.

recorded among poly-Ge(Sn) thin films. By combining GeSn with the GeO_x underlayer, p is reduced to below the order of 10^{17} cm^{-3}.[120] However, the GeO_x underlayer significantly reduces μ_p of thin ($t \leq 100$ nm) Ge films due to the presence of oxygen at the bottom of the Ge film. Figure 10(b) displays IPF images of $Ge_{0.98}Sn_{0.02}$ films grown as a monolayer ($T_d = 125$ °C, 50 nm) and as a bilayer ($T_d = 75$ and 175 °C, 25 nm each). In the bilayer structure, the bottom layer with a low T_d delays nucleation at the interface, whereas the top layer with a high T_d promotes lateral growth, resulting in larger grains than those in the monolayer.[121] This enables relatively large grain sizes and high μ_p even in thin films (50 nm). The GeSn thin film is preferentially (100)-oriented, which is consistent with previous studies on laser and flashlamp annealing.[38,74] Considering the suppression of nucleation at the substrate interface in this bilayer structure, heterogeneous nucleation at the GeSn film surface may have lower energy on the (100) plane.

Figure 10(c) compares μ_p as a function of t_i. While T_d control and the insertion of a GeO_x underlayer significantly enhance μ_p in thick films ($t_i \geq 100$ nm), their effects are not observed in thin films ($t_i \leq 50$ nm) due to the small grain size.[68,91] A bilayer structure with modulated T_d is effective for thin films ($t_i = 50$ nm), enabling larger grain sizes and higher μ_p.[121] Sandwiching the GeSn film between a-Si layers is currently the most promising approach for achieving high μ_p in thin films ($t_i \leq 50$ nm).[122] This method not only suppresses interfacial nucleation to promote larger grain sizes in GeSn thin films but also reduces carrier scattering at the interface. Combining these techniques is crucial for achieving high-performance poly-Ge(Sn) thin-film transistors.

F. Impurity doping for Fermi level control

Fermi level control is essential for all semiconductor devices. In particular, achieving n-type doping in poly-Ge thin films is challenging.[123] However, high-concentration n-type doping has been realized using near-nonequilibrium processes such as laser annealing,[124,125] flashlamp annealing,[126] and MIC.[127,128] Nevertheless, the crystallinity remains suboptimal. Figure 11 illustrates the effects of solid-phase diffusion doping on the electrical properties of poly-Ge-based thin films synthesized via advanced SPC.[129,130] Figure 11(a) presents a schematic of the doping process. The poly-Ge layer is coated with a spin-on-glass (SOG) solution containing dopants (Ga, Al, and B for p-type; P, As, and Sb for n-type), followed by diffusion annealing and subsequent SOG removal. This method enables impurity doping without damaging the crystal structure. Figures 11(b) and 11(c) show IPF images of the samples annealed at 450 °C with $T_d = 50$ and 150 °C. Solid-phase diffusion doping is performed under similar conditions. Figures 11(d) and 11(e) display the carrier concentration and mobility for p-type

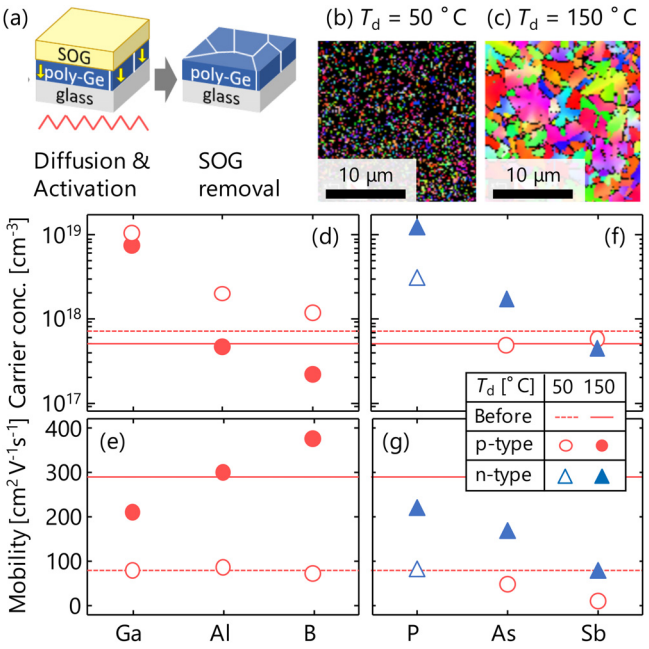

FIG. 11. Impurity doping into poly-Ge (thickness: 100 mm) using the solid-phase diffusion method. (a) Schematic of the spin-on-glass (SOG) solution-based process. IPF images of the samples after SPC at 450 °C with deposition temperatures (T_d) of (b) 50 and (c) 150 °C. Dependence of the electrical properties of poly-Ge on dopant species at $T_d = 50$ and 150 °C. (d) and (f) Carrier concentration and (e) and (g) carrier mobility for (d) and (e) p-type and (f) and (g) n-type dopants. Dopant diffusion is at 750 °C for 15 min for p-type dopants (Ga, Al, and B) and 550 °C for 30 min for n-type dopants (P, As, and Sb). The solid ($T_d = 150$ °C) and dotted ($T_d = 50$ °C) lines show the data of samples before doping.

dopants (Ga, Al, B) after diffusion annealing at 750 °C. At $T_d = 50$ °C, all p-type dopants increase p, while at $T_d = 150$ °C, Al and B lead to a decrease in p. These behaviors are likely due to two factors: smaller grains facilitate dopant diffusion through grain boundaries,[131] while PA reduces acceptor defects.[84] Among the p-type dopants, Ga results in the highest p for both T_d values. For $T_d = 50$ °C, the μ_p values are similar across all samples, as grain boundary scattering limits mobility due to the small grain size. At $T_d = 150$ °C, μ_p values are 210, 300, and 380 cm^2 V^{-1} s^{-1} for Ga, Al, and B, respectively, which is the inverse of the trend observed in p. This inverse relationship reflects the typical behavior of single-crystalline semiconductors, where higher doping levels result in stronger impurity scattering and reduced mobility.[80,81] The behavior in the poly-Ge layers is attributed to the larger grains and lower E_B.[66] Figures 11(f) and 11(g) present the results for n-type dopants (P, As, and Sb) after diffusion annealing at 550 °C. At $T_d = 150$ °C, all dopants successfully formed n-type Ge thin films, whereas at $T_d = 50$ °C, only P was achieved. This is due to P having a higher activation rate in Ge compared to As and Sb,[62–65] suggesting that activating n-type dopants in poly-Ge with small grains is challenging. Electron mobility (μ_n) is higher in $T_d = 150$ °C samples than in $T_d = 50$ °C samples, reflecting the effect of grain size. The P-doped sample at $T_d = 150$ °C exhibits the highest μ_n, at its higher n reduces E_B. These results indicate that Ga and P are the most effective p-type and n-type dopants, respectively, for achieving high-performance poly-Ge thin films via solid-phase diffusion doping.

The aforementioned method is simple; however, a drawback is that high-temperature annealing is required for dopant diffusion.[129,130] Therefore, we explored the co-deposition of a dopant during Ge deposition, followed by activation during the SPC process.[67,132,133] Figure 12 shows the influence of T_d and dopant type (P, As, and Sb) on the crystallization behavior and electrical properties of the poly-Ge layers. Figure 12(a) displays IPF images organized in a matrix according to T_d and dopant type with a dopant concentration (C_d) of 3.0×10^{20} cm^{-3}. P and As doping produce larger grains at a lower T_d, similar to Sn addition. In contrast, for the Sb-doped samples, the grain size peaks at $T_d = 125$ °C. This phenomenon is also observed in GeSiSn alloys.[134] Figure 12(b) shows Arrhenius plots of the nucleation rate and lateral growth velocity for the P-, As-, and Sb-doped samples. For each sample, the nucleation rate and lateral growth velocity are approximated by straight lines, indicating that SPC follows an activation reaction.[19,70] The slopes of these lines, which depend on the activation energies required for nucleation and growth, vary depending on the dopant type. As evident from the series of results with Sn and n-type impurity additions, the impurity species affect the SPC of Ge, and the appropriate selection of impurity species can significantly enhance the grain size of poly-Ge thin films. Figures 12(c) and 12(d) present μ_n and n as functions of C_d. For all dopant species, μ_n peaks around $C_d = 2.0 \times 10^{20}$ cm^{-3}. This behavior is consistent with grain size, indicating that μ_n is predominantly limited by grain boundary scattering of electrons.[77,78] For the P- and As-doped samples, n increased with increasing C_d and then began to decrease. This behavior may be due to dopant segregation with increasing C_d, especially at grain boundaries.[77,78] For the Sb-doped samples, n remains relatively low. The variation in n depending on the dopant species is consistent with fundamental properties, reflecting the solid solubility and diffusion rate of the dopants in Ge [62–65]. P doping is the most effective method for achieving high-performance n-type poly-Ge layers, as it enhances grain size and reduces Q_t.[67] By combining Sn addition, a mobility of 450 cm^2 V^{-1} s^{-1} has been achieved, which is the highest recorded value for n-type poly-Ge(Sn) thin films.[69]

G. Strain effects

In SPC, during the annealing process, strain is induced in the resulting polycrystalline thin films due to the difference in thermal expansion coefficients between the film and the substrate. This strain is not large enough to induce band modulation in Ge[135] but has a noticeable impact on the properties of poly-Ge thin films.[136,137] Figure 13 illustrates the effect of strain on the crystallinity and electrical properties of poly-Ge layers, modulated by different substrate materials. Figure 13(a) presents the temperature profile during SPC and the strain history in the Ge layer. Initially, strain is introduced during heating due to the thermal expansion difference ($\Delta\alpha$) between Ge and the substrate. The strain relaxes during nucleation and grain growth and reappears during cooling with the opposite polarity. Figure 13(b) shows photographs of P-doped n-type samples grown on substrates with different thermal expansion coefficients (SiO_2, Si, CaF_2, and PI).[137] Undoped p-type samples were also fabricated on the same type of substrate.[136] To standardize the influence of the Ge/substrate interface, a GeO_2 underlayer is inserted. The substrates produce different strain states in poly-Ge: tensile strain on SiO_2 and Si and compressive strain on CaF_2 and PI. Figure 13(c) plots the strain value (ε) vs $\Delta\alpha$, derived from Raman spectra.[138] Tensile strain ($\varepsilon > 0$) occurs when

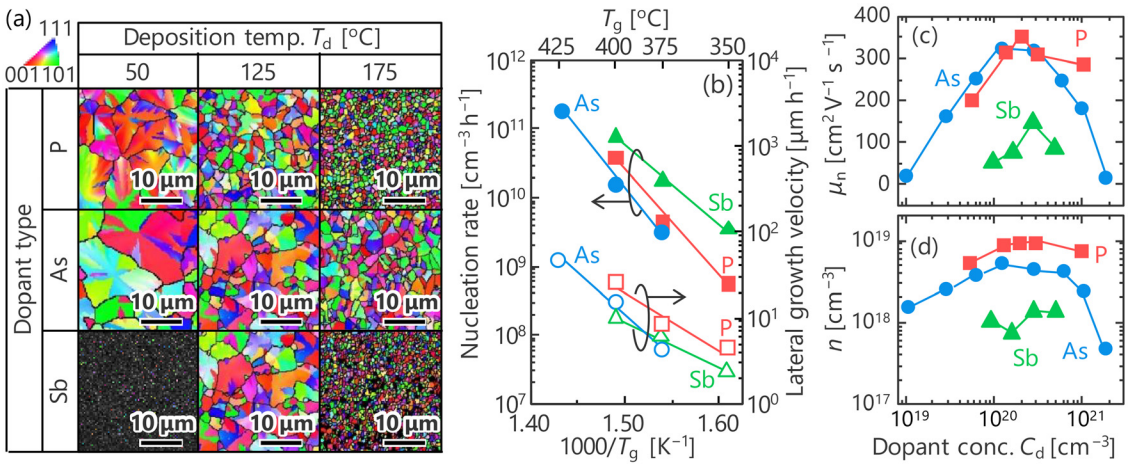

FIG. 12. Effects of using n-type impurity doping in the Ge layer (thickness: 200 mm) as an SPC precursor. (a) IPF images summarized as a matrix composed of deposition temperature T_d (50, 125, and 175 °C) and dopant type (P, As, and Sb), where the dopant concentration (C_d) is $= 3.0 \times 10^{20}$ cm^{-3}. (b) Arrhenius plots of the nucleation rate and lateral growth velocity. (c) Electron mobility (μ_p) and (d) electron concentration (n) as a function of C_d. T_d is 50 °C (As) and 125 °C (P and Sb) for the samples in (b), (c), and (d).

$\Delta\alpha < 0$, and compressive strain ($\varepsilon < 0$) when $\Delta\alpha > 0$. The experimental results closely align with theoretical predictions, which can be expressed by the equation: $\varepsilon = \Delta\alpha\Delta T/(1-\nu)$, where ΔT is the temperature change during cooling and ν is the Poisson's ratio of the thin film.[139] This result indicates that the strain originates primarily from the thermal expansion mismatch. In p-type samples, the grain size increases with the absolute value of ε,[136] whereas in n-type samples, the opposite trend is observed.[137] Regarding the impact of strain on crystal growth, some reports suggest that it promotes nucleation,[140] while others indicate that it enhances lateral growth.[141] This discrepancy may reflect differences in the properties of amorphous films.

E_B was calculated from the temperature dependence of carrier mobility, revealing an interesting correlation with strain. Figure 13(d) shows E_B as a function of $\Delta\alpha$. For p-type Ge, E_B increases with tensile strain but decreases with compressive strain, whereas n-type Ge exhibits the opposite trend. This contrasting behavior is attributed to the piezoelectric effect.[142–145] In polycrystalline semiconductors, carrier trapping at grain boundaries shifts the local energy levels such that a potential barrier forms between the grains and the boundaries. This phenomenon gives rise to E_B, which hinders carrier transport. When strain is applied to a poly-Ge layer, polarization vectors emerge within grains, aligned in the strain direction. The charge induced near the grain boundaries by this polarization (piezo-charge) interacts with the trapped carriers. If the piezo-charge and trapped carriers are of opposite types, charge compensation reduces E_B. Conversely, when they are of the same type, E_B increases. This strain-dependent modulation of E_B in poly-Ge aligns with the principles of the piezoelectric effect. These findings provide valuable insights into the strain engineering of Ge-based devices.

H. Grain boundary control using metals

Thus far, we have discussed the enlargement of poly-Ge thin film grains; however, the positions of the grains and grain boundaries remain random. Controlling grain boundaries is desirable for several device applications, including thin-film transistors. In the case of Si, metal-induced lateral crystallization (MILC), which uses a metal catalyst as the growth initiation point, has been employed to achieve grain boundary alignment[146,147] and high-mobility transistors.[148,149] The MILC of Ge has also been investigated using several metals, such as Ni,[150–154] Co,[153,154] Pd,[153,154] Cu,[154] Sn,[155] and Au;[156] however, achieving large grain growth has been challenging,[152,154] similar to conventional SPC. To address this issue, we attempted to align the grain boundaries in poly-Ge thin films by applying MILC to the precursor of large-grained SPC, testing 24 different metals in the process.[157] Figure 14 illustrates the effects of Ni and Au catalysts on grain boundary control in poly-Ge layers through MILC. Figure 14(a) presents the structure and IPF image of the Ni-catalyzed sample.[158] Ni-induced MILC produces large, rod-shaped grains aligned along the ⟨110⟩ direction, attributed to the lattice matching between NiGe{100} and Ge{110} planes. Although the mechanism behind the preferential {110} orientation in the normal direction remains uncertain, it is believed to reflect a stable surface when lateral growth proceeds along the ⟨110⟩ direction. Figure 14(b) displays an Au-catalyzed sample with a multilayer Ge structure with a modified T_d.[159] This multilayer structure suppresses heterogeneous nucleation at the Ge interface, enabling long-range MILC growth by mitigating the inhibition caused by spontaneous nucleation. While Ge grains are small near the Au catalyst, they expand as growth progresses and converge to the {100} orientation. The preferential {100} orientation is commonly observed in unidirectional melt-grown Ge, which has been discussed in terms of interfacial energy minimization.[38,73] Figure 14(c) presents a cross-sectional TEM image of the Au-catalyzed sample, showing the high crystallinity of Ge. For both Ni and Au catalyzed samples, although the residual metal concentration in Ge is below the detection limit of energy-dispersive x-ray spectroscopy, further studies are required to evaluate their effect on carrier transport and lifetime. Ni and Au catalysts produce contrasting growth morphologies and grain orientations due to their different reaction mechanisms: compound formation with Ni results in dendritic {110}-oriented grains, whereas eutectic interactions with Au yield uniform {100}-oriented grains with grain boundary alignment. Similar growth modes have been observed with metals

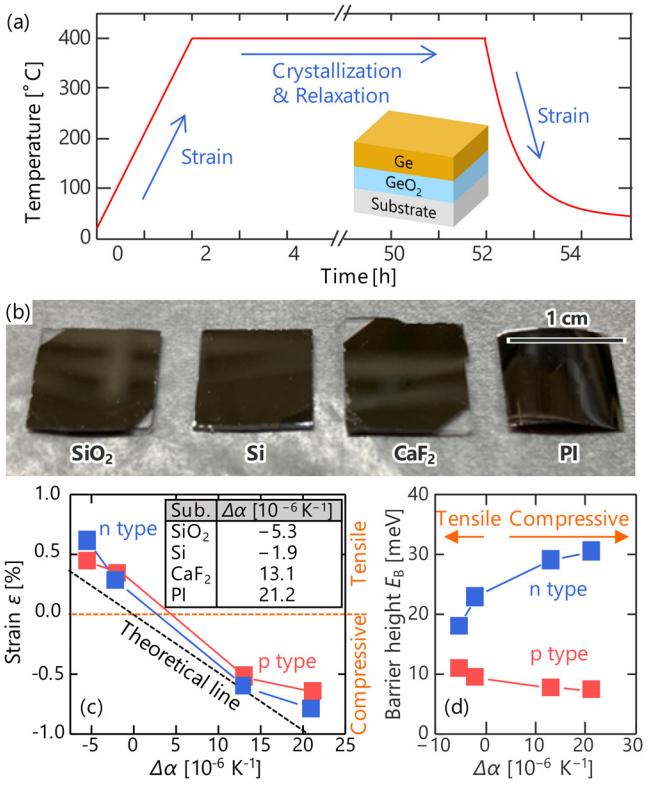

FIG. 13. Effects of strains on the poly-Ge layers (thickness: 100 mm). (a) Temperature profile and strain history in Ge. The inset shows the schematic of the sample structure. (b) Photograph of the samples with a SiO_2, Si, CaF_2, and PI substrate. (c) Strain values (ε) as a function of the coefficient of thermal expansion difference between Ge and the substrate ($\Delta\alpha$), where $\varepsilon > 0$ corresponds to tensile strain and $\varepsilon < 0$ corresponds to compressive strain. The black dotted line shows the theoretical strain.[139] The inserted table shows the correspondence between substrate types and $\Delta\alpha$. (d) Grain boundary barrier height E_B for p-type and n-type Ge layers as a function of $\Delta\alpha$.

other than Ni and Au.[157] These findings highlight the potential of MILC to engineer grain boundary structures and orientations, which are critical for optimizing the electrical performance of poly-Ge-based devices including thin-film transistors.

IV. BENCHMARKS OF ELECTRICAL PROPERTIES

Figure 15 benchmarks the electrical performance of Ge-based thin films directly grown on insulating substrates. The plots illustrate the relationship between carrier mobility and concentration, with dotted lines representing reference data for bulk Si and Ge.[81] It should be noted that this is not necessarily a comparison of the superiority of each method, as film thickness and process temperature vary depending on the technique. All the mobility values presented are Hall mobilities. In single-crystalline Ge-MOSFETs, the field-effect mobility can exceed 1000 $cm^2 V^{-1} s^{-1}$, although it is typically limited by gate dielectric interface scattering.[3–6] In comparison, the Hall mobility of the present poly-Ge layers suggests that only modest degradation is expected when these films are integrated into MOSFET structures. In fact, the field-effect mobility obtained from our fabricated poly-Ge thin-film

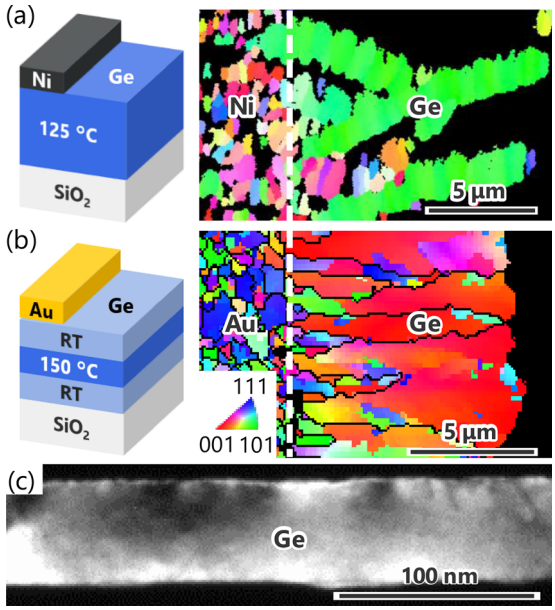

FIG. 14. Grain boundary control of the Ge layers through metal-induced lateral crystallization. Schematic and IPF images of the samples with (a) Ni and (b) Au catalysts. (c) Cross-sectional dark-field TEM image of the samples in (b). The growth conditions for the Ni sample are a 100-nm-thick monolayer Ge with $T_d = 125\,°C$ and $T_g = 325\,°C$, while those for the Au sample are a 50-nm-thick multilayer Ge with T_d = RT for the top and bottom layers, $T_d = 150\,°C$ for the middle layer, and $T_g = 375\,°C$.

transistors is largely consistent with the Hall mobility, implying minimal additional degradation due to interface effects.[114,115,160] Figures 15(a) and 15(b) highlight recent advancements achieved through SPC for p-type and n-type Ge thin films, respectively. More reports are available for p-type films compared to n-type films, reflecting both the natural tendency of poly-Ge thin films to become p-type due to acceptor defects and the difficulty of controlling n-type conduction. As a general trend, μ_p improves as p decreases, whereas μ_n exhibits a peak with respect to n. This phenomenon can be interpreted as follows:[161] in p-type films, due to the lower E_B, μ_p is more susceptible to impurity scattering, particularly in large-grain films. In contrast, in n-type films, the higher E_B makes μ_n more sensitive to grain boundary scattering. Since E_B decreases as n increases,[77,78] μ_n initially rises with increasing n but eventually declines due to impurity scattering. Notably, for both p-type and n-type films, mobility values approaching those of bulk single-crystal Ge, where the mobility is limited by impurity scattering, have been achieved in polycrystalline thin films. The highest mobility values for both types have been recorded in poly-Ge(Sn) thin films formed through our SPC process with T_d control, all synthesized via low-temperature processes below 500 °C. The highest μ_p of 690 $cm^2 V^{-1} s^{-1}$ is achieved through grain enlargement induced by the GeO_x interlayer and strain control enabled by the PI substrate.[68] Although reducing acceptor defects below 10^{17} cm^{-3} is challenging, it has been accomplished through hydrogen incorporation in Ge layers.[162] Conversely, the highest μ_n of 450 $cm^2 V^{-1} s^{-1}$ is obtained on a SiO_2 glass substrate through the co-addition of P and Sn into a-Ge thin films.[69] Although lower, a μ_n of 200 $cm^2 V^{-1} s^{-1}$ has also been

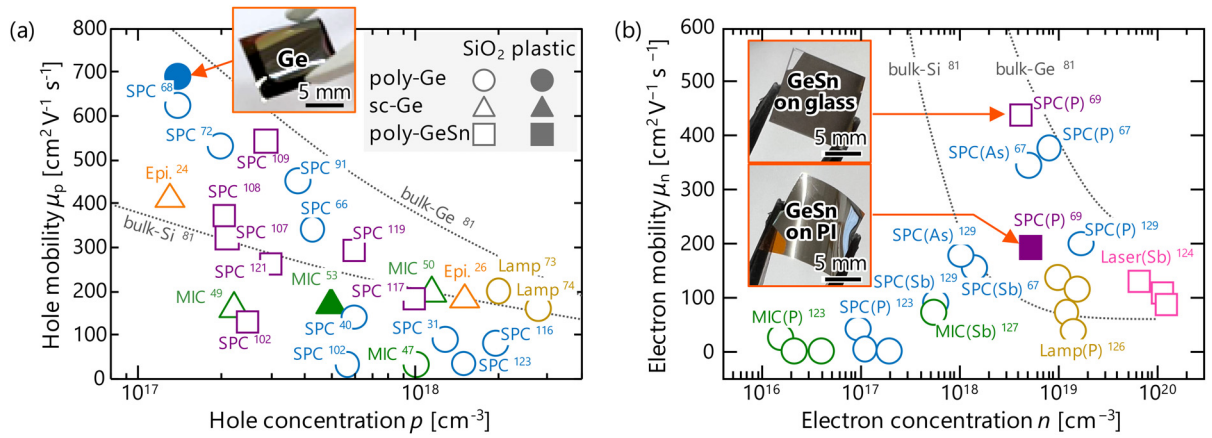

FIG. 15. Benchmarks of the electrical properties of (a) undoped p-type and (b) n-type polycrystalline Ge-based thin films. Representative sample photographs are inserted into each graph. The growth method, reference number, and n-type dopant are shown near each symbol. The dotted lines show the data for bulk Si and Ge,[81] which were derived from electrical conductivity and carrier concentration.

achieved on a PI substrate. These results demonstrate that by optimizing the SPC process of Ge, the highest carrier mobility among semiconductor thin films synthesized at low temperatures on insulating substrates has been achieved. The near-bulk-level electrical performance of poly-Ge(Sn) thin films paves the way for their application in high-performance thin-film transistors and flexible electronic devices.

V. SUMMARY AND PROSPECTS

We provided a comprehensive review of the latest advances in the SPC of poly-Ge thin films. We began by elucidating how conventional SPC processes affect the crystallinity and carrier transport properties of Ge films, highlighting the poor characteristics that must be addressed. By meticulously controlling the amorphous deposition temperature, introducing Sn, optimizing impurity doping, adjusting film thickness, and employing interfacial layers, we have overcome long-standing challenges such as small grain sizes, high densities of acceptor defects, and the difficulty of achieving stable n-type conduction. These process optimizations have led to significant improvements in electrical performance, with p-type films achieving a record-high mobility of 690 cm^2 V^{-1} s^{-1} and n-type films reaching 450 cm^2 V^{-1} s^{-1}, approaching the performance of bulk Ge.

Future research should focus on further reducing acceptor defect densities at low processing temperatures and enhancing the activation efficiency of n-type dopants, both of which remain critical challenges for achieving stable and controlled electrical properties in poly-Ge thin films. Additionally, optimizing semiconductor–dielectric interfaces and exploring novel interfacial layers will be essential for improving device performance, particularly in flexible and large-area electronics. Approaches such as bilayer deposition, interfacial engineering, and strain modulation may prove effective in mitigating carrier scattering and ensuring long-term reliability, while machine learning–driven optimization of SPC parameters could further accelerate materials development.

In addition to these technical refinements, it is important to contextualize poly-Ge within the broader landscape of thin-film semiconductors. Compared to oxide semiconductors, poly-Ge offers significantly higher hole and electron mobility, making it promising for high-speed, low-voltage operation. While oxide semiconductor materials are advantageous for their optical transparency and RT processability, they face limitations in p-type conduction and exhibit moderate mobilities, which constrain their use in complementary logic circuits. Conversely, low-temperature poly-Si, used in the display industry, remains a practical and well-established technology, supported by a mature infrastructure. However, it typically requires high crystallization temperatures and exhibits lower mobility than optimized poly-Ge, making it less favorable for integration into back-end-of-line processes where thermal budget constraints are stringent. In contrast, poly-Ge can achieve high mobility and excellent electrical performance through processes conducted below 500 °C, offering superior back-end-of-line compatibility.

Given these advantages—high mobility, low thermal budget requirements, and integration flexibility—poly-Ge stands out as a compelling platform for next-generation thin-film devices, including transistors, flexible electronics, photonic components, and thermoelectric converters. Continued progress in materials design and process innovation will be essential to unlock the full potential of poly-Ge and establish it as a foundational material in the future of semiconductor technology.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

K. Toko: Conceptualization (lead); Data curation (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (equal); Methodology (equal); Project administration (lead); Resources (lead); Software (equal); Supervision (lead); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **K. Moto:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **T. Imajo:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (supporting). **T. Ishiyama:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Software (lead); Validation (equal); Visualization (equal); Writing – review & editing (supporting). **K. Nozawa:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (supporting). **S. Maeda:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (supporting). **K. Igura:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (supporting). **T. Suemasu:** Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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